Octal registered transceiver (3-State)

54ABT2952

FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- AM2952 functional equivalent
- Outputs sink 48mA and source -24mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883C Method 3015.6 and 200V per Machine Model

DESCRIPTION

The 54ABT2952 is an 8-bit Registered Transceiver. Two 8-bit back registers store data flowing in both directions between two bi-directional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-state output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

ORDERING INFORMATION

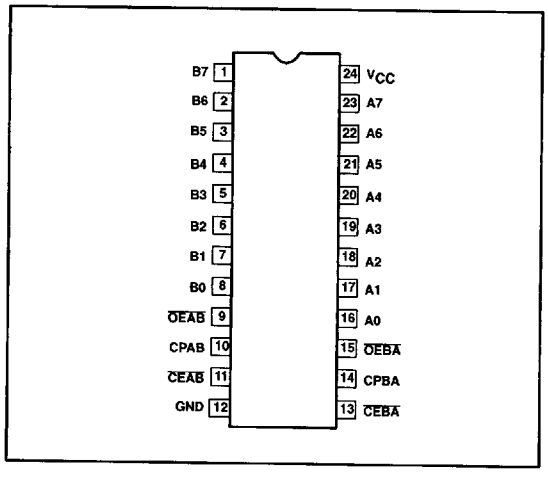
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24-Pin Ceramic DIP	54ABT2952/BLA	GDIP3-T24
28-Pin Ceramic LLCC	54ABT2952/B3A	CQCC2-N28

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

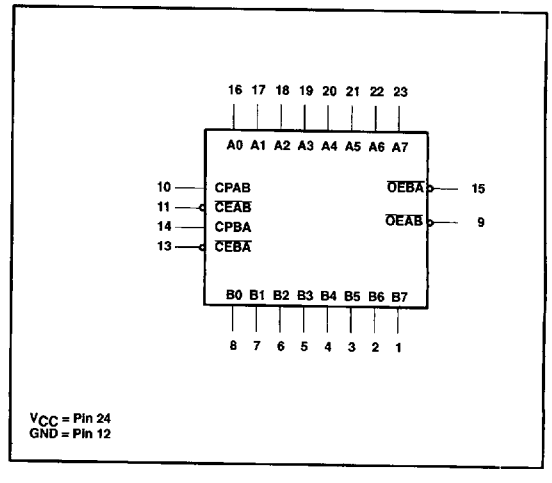
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB/CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{CEAB}/\overline{CEBA}$	Clock enable input A to B / Clock enable B to A
16, 17, 18, 19, 20, 21, 22, 23	A0 - A7	Data inputs/outputs (A side)
1, 2, 3, 4, 5, 6, 7, 8	B0 -B7	Data inputs/outputs (B side)
9, 15	$\overline{OEAB}/\overline{OEBA}$	Output enable input
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

PIN CONFIGURATION



LOGIC SYMBOL



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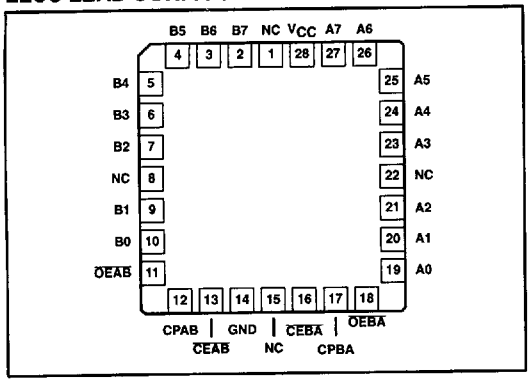
LLCC LEAD CONFIGURATION



FUNCTION TABLE FOR REGISTER An or Bn

INPUTS			INTERNAL	OPERATING
An or Bn	CPXX	$\overline{CEXX}$	Q	MODE
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE FOR OUTPUT ENABLE

INPUT	INTERNAL	An or Bn	OPERATING
$\overline{OEXX}$	Q	OUTPUTS	MODE
H	X	Z	Disable outputs
L L	L H	L H	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

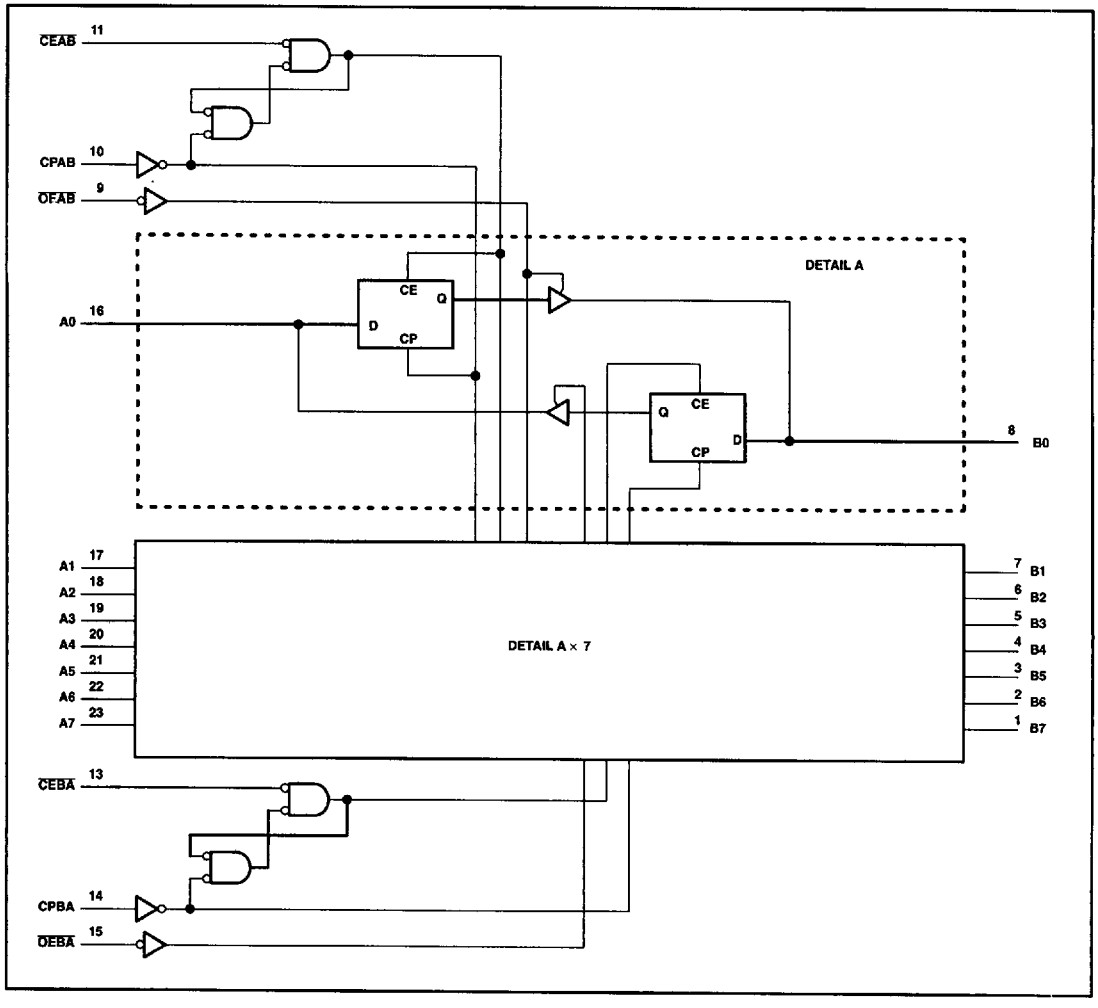
ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage range		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage range[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage range[3]	Output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	96	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-24	mA
I_{OL}	Low-level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-55	+125	°C

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS

(V_{CC} = MAX, V_I = V_{IL} or V_{IH}, T_{amb} = -55 to +125 °C unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V, I_{IK} = -18mA		-0.9	-1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = -3mA	2.5	3.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA	3.0	3.5		V
			V_{CC} = 4.5V; I_{OH} = -24mA	2.0	2.6		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 48mA		0.42	0.55	V
I_I	Input leakage current	Control pins	V_I = GND or 5.5V		±0.01	±1.0	µA
		Data pins[6]	V_I = GND or 5.5V		5	100	µA
I_{IH} + I_{OZH}	3-State output High current		V_O = 2.7V, V_I = V_{IL} or 3.0V[10]		5.0	10	µA
I_{IL} + I_{OZL}	3-State output Low current		V_O = 0.5V, V_I = V_{IL} or 3.0V[10]		-5.0	-10	µA
I_O	Output current[4]		V_O = 2.5V, V_I = GND or V_{CC}	-50	-80	-180	mA
I_{CCH}	Quiescent supply current		Outputs High, V_I = GND or V_{CC}		50	250	µA
I_{CCL}			Outputs Low, V_I = GND or V_{CC}		20	30	mA
I_{CCZ}			Outputs 3-State, V_I = GND or V_{CC}		50	250	µA
ΔI_{CC}	Additional supply current per input pin[5]		One input at 3.4V, other inputs at V_{CC} or GND, V_{CC} = 5.5V		0.3	1.5	mA
I_{OFF}	Power OFF leakage current		T_{amb} = 25°C Only V_{CC} = 0.0V; V_I or $V_O \leq$ 4.5V	-100	0.5	100	µA
I_{CEX}	Output HIGH leakage current		V_{CC} = 5.5V; V_O = 5.5V			50	µA

AC ELECTRICAL CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	150			150[9]		ns
t_{PLH} t_{PHL}	Propagation delay CPBA to An, CPA to An	Waveform 1	2.0 2.5	5.1 5.7	6.6 7.2	2.0 2.5	7.5 8.2	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	Waveform 3 Waveform 4	1.0 2.2	3.3 4.7	4.8 6.2	0.8 2.2	5.8 7.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	Waveform 3 Waveform 4	2.0 1.5	6.1 5.6	7.6 7.1	2.0 1.5	8.1 7.6	ns ns

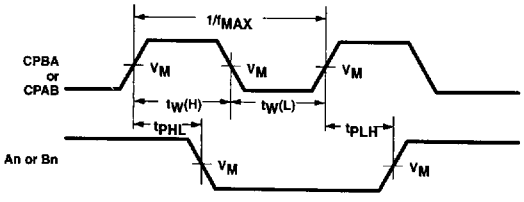
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	WAVEFORM,	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -55°C to +125°C, V_{CC} = +5.0V ± 0.5V		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time An to CPAB or Bn to CPBA	Waveform 2	4.5 3.5	3.1 1.9		4.5 3.5		ns ns
$t_h(H)^7$ $t_h(L)^7$	Hold time An to CPAB or Bn to CPBA	Waveform 2	0.0 0.0	-1.5 -2.8		0.0 0.0		ns ns
$t_x(H)$ $t_s(L)$	Setup time $\overline{CEAB}$ to CPAB, $\overline{CEBA}$ to CPBA	Waveform 2	4.0 3.0	2.6 1.8		4.0 3.0		ns ns
$t_h(H)^7$ $t_h(L)^7$	Hold time $\overline{CEAB}$ to CPAB, $\overline{CEBA}$ to CPBA	Waveform 2	0.0 0.0	-1.5 -1.5		0.0 0.0		ns ns
$t_w(H)^8$ $t_w(L)^8$	Pulse width, High or Low CPAB or CPBA	Waveform 1	3.0 3.5	1.9 2.6		3.0 3.5		ns ns

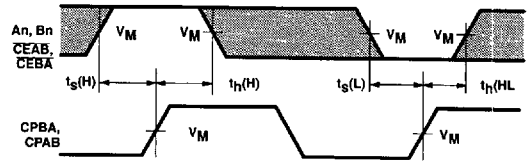
NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
5. This is the increase in supply current for each input at 3.4V.
6. Input leakage on transceiver data pins also includes I_{OZH} or I_{OZL} current from the output circuitry.
7. T_{set} and T_{hold} limits that are less than 3.0ns are guaranteed, but are only tested to a 3.0ns limit due to tester limitations.
8. T_w limits that are less than 6.0ns are guaranteed, but are only tested to a 6.0ns limit due to tester limitations
9. f_{MAX} is guaranteed but not tested over temperature.
10. To accommodate tester limitations, I_{OZ} tests are tested with V_{IH} = 3.0V, but 2.0V V_{IH} is guaranteed.

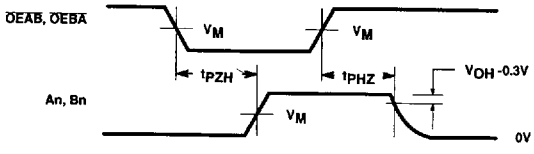
AC WAVEFORMS



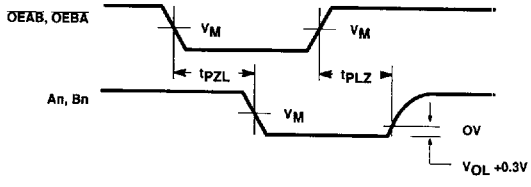
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times



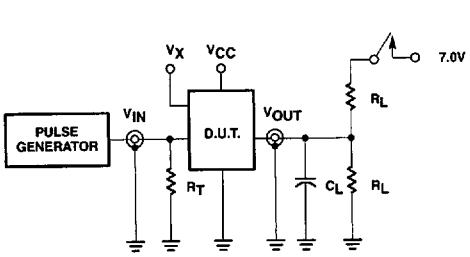
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



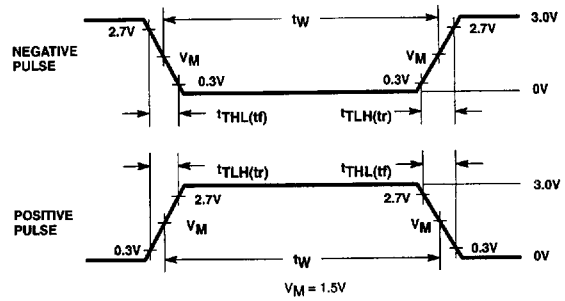
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE REQUIREMENTS					
Family	**Amplitude**	**Rep. Rate**	t_W	t_R	t_F
54ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.