

FAN73933

Half-Bridge Gate Drive IC

Features

- Floating Channel for Bootstrap Operation to +600V
- Typically 2.5A/2.5A Sourcing/Sinking Current Driving Capability
- Extended Allowable Negative V_S Swing to -9.8V for Signal Propagation at $V_{BS}=15V$
- Output in Phase with Input Signal
- 3.3V and 5V Input Logic Compatible
- Matched Propagation Delay for Both Channels
- Built-in UVLO Functions for Both Channels
- Built-in Common-Mode dv/dt Noise Cancelling Circuit
- Programmable Dead-Time Control Function
- Internal 220ns Minimum Dead Time at $R_{DT}=0\Omega$

Applications

- High-Speed Power MOSFET and IGBT Gate Driver
- Induction Heating
- High-Power DC-DC Converter
- Synchronous Step-Down Converter
- Motor Drive Inverter

Description

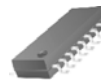
The FAN73933 is a half-bridge, gate-drive IC with programmable dead-time control functions that can drive high-speed MOSFETs and IGBTs operating up to +600V. It has a buffered output stage with all NMOS transistors designed for high-pulse-current driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level-shift circuit offers high-side gate driver operation up to $V_S=-9.8V$ (typical) for $V_{BS}=15V$.

The UVLO circuit prevents malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

The high-current and low-output voltage drop feature makes this device suitable for diverse half- and full-bridge inverters; motor drive inverters, switching mode power supplies, induction heating, and high-power DC-DC converter applications.

14-SOP



Ordering Information

Part Number	Package	Operating Temperature Range	Eco Status	Packing Method
FAN73933M	14-Lead, Small Outline Integrated Circuit (SOIC), Non-JEDEC, .150 Inch Narrow Body, 225SOP	-40°C to +125°C	RoHS	Tube
FAN73933MX				Tape & Reel

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For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Typical Application Diagrams

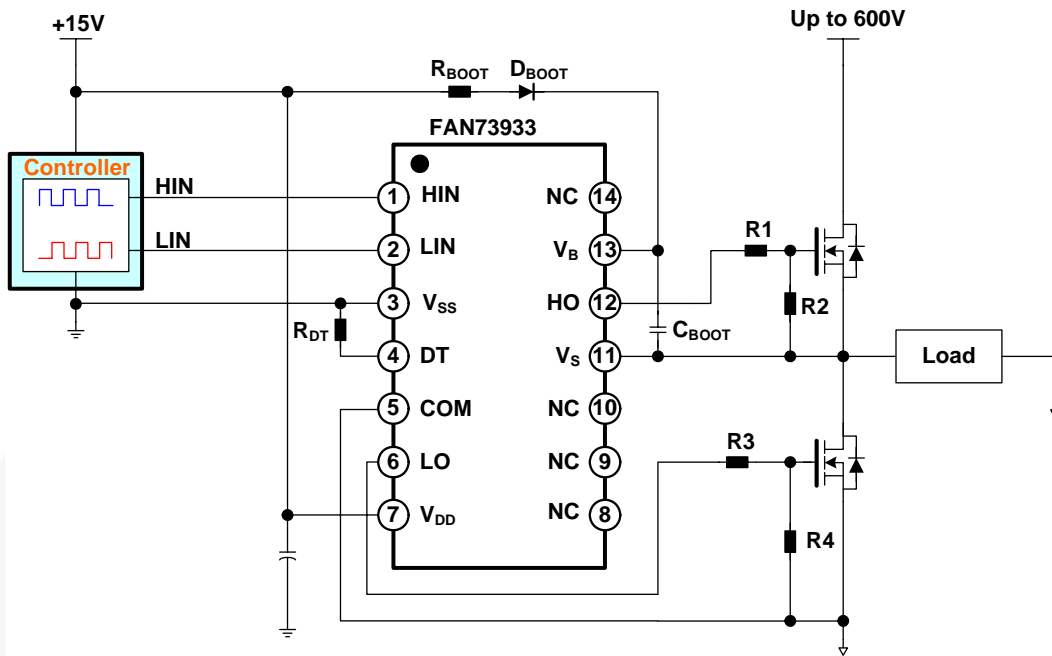


Figure 1. Typical Application Circuit

Internal Block Diagram

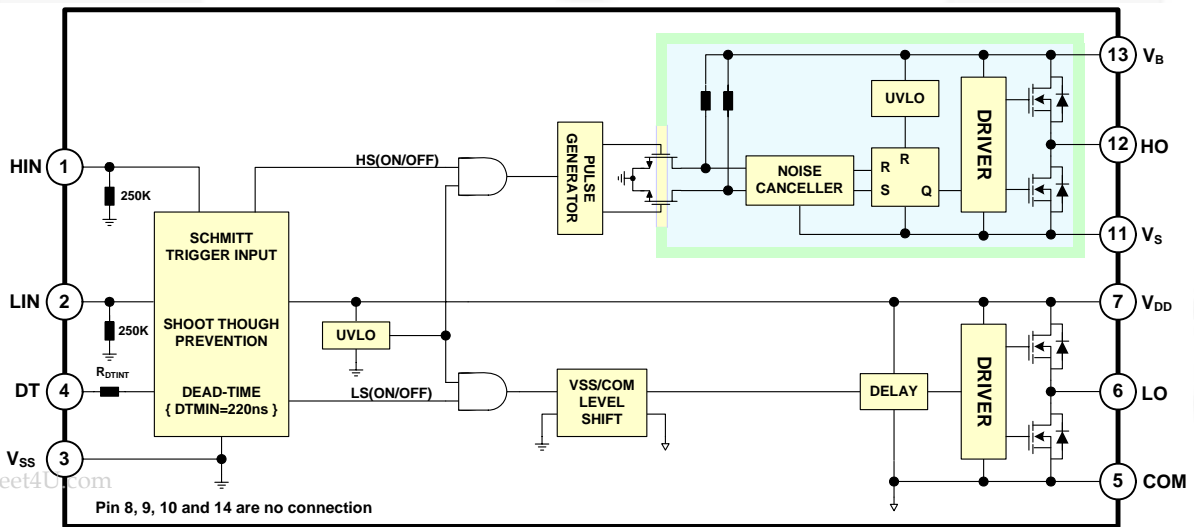


Figure 2. Functional Block Diagram

Pin Configuration

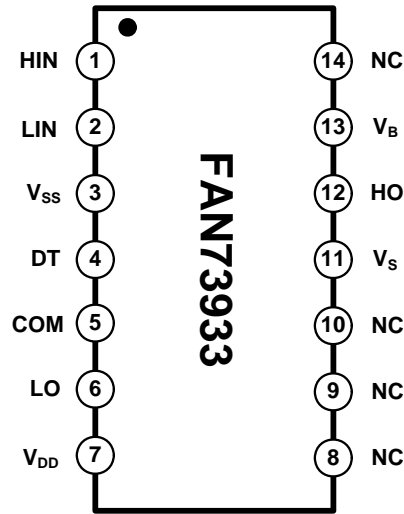


Figure 3. Pin Configurations (Top View)

Pin Definitions

Pin #	Name	Description
1	HIN	Logic Input for High-Side Gate Driver Output
2	LIN	Logic Input for Low-Side Gate Driver Output
3	V _{SS}	Logic Ground
4	DT	Dead-Time Control with External Resistor (Referenced to V _{SS})
5	COM	Ground
6	LO	Low-Side Driver Return
7	V _{DD}	Supply Voltage
8	NC	No Connection
9	NC	No Connection
10	NC	No Connection
11	V _S	High-Voltage Floating Supply Return
12	HO	High-Side Driver Output
13	V _B	High-Side Floating Supply
14	NC	No Connection

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A=25^{\circ}\text{C}$ unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
V_B	High-Side Floating Supply Voltage	-0.3	625.0	V
V_S	High-Side Floating Offset Voltage	$V_B-25.0$	$V_B+0.3$	V
V_{HO}	High-Side Floating Output Voltage	$V_S-0.3$	$V_B+0.3$	V
V_{LO}	Low-Side Output Voltage	-0.3	$V_{DD}+0.3$	V
V_{DD}	Low-Side and Logic Fixed Supply Voltage	-0.3	25.0	V
V_{IN}	Logic Input Voltage (HIN and LIN)	-0.3	$V_{DD}+0.3$	V
DT	Programmable Dead-Time Pin Voltage	-0.3	$V_{DD}+0.3$	V
V_{SS}	Logic Ground	$V_{DD}-25$	$V_{DD}+0.3$	V
dV_S/dt	Allowable Offset Voltage Slew Rate		± 50	V/ns
P_D	Power Dissipation ^(1, 2, 3)		1	W
θ_{JA}	Thermal Resistance		110	$^{\circ}\text{C/W}$
T_J	Junction Temperature		+150	$^{\circ}\text{C}$
T_{STG}	Storage Temperature	-55	+150	$^{\circ}\text{C}$

Notes:

- 1 Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
- 2 Refer to the following standards:
JESD51-2: Integral circuits thermal test method environmental conditions - natural convection, and
JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages.
- 3 Do not exceed maximum P_D under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_B	High-Side Floating Supply Voltage	V_S+10	V_S+20	V
V_S	High-Side Floating Supply Offset Voltage	$6-V_{DD}$	600	V
V_{HO}	High-Side Output Voltage	V_S	V_B	V
V_{DD}	Low-Side and Logic Fixed Supply Voltage	10	20	V
V_{LO}	Low-Side Output Voltage	COM	V_{DD}	V
V_{IN}	Logic Input Voltage (HIN and LIN)	V_{SS}	V_{DD}	V
DT	Programmable Dead-Time Pin Voltage	V_{SS}	V_{DD}	V
V_{SS}	Logic Ground	-5	+5	V
T_A	Operating Ambient Temperature	-40	+125	$^{\circ}\text{C}$

Electrical Characteristics

$V_{BIAS}(V_{DD}, V_{BS})=15.0V$, $V_{SS}=COM=0V$, $DT=V_{SS}$ and $T_A = 25^\circ C$, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: HIN and LIN. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
POWER SUPPLY SECTION						
I_{QDD}	Quiescent V_{DD} Supply Current	$V_{IN}=0V$ or $5V$		0.9	1.5	mA
I_{QBS}	Quiescent V_{BS} Supply Current	$V_{IN}=0V$ or $5V$		50	100	μA
I_{PDD}	Operating V_{DD} Supply Current	$f_{IN}=20KHz$, No Load		1.3	1.9	mA
I_{PBS}	Operating V_{BS} Supply Current	$C_L=1nF$, $f_{IN}=20KHz$, rms		450	800	μA
I_{LK}	Offset Supply Leakage Current	$V_B=V_S=600V$			10	μA
BOOTSTRAPPED SUPPLY SECTION						
V_{DDUV+} V_{BSUV+}	V_{DD} and V_{BS} Supply Under-Voltage Positive-Going Threshold Voltage	$V_{IN}=0V$, $V_{DD}=V_{BS}=Sweep$	8.0	9.0	10	V
V_{DDUV-} V_{BSUV-}	V_{DD} and V_{BS} Supply Under-Voltage Negative-Going Threshold Voltage	$V_{IN}=0V$, $V_{DD}=V_{BS}=Sweep$	7.4	8.4	9.4	V
V_{DDUVH-} V_{BSUVH}	V_{DD} and V_{BS} Supply Under-Voltage Lockout Hysteresis Voltage	$V_{IN}=0V$, $V_{DD}=V_{BS}=Sweep$		0.6		V
INPUT LOGIC SECTION						
V_{IH}	Logic "1" Input Voltage for HO & Logic "0" for LO		2.5			V
V_{IL}	Logic "0" Input Voltage for HO & Logic "1" for LO				0.8	V
I_{IN+}	Logic Input High Bias Current	$V_{IN}=5V$		20	50	μA
I_{IN-}	Logic Input Low Bias Current	$V_{IN}=0V$			2	μA
R_{IN}	Logic Input Pull-Down Resistance		100	250		$K\Omega$
GATE DRIVER OUTPUT SECTION						
V_{OH}	High-Level Output Voltage ($V_{BIAS} - V_O$)	No Load			1.5	V
V_{OL}	Low-Level Output Voltage	No Load			100	mV
I_{O+}	Output High, Short-Circuit Pulsed Current ⁽⁴⁾	$V_{HO}=0V$, $V_{IN}=5V$, $PW \leq 10\mu s$	2.0	2.5		A
I_{O-}	Output Low, Short-Circuit Pulsed Current ⁽⁴⁾	$V_{HO}=15V$, $V_{IN}=0V$, $PW \leq 10\mu s$	2.0	2.5		A
V_S	Allowable Negative V_S Pin Voltage for IN Signal Propagation to HO			-9.8	-7.0	V

Note:

4. These parameters guaranteed by design.

Dynamic Electrical Characteristics

$V_{BIAS}(V_{DD}, V_{BS})=15.0V$, $V_{SS}=COM=0V$, $C_L=1000pF$, $DT=V_{SS}$ and $T_A=25^\circ C$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Turn-On Propagation Delay Time ⁽⁵⁾	$V_S=0V$, $R_{DT}=0\Omega$		160	230	ns
t_{OFF}	Turn-Off Propagation Delay Time	$V_S=0V$		160	230	ns
Mt_{ON}	Delay Matching, HO & LO Turn-On			0	50	ns
Mt_{OFF}	Delay Matching, HO & LO Turn-Off			0	50	ns
t_R	Turn-On Rise Time	$V_S=0V$		40	60	ns
t_F	Turn-Off Fall Time	$V_S=0V$		20	35	ns
DT	Dead Time: LO Turn-Off to HO Turn-On & HO Turn-Off to LO Turn-On	$R_{DT}=0\Omega$	170	220	270	ns
		$R_{DT}=300K\Omega$	400	500	600	ns
MDT	Dead-Time Matching= $ DT_{LO-HO} - DT_{HO-LO} $	$R_{DT}=0\Omega$		0	50	ns
		$R_{DT}=300K\Omega$		0	100	ns

Note:

5 The turn-on propagation delay does not include dead time.

Typical Characteristics

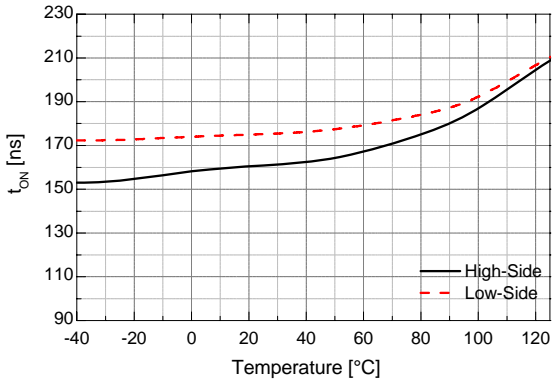


Figure 4. Turn-On Propagation Delay vs. Temperature

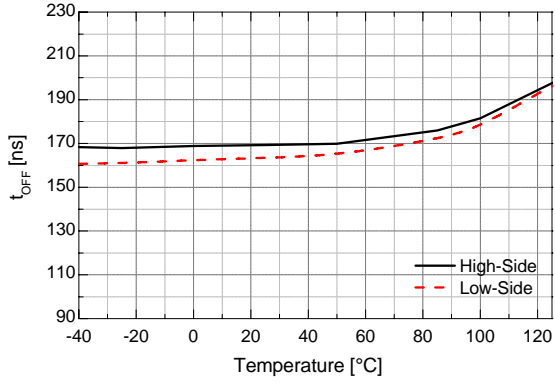


Figure 5. Turn-Off Propagation Delay vs. Temperature

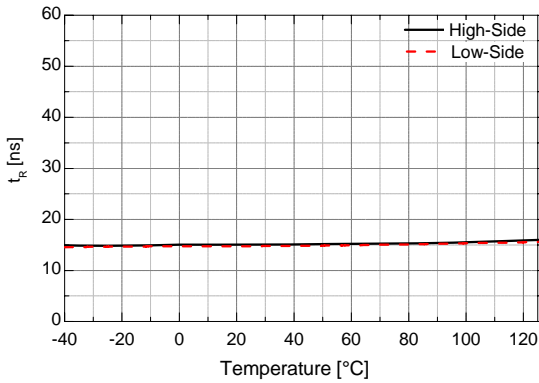


Figure 6. Turn-On Rise Time vs. Temperature

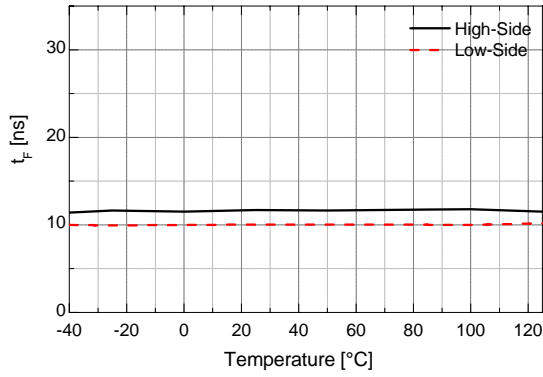


Figure 7. Turn-Off Fall Time vs. Temperature

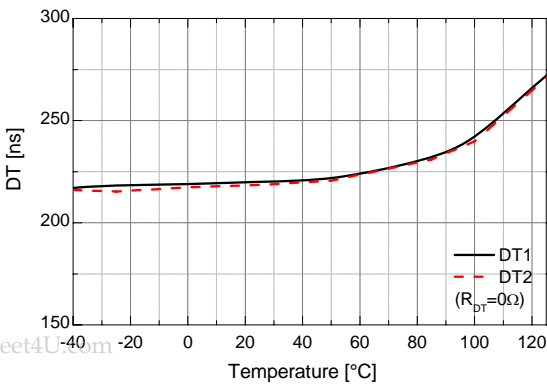


Figure 8. Dead Time ($R_{DT}=0\Omega$) vs. Temperature

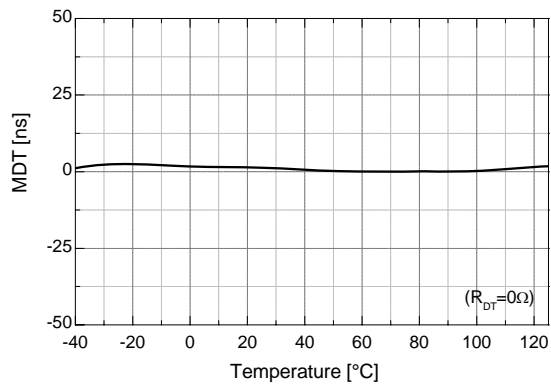


Figure 9. Dead Time Matching ($R_{DT}=0\Omega$) vs. Temperature

Typical Characteristics (Continued)

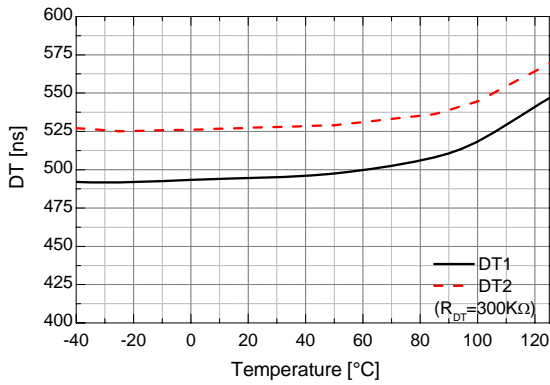


Figure 10. Dead Time ($R_{DT}=300K\Omega$) vs. Temperature

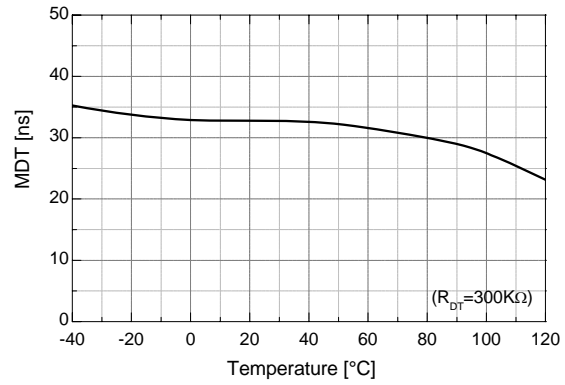


Figure 11. Dead Time Matching ($R_{DT}=300K\Omega$) vs. Temperature

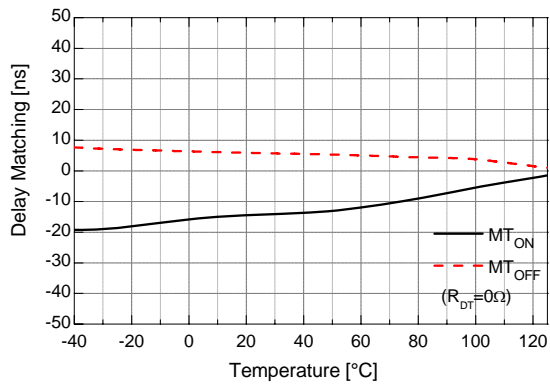


Figure 12. Delay Matching vs. Temperature

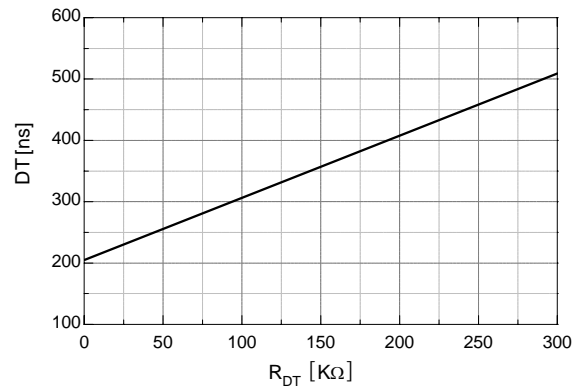


Figure 13. Dead Time vs. R_{DT}

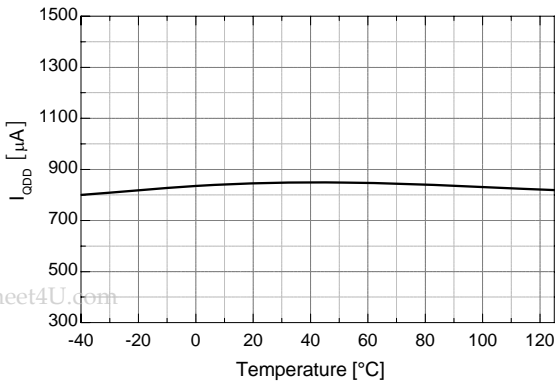


Figure 14. Quiescent V_{DD} Supply Current vs. Temperature

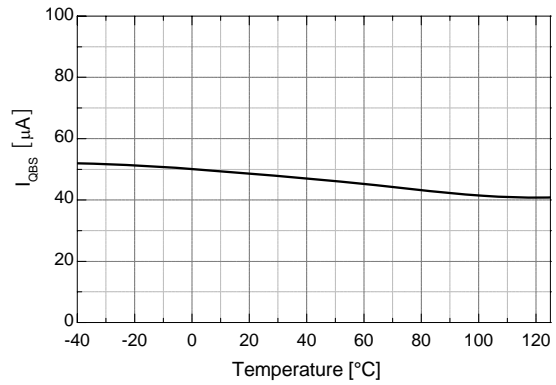


Figure 15. Quiescent V_{BS} Supply Current vs. Temperature

Typical Characteristics (Continued)

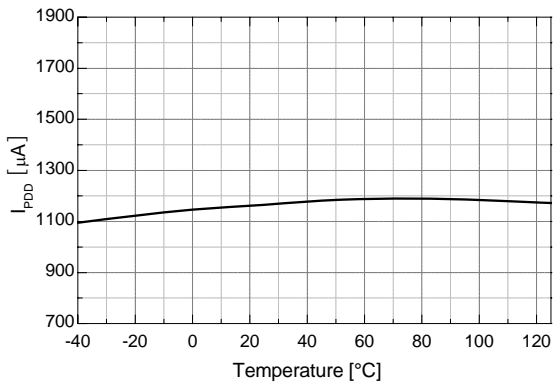


Figure 16. Operating V_{CC} Supply Current vs. Temperature

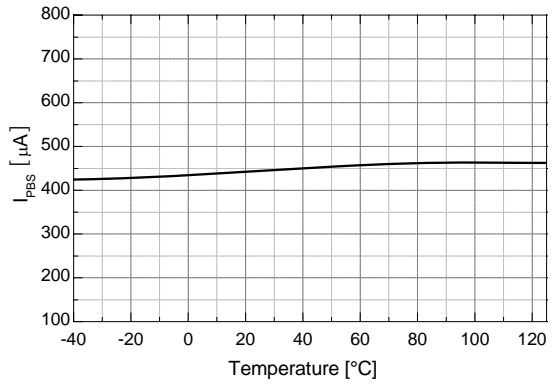


Figure 17. Operating V_{BS} Supply Current vs. Temperature

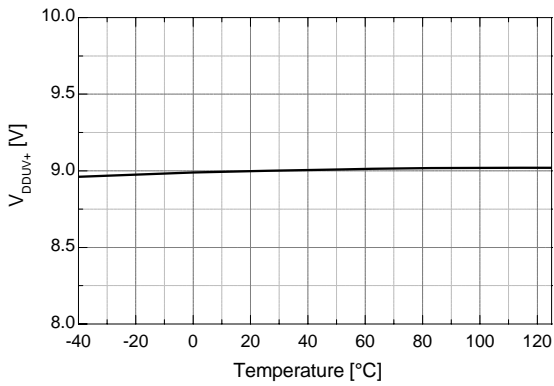


Figure 18. V_{DD} UVLO+ vs. Temperature

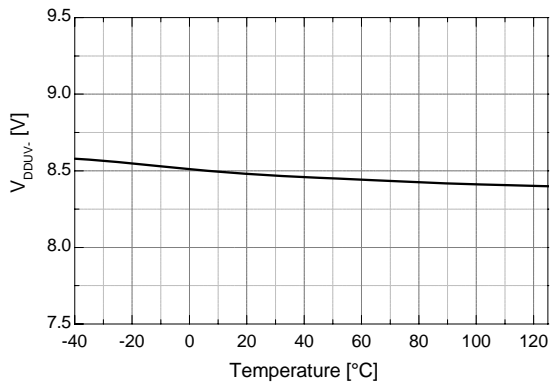


Figure 19. V_{DD} UVLO- vs. Temperature

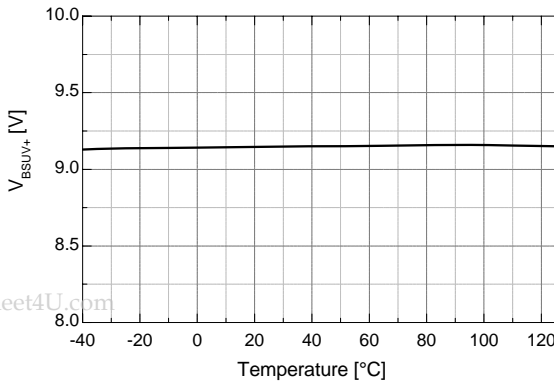


Figure 20. V_{BS} UVLO+ vs. Temperature

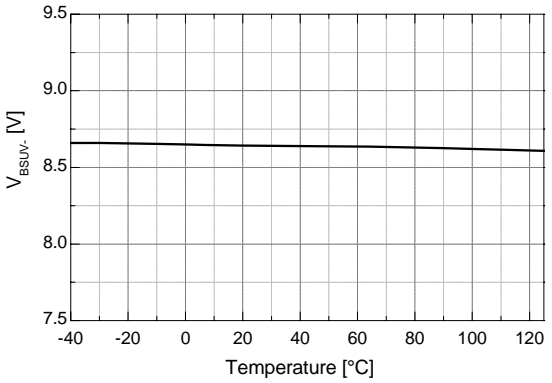


Figure 21. V_{BS} UVLO- vs. Temperature

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Typical Characteristics (Continued)

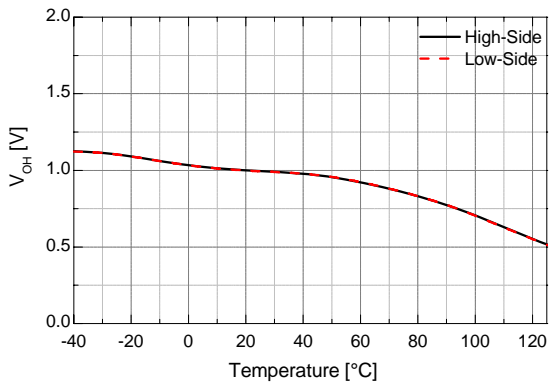


Figure 22. High-Level Output Voltage vs. Temperature

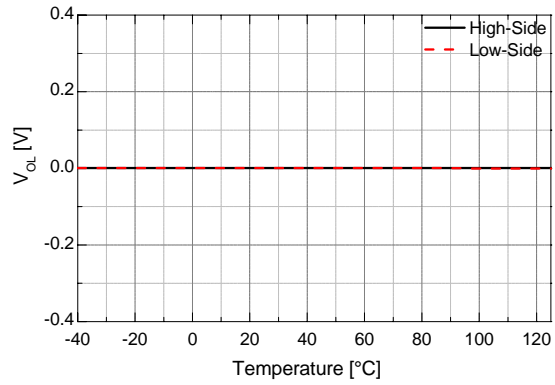


Figure 23. Low-Level Output Voltage vs. Temperature

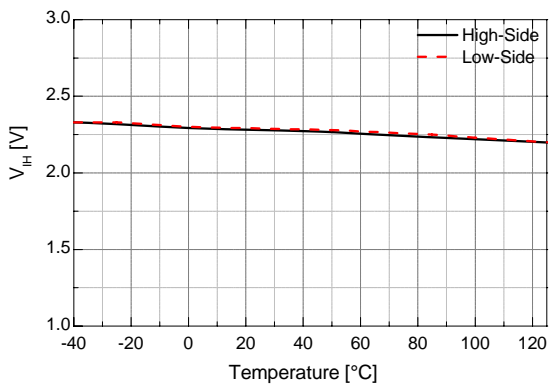


Figure 24. Logic High Input Voltage vs. Temperature

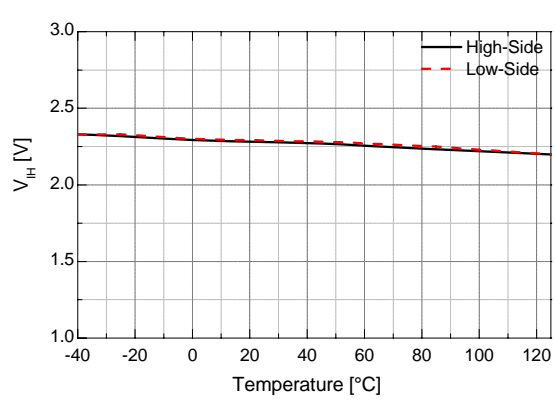


Figure 25. Logic Low Input Voltage vs. Temperature

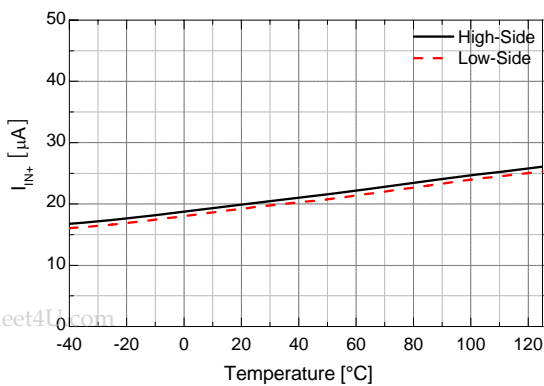


Figure 26. Logic Input High Bias Current vs. Temperature

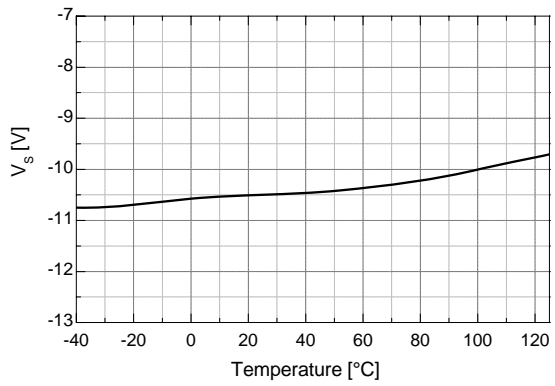


Figure 27. Allowable Negative V_S Voltage vs. Temperature

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Typical Characteristics (Continued)

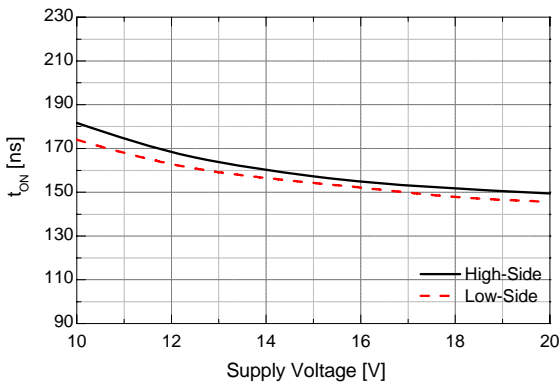


Figure 28. Turn-On Propagation Delay vs. Supply Voltage

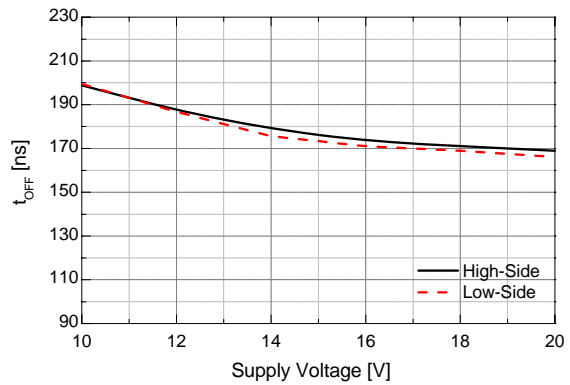


Figure 29. Turn-Off Propagation Delay vs. Supply Voltage

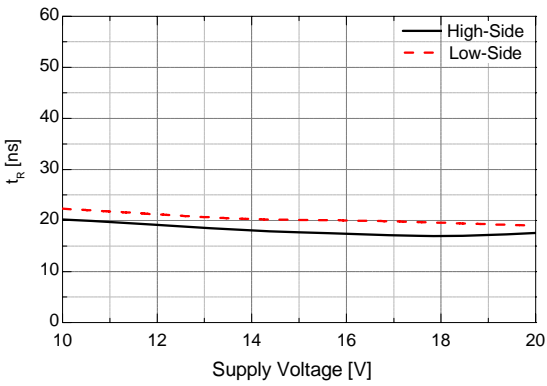


Figure 30. Turn-On Rise Time vs. Supply Voltage

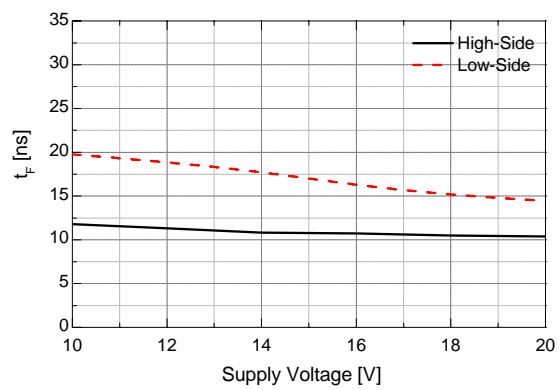


Figure 31. Turn-Off Fall Time vs. Supply Voltage

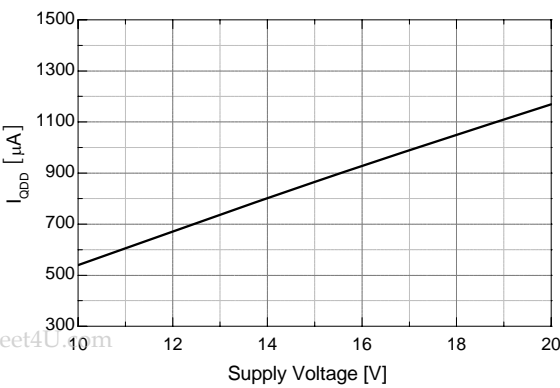


Figure 32. Quiescent V_{DD} Supply Current vs. Supply Voltage

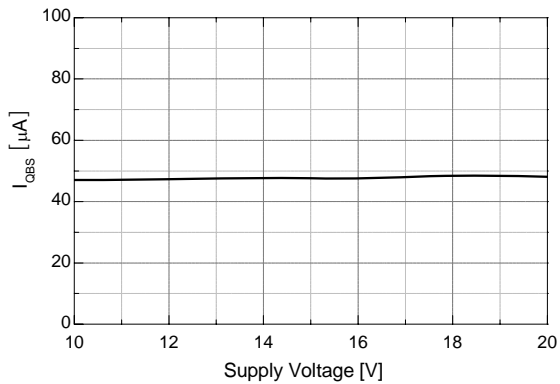


Figure 33. Quiescent V_{BS} Supply Current vs. Supply Voltage

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Typical Characteristics (Continued)

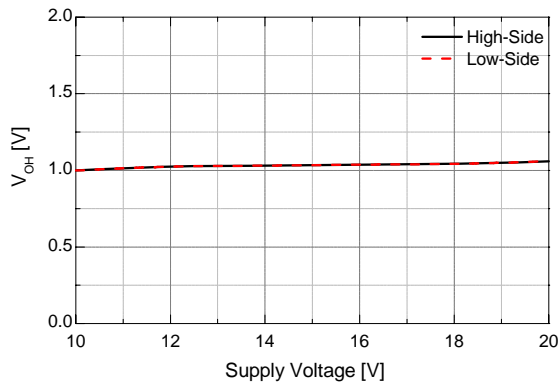


Figure 34. High-Level Output Voltage vs. Supply Voltage

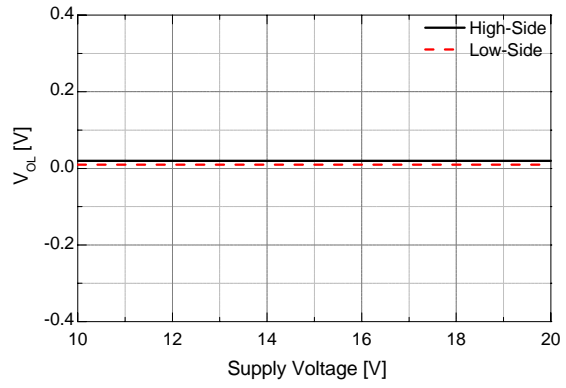


Figure 35. Low-Level Output Voltage vs. Supply Voltage

Switching Time Definitions

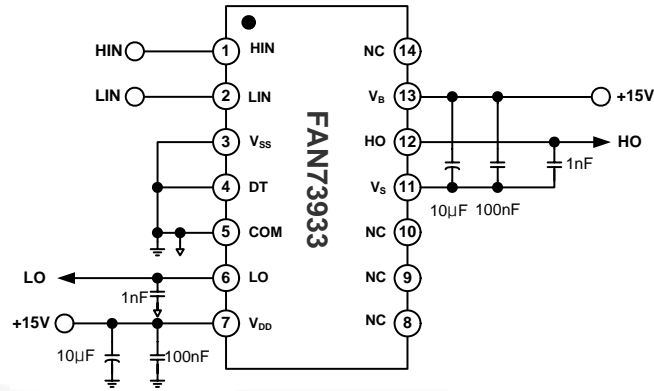


Figure 36. Switching Time Test Circuit

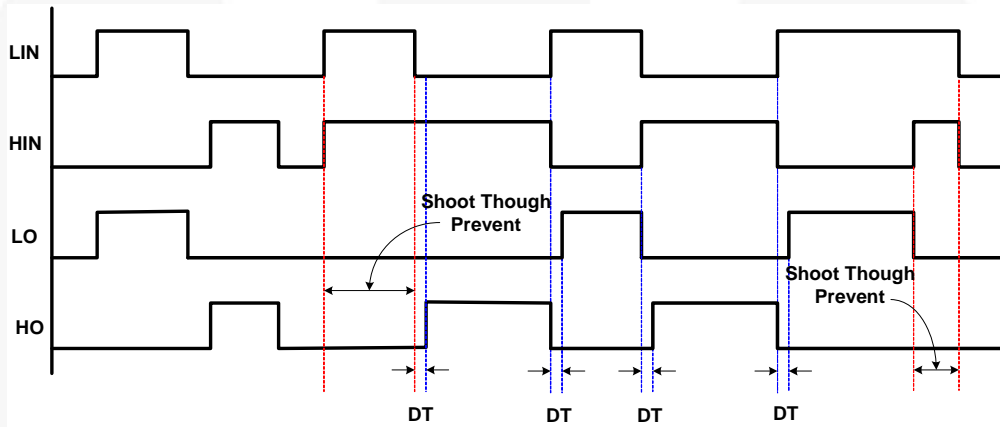


Figure 37. Input/Output Timing Diagram

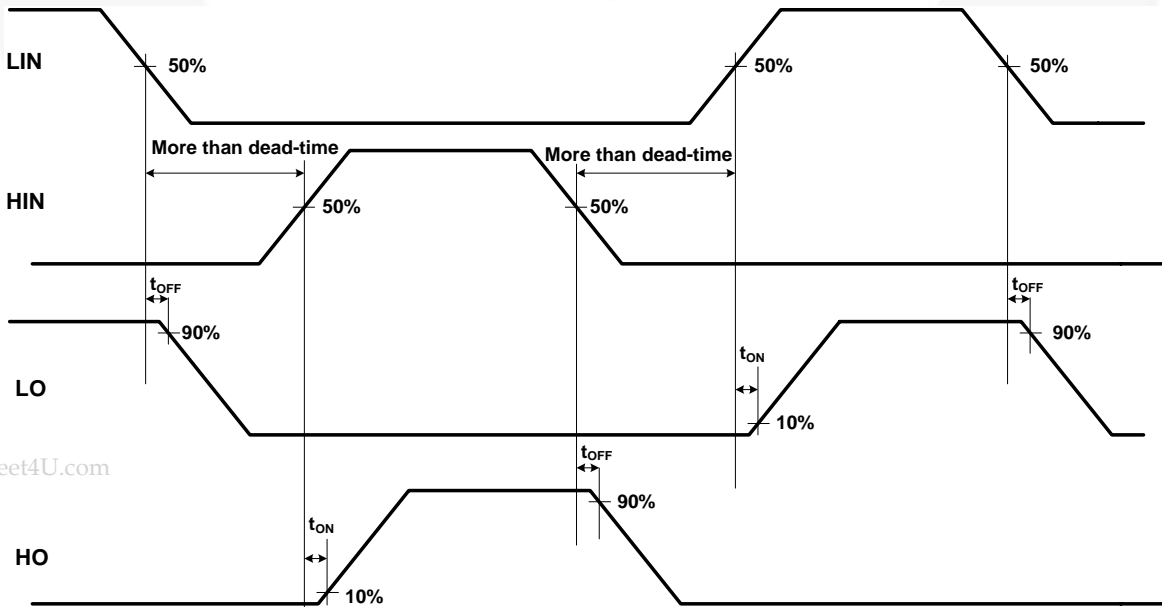


Figure 38. Switching Time Waveform Definitions

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Application Information

Negative V_S Transient

The bootstrap circuit has the advantage of being simple and low cost, but has some limitations. The biggest difficulty with this circuit is the negative voltage present at the emitter of the high-side switching device when the high-side switch is turned off in half-bridge applications.

If the high-side switch, Q1, turns-off while the load current is flowing to an inductive load; a current commutation occurs from high-side switch, Q1, to the diode, D2, in parallel with the low-side switch of the same inverter leg. Then the negative voltage present at the emitter of the high-side switching device, just before the freewheeling diode, D2, starts clamping, causes load current to suddenly flow to the low-side freewheeling diode, D2, as shown in Figure 39.

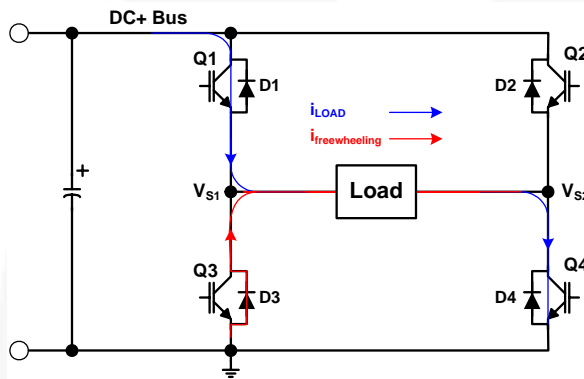


Figure 39. Half-Bridge Application Circuits

This negative voltage can be trouble for the gate driver's output stage. There is the possibility to develop an over-voltage condition of the bootstrap capacitor, input signal missing, and latch-up problems because it directly affects the source V_S pin of the gate driver, as shown in Figure 40. This undershoot voltage is called "negative V_S transient".

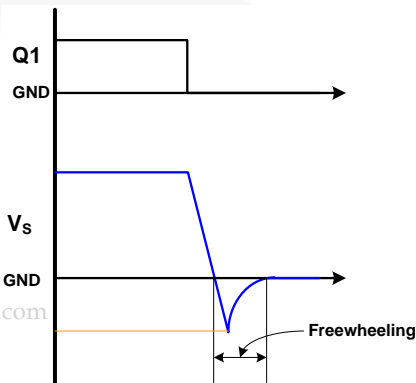


Figure 40. V_S Waveforms During Q1 Turn-Off

Figure 41. and Figure 42. show the commutation of the load current between the high-side switch, Q1, and low-side freewheeling diode, D3, in same inverter leg. The parasitic inductances in the inverter circuit from the die wire bonding to the PCB tracks are jumped together in L_C and L_E for each IGBT. When the high-side switch, Q1, and low-side switch, Q4, are turned on; the V_{S1} node is below DC+ voltage by the voltage drops associated with the power switch and the parasitic inductances of the circuit due to load current is flows from Q1 and Q4, as shown in Figure 41. When the high-side switch, Q1, is turned off and Q4 remains turned on, the load current to flows the low-side freewheeling diode, D3, due to the inductive load connected to V_{S1} as shown in Figure 42. The current flows from ground (which is connected to the COM pin of the gate driver) to the load and the negative voltage present at the emitter of the high-side switching device.

In this case, the COM pin of the gate driver is at a higher potential than the V_S pin due to the voltage drops associated with freewheeling diode, D3, and parasitic elements, L_{C3} and L_{E3} .

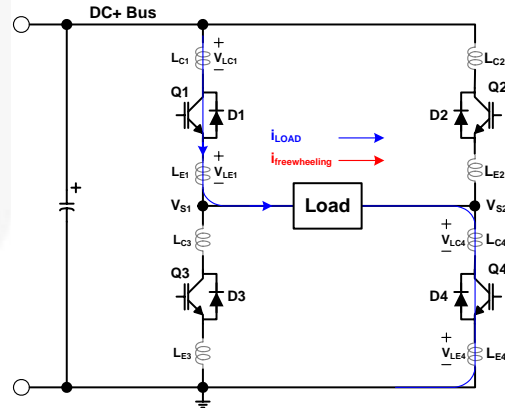


Figure 41. Q1 and Q4 Turn-On

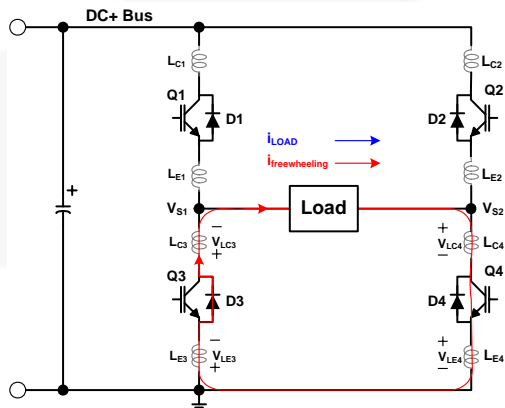


Figure 42. Q1 Turn-Off and D3 Conducting

The FAN73933 has a negative V_S transient performance curve, as shown in Figure 43.

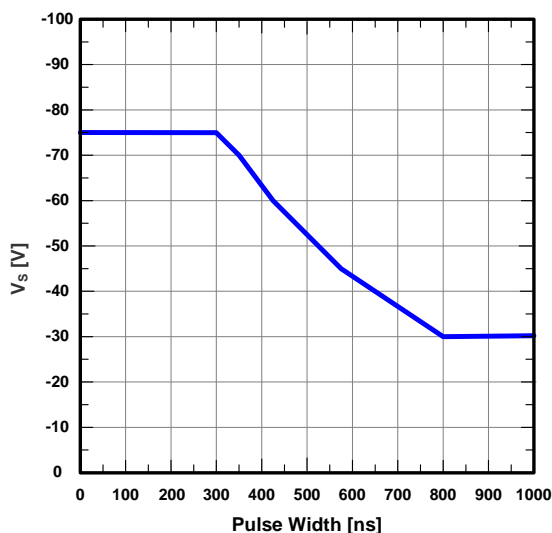


Figure 43. Negative V_S Transient Characteristic

Even though the FAN73933 has been shown able to handle these negative V_S transient conditions, it is strongly recommended that the circuit designer limit the negative V_S transient as much as possible by careful PCB layout to minimize the value of parasitic elements and component use. The amplitude of negative V_S voltage is proportional to the parasitic inductances and the turn-off speed, di/dt , of the switching device.

General Guidelines

Printed Circuit Board Layout

The layout recommended for minimized parasitic elements is as follows:

- Direct tracks between switches with no loops or deviation.
- Avoid interconnect links. These can add significant inductance.
- Reduce the effect of lead-inductance by lowering package height above the PCB.
- Consider co-locating both power switches to reduce track length.
- To minimize noise coupling, the ground plane should not be placed under or near the high-voltage floating side.
- To reduce the EM coupling and improve the power switch turn-on/off performance, the gate drive loops must be reduced as much as possible.

Placement of Components

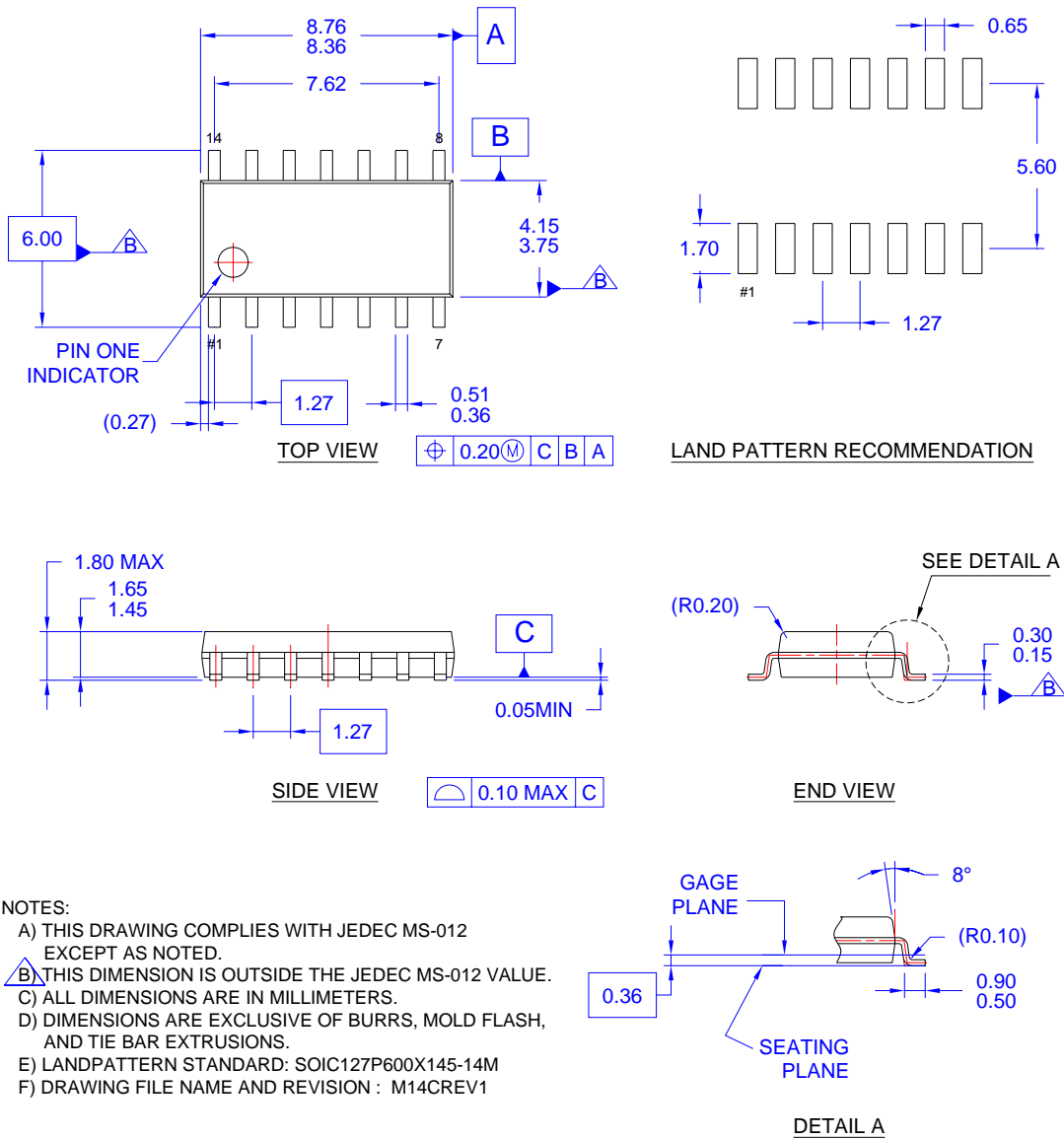
The recommended selection of component is as follows:

- Place a bypass capacitor between the V_{DD} and V_{SS} pins. A ceramic $1\mu\text{F}$ capacitor is suitable for most applications. This component should be placed as close as possible to the pins to reduce parasitic elements.
- The bypass capacitor from V_{CC} to COM supports both the low-side driver and bootstrap capacitor recharge. A value at least ten times higher than the bootstrap capacitor is recommended.
- The bootstrap resistor, R_{BOOT} , must be considered in sizing the bootstrap resistance and the current developed during initial bootstrap charge. If the resistor is needed in series with the bootstrap diode, verify that V_B does not fall below COM (ground). Recommended use is typically $5 \sim 10\Omega$, which increases the V_{BS} time constant. If the voltage drop of the bootstrap resistor and diode is too high or the circuit topology does not allow a sufficient charging time, a fast recovery or ultra-fast recovery diode can be used.
- The bootstrap capacitor, C_{BOOT} , uses a low-ESR capacitor, such as a ceramic capacitor.

It is strongly recommended that the placement of components is as follows:

- Place components tied to the floating voltage pins (V_B and V_S) near the respective high-voltage portions of the device and the FAN73933. NC (not connected) pins in this package maximize the distance between the high-voltage and low-voltage pins (see Figure 3).
- Place and route for bypass capacitors and gate resistors as close as possible to gate drive IC.
- Locate the bootstrap diode, D_{BOOT} , as close as possible to bootstrap capacitor, C_{BOOT} .
- The bootstrap diode must use a lower forward voltage drop and minimal switching time as soon as possible for fast recovery or ultra-fast diode.

Physical Dimensions



NOTES:

- A) THIS DRAWING COMPLIES WITH JEDEC MS-012 EXCEPT AS NOTED.
- B) THIS DIMENSION IS OUTSIDE THE JEDEC MS-012 VALUE.
- C) ALL DIMENSIONS ARE IN MILLIMETERS.
- D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- E) LANDPATTERN STANDARD: SOIC127P600X145-14M
- F) DRAWING FILE NAME AND REVISION : M14CREV1

Figure 44. 14-Lead, Small Outline Integrated Circuit (SOIC), Non-JEDEC, .150 Inch Narrow Body, 225SOP

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