

# SANYO Semiconductors

# DATA SHEET

An ON Semiconductor Company

LC749403BG-

# Silicon gate LCD Picture Quality Improvement IC

#### Overview

LC749403BG is a IC which enables higher picture quality in LCD products by improving the signals outputed to the LCD panel. In addition to the function to improve the picture quality of the color equation and the brightness correction, smooth picture quality is realized by converting One Seg video from 15fps to 30fps using flame interpolation technique.

**CMOSIC** 

It supports up to WVGA resolution. \*

#### **Features**

- (1) Digital Input/Output
- Supports digital video input: YCbCr/YPbPr 24bit,16bit (4: 2: 2) signals or ITU-R BT.656 (8bit) input
- Digital RGB 24 bit signal input
- Digital RGB 18bit/24bit signal output
- Digital YCbCr 16bit/24bit signal output
- (2) Picture Quality Improvement Function
- Y signal picture quality improvement: brightness adjustment, contour correction, CDEX (Color Depth Expander),
- C signal picture quality improvement: color exciter, skin color correction, color and hue adjustment
- RGB signal picture quality improvement: brightness, contrast, white balance, black balance, gamma correction (3) Panel Interface
- Embedded timing controller for panel driver
- Automtic timing signal generation for panel protection
- PWM for backlight control (video adaptation low power consumtion processing)
- (4) Frame interpolation (×2) for One-Seg broadcast
- Double-speed (×2) mode (15fps ⇒ 30fps)
   Intermediate image is predicted from the previous and next image.
- \*: Video input of the LC749403BG meets the following conditions:
  - (1) horizontal resolution is under 880 dots, and (2) vertical resolution is under 480 lines.
    - Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.
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# **LSI Specifications**

• Power supply voltage (typ)

Core block: 1.2V SDRAM I/F block: 1.8V

I/O block: 1.8V/2.85V/3.3V selectable

• Maximum operating frequency

internal: 36MHz SDRAM I/F block: 80MHz

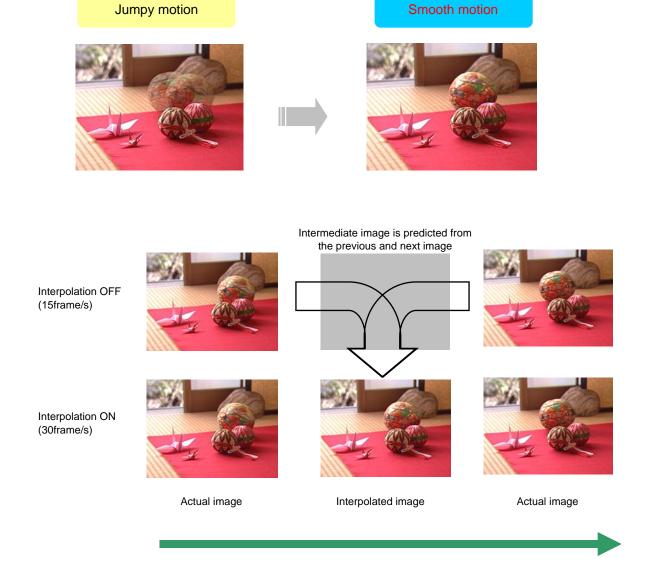
• Package: FBGA144 11mm × 11mm (stacked MCP with SDRAM)

#### **Target Application**

• LCD display devices, One-Seg broadcast receiver (Car-Navigation, One-Seg TV, Portable DVD player, etc)

#### Frame interpolation (×2) example

Smooth image quality is realized by converting One Seg video from 15fps to 30fps using flame interpolation technique



# **CDEX (Color Depth Expander) Example**

This specification may be changed without any notices for product improvement.



# **Specifications**

 $\label{eq:absolute Maximum Ratings} \mbox{ at } \mbox{Ta} = 25^{\circ}\mbox{C, } \mbox{DV}_{SS} = 0\mbox{V, } \mbox{AV}_{SS} \mbox{PLL} = 0\mbox{V, } \mbox{AV}_{SS} \mbox{OSC} = 0\mbox{V, } \mbox{SDV}_{SS} = 0\mbox{V,$ 

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage (I/O)	DV <sub>DD</sub> _IO		-0.3 to +3.96	V
Maximum supply voltage (SDRAM, SDRAMIF I/O, PLL)	DV <sub>DD</sub> SDIO, AV <sub>DD</sub> PLL, SDV <sub>DD</sub> , SDV <sub>DDQ</sub>		-0.3 to +2.6	٧
Maximum supply voltage (core, osc)	DV <sub>DD</sub> CORE AV <sub>DD</sub> OSC		-0.3 to +1.8	V
Digital input voltage	VI		-0.3 to DV <sub>DD</sub> _IO+0.3	V
Digital output voltage	V <sub>O</sub>		-0.3 to DV <sub>DD</sub> _IO+0.3	V
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

# $\label{eq:allowable Operation Ranges} \ \text{at Ta = -40 to +85°C, DV}_{SS} = 0V, \ AV_{SS}\_PLL = 0V, \ AV_{SS}\_OSC = 0V, \ SDV_{SS} = 0V, \ SDV_{SSO} = 0V,$

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Parameter	Symbol	Conditions	min	typ	max	unit
Supply voltage (I/O)	DV <sub>DD</sub> _IO		2.6	2.85	3.6	V
			1.7	1.8	1.95	V
Supply voltage (SDRAMIF I/O)	DV <sub>DD</sub> SDIO		1.7	1.8	1.95	V
Supply voltage (SDRAM, PLL)	$SDV_{DD}$ , $SDV_{DDQ}$ $AV_{DD}$ PLL		1.7	1.8	1.95	V
Supply voltage (core, osc)	DV <sub>DD</sub> CORE AV <sub>DD</sub> OSC		1.14	1.2	1.26	V
Input voltage range	V <sub>IN</sub>		0		DV <sub>DD</sub> _IO	V

 $\begin{aligned} \textbf{DC Characteristics} \text{ at } T_{a} = -40 \text{ to } +85^{\circ}\text{C}, DV_{SS} = 0\text{V}, AV_{SS}\_PLL = 0\text{V}, AV_{SS}\_OSC = 0\text{V}, SDV_{SS} = 0\text{V}, \\ SDV_{SSQ} = 0\text{V}, DV_{DD}\_IO = 1.7 \text{ to } 3.6\text{V}, DV_{DD}\_SDIO = 1.7 \text{ to } 1.95\text{V}, \\ DV_{DD}\_CORE = 1.14 \text{ to } 1.26\text{V}, SDV_{DD} = 1.7 \text{ to } 1.95\text{V}, SDV_{DDQ} = 1.7 \text{ to } 1.95\text{V} \end{aligned}$ 

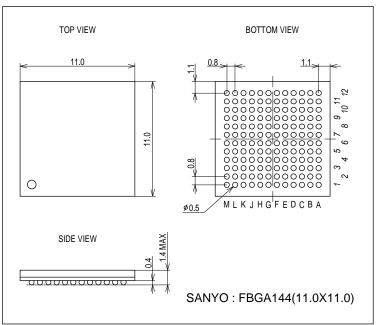
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Parameter	Symbol	Conditions	min	min typ max		unit
Input high-level voltage	V <sub>IH</sub>	CMOS level inputs	0.7DV <sub>DD</sub> _IO			V
смоз		CMOS level schmitt inputs	0.7DV <sub>DD</sub> _IO			V
Input low-level voltage	V <sub>IL</sub>	CMOS level inputs			0.3DV <sub>DD</sub> _IO	V
		CMOS level schmitt inputs			0.3DV <sub>DD</sub> _IO	V
Input high-level current	lн	V <sub>I</sub> =DV <sub>DD</sub> _IO			10	μΑ
		V <sub>I</sub> =DV <sub>DD</sub> IO, with pull-down resistor			100	μΑ
Input low-level current	I <sub>IL</sub>	V <sub>I</sub> =DV <sub>SS</sub>	-10			μΑ
Output high-level voltage	Voн	CMOS voltage: 2.6V to 3.6V, 1.7V to 1.9V  I/O type D: I <sub>OH</sub> = -1mA  I/O type E: I <sub>OH</sub> = -1mA (2mA mode)  I <sub>OH</sub> = -2mA (4mA mode)  I/O type F: I <sub>OH</sub> = -2mA (4mA mode)  I/O type G: I <sub>OH</sub> = -2mA  I/O type H: I <sub>OH</sub> = -1mA (2mA mode)	DV <sub>DD</sub> _IO-0.4			V
Output low-level voltage	V <sub>OL</sub>	I <sub>OH</sub> = -2mA (4mA mode)			0.4	V
Output leakage current	loz	In high-impedance output mode			3	μА
Pull-down resistance	R <sub>DN</sub>	condition: typ  Ta = 25°C  DV <sub>DD</sub> _IO = 2.85V  DV <sub>DD</sub> _CORE = 1.2V		98		kΩ
		condition: typ  Ta = 25°C  DV <sub>DD</sub> _IO = 1.8V  DV <sub>DD</sub> _CORE = 1.2V		69		kΩ
Operating current drain	IDDOP	condition: typ $Ta = 25^{\circ}C$ $DV_{DD} = 2.85V$ $DV_{DD} = 1.2V$ $QVGA, tck = 6.6MHz = 10step$		25		mA
		condition: typ  Ta = 25°C  DV <sub>DD</sub> _IO = 2.85V  DV <sub>DD</sub> _CORE = 1.2V  WVGA, tck = 34.24MHz 10step		112		mA
Static current drain *1	IDDST	condition: typ  Ta = 25°C  DV <sub>DD</sub> _IO = 2.85V  DV <sub>DD</sub> _CORE = 1.2V  Output open,  V <sub>I</sub> = DV <sub>SS</sub> or DV <sub>DD</sub> _IO		35		μΑ

<sup>\*1:</sup> Certain input pins have build-in pull-down resistors. Thus there are cases where, due to the circuit sturucture, the static current drain can not beguranteed.

# **Package Dimensions**

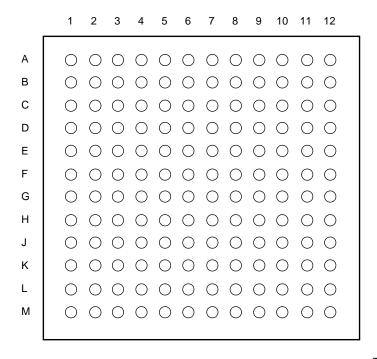
unit: mm (typ)

3409



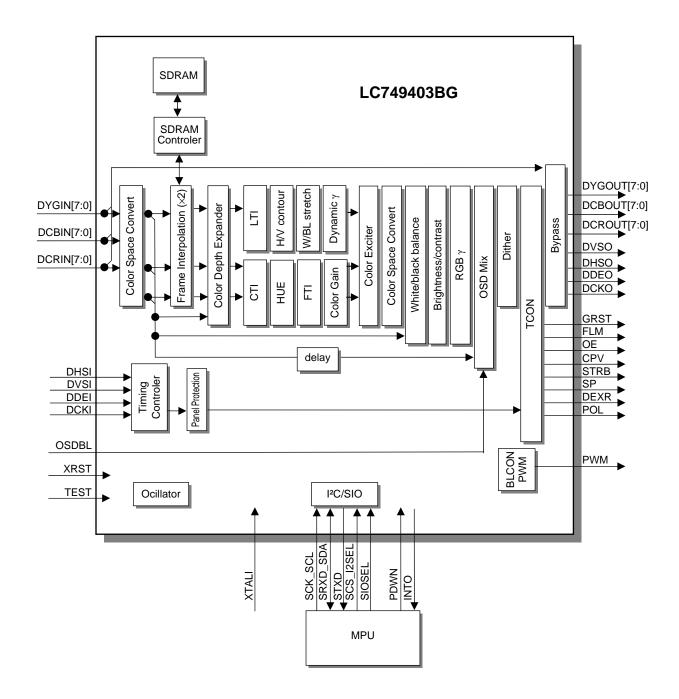
# **Pin Assignment**

#### LC749403BG



Top View

# **Block Diagram**



# **Pin Functions**

Pin No.	Din No Din symbol		ormat	Connecting destination		Pomarks		
PIII NO.	Pin symbol	I/O	Format	Connecting	desimation	Remarks		
A1	AV <sub>DD</sub> OSC	Р	-	Core voltage	Analog			
A2	RC_BIAS	I	J	Resistor	Analog	Bias resistor connection (connect this pin to GND with a $20k\Omega$ )		
А3	AV <sub>SS</sub> _OSC	Р	-	GND	Analog			
A4	DHSI	I	С	CMOS	Digital	Horizontal synchronizing signal.		
A5	DDEI	1	С	CMOS	Digital	Data enable signal. Connect this pin to GND in the internal generation mode.		
A6	STXD	0	D	CMOS	Digital	SIO data		
A7	SCK_SCL	I	С	CMOS	Digital	Bus clock (common to SIO and I <sup>2</sup> C)		
A8	XTALI	I	С	CMOS	Digital	Panel protection, PWM generation clock Connect this pin to GND when not to be used.		
A9	TEST	I	В	CMOS	Digital	Test (Normally, connect this pin to GND)		
A10	AV <sub>DD</sub> _PLL	Р	-	PLL voltage	Analog			
A11	PDO	0	J		Analog	Test (Normally, connect this pin to GND)		
A12	AV <sub>SS</sub> _PLL	Р	-	GND	Analog			
B1	DCRIN2	- 1	С	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.		
B2	DV <sub>DD</sub> CORE	Р	-	Core voltage	Digital			
В3	DV <sub>SS</sub>	Р	-	GND	Digital			
B4	DV <sub>SS</sub>	Р	-	GND	Digital			
B5	DVSI	I	С	CMOS	Digital	Vertical synchronizing signal		
B6	SRXD_SDA	I/O	G	CMOS	Digital	SIO data input/I <sup>2</sup> C data input/output		
В7	XRST	I	Α	CMOS	Digital	System reset ("L" reset)		
B8	DCKI	I	С	CMOS	Digital	Video clock.		
B9	DV <sub>DD</sub> SDIO	Р	-	IO voltage	Digital			
B10	$DV_SS$	Р	-	GND	Digital			
B11	DV <sub>SS</sub>	Р	-	GND	Digital			
B12	DCKO	0	F	CMOS	Digital	Video clock output		
C1	DCRIN1	I	С	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.		
C2	DCRIN0	I	С	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.		
C3	SDV <sub>SS</sub>	Р	-	GND	Digital	SDRAM ground		
C4	SDV <sub>SS</sub>	Р	-	GND	Digital	SDRAM ground		
C5	DV <sub>DD</sub> CORE	Р	-	Core voltage	Digital			
C6	INTO	0	D	CMOS	Digital	Interrupt		
C7	PDWN	I	А	CMOS	Digital	"L" power down  Connect this pin to GND when not to be used.		
C8	SIOSEL	I	С	CMOS	Digital	"L": I <sup>2</sup> C slave, "H": 3 wire SIO		
C9	DVSS	Р	-	GND	Digital			
C10	DVSS	Р	-	GND	Digital			
C11	DHSO/SP2	0	E	CMOS	Digital	Horizontal synchronizing signal/Start pulse signal for source driver		
C12	DVSO/FLM2	0	Е	CMOS	Digital	Vertical synchronizing signal/Start pulse signal for gate driver		

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Pin No. Pin symbol		Input/out	out format	Connecting destination		Remarks			
1 11110.	1 III Symbol	I/O	Format	Cormodaling documentary		Kemaks			
D1	DCRIN3	1	С	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.			
D2	DCRIN4	1	С	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.			
D3	DCRIN5	I	С	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.			
D4	DV <sub>SS</sub>	Р	-	GND	Digital				
D5	SDV <sub>SS</sub>	Р	-	GND	Digital	SDRAM ground			
D6	SDVSS	Р	-	GND	Digital	SDRAM ground			
D7	$SDV_DD$	Р	-	IO voltage	Digital	SDRAM power			
D8	SDV <sub>DD</sub>	Р	-	IO voltage	Digital	SDRAM power			
D9	PWM	0	D	CMOS	Digital	Pulse width modulation waveform			
D10	OSDBL	1	С	CMOS	Digital	Data enable signal for external OSD. (Connect to GND when not used.)			
D11	SCS_I2SEL	ı	А	CMOS	Digital	SIO chip enable/l <sup>2</sup> C slave select			
D12	DDEO	0	Е	CMOS	Digital	Data enable signal			
	B0B111=			21122		R/Cr video(MSB).			
E1	DCRIN7	I	С	CMOS	Digital	Connect this pin to GND when not to be used.			
E2	DCRIN6	I	С	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.			
E3	DYGIN1	I	С	CMOS	Digital	G/Y/656 video. Connect this pin to GND when not to be used.			
E4	DYGIN0	ı	С	CMOS	Digital	G/Y/656 video (LSB).			
					_	Connect this pin to GND when not to be used.			
E5	DV <sub>DD</sub> _IO	P	-	IO voltage	Digital				
E6	DV <sub>DD</sub> IO	P	-	IO voltage	Digital				
E7	DV <sub>DD</sub> _IO	Р	-	IO voltage	Digital				
E8	DV <sub>DD</sub> _CORE	Р	-	Core voltage	Digital				
E9	DBOUT4	0	E	CMOS	Digital	B/Cb/C video			
E10	DBOUT5	0	E	CMOS	Digital	B/Cb/C video			
E11	DBOUT6	0	E	CMOS	Digital	B/Cb/C video			
E12	DBOUT7	0	E	CMOS	Digital	B/Cb/C video (MSB)			
F1	DYGIN3	ļ	С	CMOS	Digital	G/Y/656 video. Connect this pin to GND when not to be used.			
F2	DYGIN2	I	С	CMOS	Digital	G/Y/656 video. Connect this pin to GND when not to be used.			
F3	DYGIN5	I	С	CMOS	Digital	G/Y/656 video. Connect this pin to GND when not to be used.			
F4	DYGIN4	I	С	CMOS	Digital	G/Y/656 video. Connect this pin to GND when not to be used.			
F5	DV <sub>DD</sub> _CORE	Р	-	Core voltage	Digital				
F6	DV <sub>DD</sub> _CORE	Р	-	Core voltage	Digital				
F7	DV <sub>DD</sub> _IO	Р	-	IO voltage	Digital				
F8	DV <sub>DD</sub> CORE	Р	-	Core voltage	Digital				
F9	DBOUT1	0	E	CMOS	Digital	B/Cb/C video			
F10	DBOUT3	0	E	CMOS	Digital	B/Cb/C video			
F11	DBOUT0	0	Е	CMOS	Digital	B/Cb/C video (LSB)			
F12	DBOUT2	0	Е	CMOS	Digital	B/Cb/C video			

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Pin No. Pin symbol		Input/out	out format	Connecting destination		Remarks		
1 111110.	T III SYIIIDOI	I/O	Format	Connecting	destination	Remarks		
G1	DCBIN0	I	С	CMOS	Digital	B/Cb/C video		
G2	DYGIN6	I	С	CMOS	Digital	G/Y/656 video		
G3	DYGIN7	I	С	CMOS	Digital	G/Y/656 video		
G4	DCBIN1	I	С	CMOS	Digital	B/Cb/C video. Connect this pin to GND when not to be used.		
G5	DV <sub>DD</sub> CORE	Р	-	Core Voltage	Digital			
G6	DV <sub>DD</sub> CORE	Р	-	Core Voltage	Digital			
G7	DV <sub>DD</sub> SDIO	Р	-	IO voltage	Digital			
G8	DV <sub>DD</sub> SDIO	Р	-	IO voltage	Digital			
G9	DGOUT5	0	E	CMOS	Digital	G/Y/656 video		
G10	DGOUT6	0	Е	CMOS	Digital	G/Y/656 video		
G11	DGOUT3	0	Е	CMOS	Digital	G/Y/656 video		
G12	DGOUT7	0	Е	CMOS	Digital	G/Y/656 video (MSB)		
H1	DCBIN4	I	С	CMOS	Digital	B/Cb/C video		
H2	DCBIN3	I	С	CMOS	Digital	B/Cb/C video		
НЗ	DCBIN2	1	С	CMOS	Digital	B/Cb/C video		
H4	DCBIN5	I	С	CMOS	Digital	B/Cb/C video		
H5	DV <sub>DD</sub> SDIO	Р	-	IO voltage	Digital			
H6	DV <sub>DD</sub> SDIO	Р	-	IO voltage	Digital			
H7	DV <sub>DD</sub> SDIO	Р	-	IO voltage	Digital			
H8	DV <sub>DD</sub> _SDIO	Р	-	IO voltage	Digital			
Н9	DGOUT0	0	Е	CMOS	Digital	G/Y/656 video (LSB)		
H10	DGOUT1	0	Е	CMOS	Digital	G/Y/656 video		
H11	DGOUT2	0	Е	CMOS	Digital	G/Y/656 video		
H12	DGOUT4	0	Е	CMOS	Digital	G/Y/656 video		
J1	CPV	I/O	Н	CMOS	Digital	Clock signal for gate driver		
J2	STRB	I/O	Н	CMOS	Digital	Data strobe signal for source driver		
J3	DEXR	0	Е	CMOS	Digital	Video inverse signal output for DTR		
J4	DV <sub>SS</sub>	Р	-	GND	Digital			
J5	DV <sub>SS</sub>	Р	-	GND	Digital			
J6	DV <sub>SS</sub>	Р	-	GND	Digital			
J7	DV <sub>SS</sub>	Р	-	GND	Digital			
J8	DV <sub>SS</sub>	Р	-	GND	Digital			
J9	DV <sub>SS</sub>	Р	-	GND	Digital			
J10	DVSS	Р	-	GND	Digital			
J11	DV <sub>SS</sub>	Р	-	GND	Digital			
J12	DROUT7	I/O	Н	CMOS	Digital	R/Cr video (MSB)		

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Pin No. Pin symbol		Input/out	out format	Connecting destination		Remarks				
1 111110.	i iii syiiiboi	I/O	Format	Connecting	destination	Remarks				
K1	FLM	I/O	Н	CMOS	Digital	Start pulse signal for gate driver				
K2	OE	I/O	Н	CMOS	Digital	Output enable signal for gate driver				
K3	DVSS	Р	-	GND	Digital					
K4	DVSS	Р	-	GND	Digital					
K5	$DV_SS$	Р	-	GND	Digital					
K6	DVSS	Р	-	GND	Digital					
K7	DVSS	Р	-	GND	Digital					
K8	DVSS	Р	-	GND	Digital					
K9	DVSS	Р	-	GND	Digital					
K10	DV <sub>SS</sub>	Р	-	GND	Digital					
K11	DROUT0	I/O	Н	CMOS	Digital	R/Cr video (LSB)				
K12	DROUT6	I/O	Н	CMOS	Digital	R/Cr video				
L1	DCBIN7	ı	С	CMOS	Digital	B/Cb/C video (MSB).				
LI	DCBIN7	'	C	CIVIOS	Digital	Connect this pin to GND when not to be used.				
L2	SP	I/O	Н	CMOS	Digital	Start pulse signal for source driver				
L3	$SDV_DDQ$	Р	-	IO voltage	Digital	SDRAM power *1				
L4	$SDV_DDQ$	Р	-	IO voltage	Digital	SDRAM power *1				
L5	SDV <sub>DDQ</sub>	Р	-	IO voltage	Digital	SDRAM power *1				
L6	SDV <sub>DDQ</sub>	Р	-	IO voltage	Digital	SDRAM power *1				
L7	$SDV_DDQ$	Р	-	IO voltage	Digital	SDRAM power *1				
L8	$SDV_DDQ$	Р	-	IO voltage	Digital	SDRAM power *1				
L9	$SDV_{DDQ}$	Р	-	IO voltage	Digital	SDRAM power *1				
L10	DV <sub>SS</sub>	Р	-	GND	Digital					
L11	DROUT2	I/O	Н	CMOS	Digital	R/Cr video				
L12	DROUT5	I/O	Н	CMOS	Digital	R/Cr video				
M1	DCBIN6	I	С	CMOS	Digital	B/Cb/C video. Connect this pin to GND when not to be used.				
M2	POL	0	E	CMOS	Digital	Voltage polarity selection signal for source driver				
М3	GRST	I/O	Н	CMOS	Digital	Reset signal for gate driver				
M4	SDV <sub>SSQ</sub>	Р	-	GND	Digital	SDRAM ground *2				
M5	SDV <sub>SSQ</sub>	Р	-	GND	Digital	SDRAM ground *2				
M6	SDV <sub>SSQ</sub>	Р	-	GND	Digital	SDRAM ground *2				
M7	SDV <sub>SSQ</sub>	Р	-	GND	Digital	SDRAM ground *2				
M8	SDV <sub>SSQ</sub>	Р	-	GND	Digital	SDRAM ground *2				
M9	SDV <sub>SSQ</sub>	Р	-	GND	Digital	SDRAM ground *2				
M10	DROUT1	I/O	Н	CMOS	Digital	R/Cr video				
M11	DROUT3	I/O	Н	CMOS	Digital	R/Cr video				
M12	DROUT4	I/O	Н	CMOS	Digital	R/Cr video				

<sup>\*1:</sup> We recommend isolated power to be supplied to SDRAM for improved noise immunity.

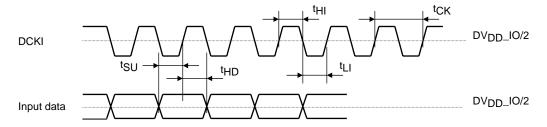
<sup>\*2:</sup> We recommend isolated ground to be supplied to SDRAM for improved noise immunity.

#### **Pin Circuits**

In/output form	Function	Equivalent circuit	Application Terminal
А	Schmitt trigger CMOS input		XRST, PDWN, SCS_I2SEL
В	CMOS input with built-in pull-down resister		TEST
С	CMOS input		SCK_SCL, SIOSEL, DVSI, DHSI, DDEI, OSDBL, DYGIN7, DYGIN6, DYGIN5, DYGIN4, DYGIN3, DYGIN2, DYGIN1, DYGIN0, DCBIN7, DCBIN6, DCBIN5, DCBIN4, DCBIN3, DCBIN2, DCBIN1, DCBIN0, DCRIN7, DCRIN6, DCRIN5, DCRIN4, DCRIN3, DCRIN2, DCRIN1, DCRIN0
D	2mA 3-STATE drive CMOS output		STXD, PWM, INTO
E	2mA/4mA switching 3-STATE drive CMOS output		DBOUT7, DBOUT6, DBOUT5, DBOUT4, DBOUT3, DBOUT2, DBOUT1, DBOUT0, DGOUT7, DGOUT6, DGOUT5, DGOUT4, DGOUT3, DGOUT2, DGOUT1, DGOUT0, DHSO/SP2, DVSO/FLM2, DDEO FLM, DEXR, POL
F	4mA/8mA switching 3-STATE drive CMOS output		DCKO
G	4mA 3-STATE drive CMOS input/output		SRXD_SDA
Н	2mA/4mA switching 3-STATE CMOS input/output		DROUT7, DROUT6, DROUT5, DROUT4, DROUT3, DROUT2, DROUT1, DROUT0, GRST, CPV, SP, OE, STRB
J	Analog input/output	<b>├</b>	RC_BIAS

# **Input/Output Timing**

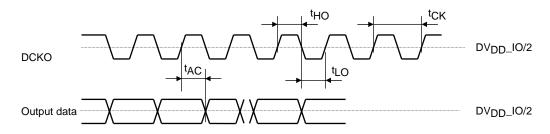
### (1) Input data timing



Pin Name	Parameter	Symbol	min	typ	max	unit
B014	Clock cycle	<sup>t</sup> CK	25			ns
DCKI	Duty			50		%
DCRIN*, DYGIN*, DCBIN*, DVSI, DHSI, DDEI, OSDBL	Input data set up time (DV <sub>DD</sub> _IO=2.6 to 3.6V)	<sup>t</sup> su	3			ns
	Input data set up time (DV <sub>DD</sub> _IO=1.7 to 1.95V)	<sup>t</sup> su	3			ns
	Input data hold time (DV <sub>DD</sub> _IO=2.6 to 3.6V)	<sup>t</sup> HD	2			ns
	Input data hold time (DV <sub>DD</sub> _IO=1.7 to 1.95V)	<sup>t</sup> HD	2			ns

<sup>\*:</sup> We recommend a 50% duty cycle for the input clock.

# (2) Output data timing



Pin Name	Parameter	Symbol	min	typ	max	unit
2010	Clock cycle	<sup>t</sup> CK	25			ns
DCKO	Duty			50		%
DROUT*, DGOUT*, DBOUT*, DVSO, DHSO, DDEO, DEXR, POL, SP, STRB, CPV, OE, FLM, GRST	Output data delay time (DV <sub>DD</sub> _IO=2.6 to 3.6V) I/O typ E: 4mA setting I/O typ F: 8mA setting	<sup>t</sup> AC	-3		3	ns
	Output data delay time (DV <sub>DD</sub> _IO=2.6 to 3.6V) I/O typ E: 2mA setting I/O typ F: 4mA setting	<sup>t</sup> AC	-3		6	ns
	Output data hold time (DV <sub>DD</sub> _IO=1.7 to 1.95V) I/O typ E: 4mA setting I/O typ F: 8mA setting	<sup>t</sup> AC	-5		4	ns
	Output data hold time (DV <sub>DD</sub> _IO=1.7 to 1.95V) I/O typ E: 2mA setting I/O typ F: 4mA setting	<sup>t</sup> AC	-6		9	ns

<sup>\*:</sup> When DCKO is set to the forward rotation output. Output load capacity: 5pF

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