M59BW102

1 Mbit (64Kb x16, Burst) Low Voltage Flash Memory

PRELIMINARY DATA

- 2.7 to 3.6V SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPERATIONS
- SEQUENTIAL CYCLE TIME: 25ns
- RANDOM ACCESS TIME
- PROGRAMMING TIME: 10µs typical
- INTERLEAVED ACCESS TIME: 16ns
- CONTINUOUS MEMORY INTERLEAVING
– Unlimited Linear Access Data Output
- PROGRAM/ERASE CONTROLLER (P/E.C.)
– Program Word-by-Word
– Status Register bits
- LOW POWER CONSUMPTION
– Stand-by and Automatic Stand-by
- 100,000 PROGRAM/ERASE CYCLES
- 20 YEARS DATA RETENTION
– Defectivity below 1ppm/year
- ELECTRONIC SIGNATURE
– Manufacturer Code: 20h
– Device Code: C1h

TSOP40 (N)
10 x 14mm

DESCRIPTION

The M59BW102 is a non-volatile memory that may be erased electrically at the chip level and programmed in-system on a Word-by-Word basis using only a single 3V V_{CC} supply. For Program and Erase operations the necessary high voltages are generated internally. The device can also be programmed in standard programmers.

The device can be programmed and erased over 100,000 cycles.

Instructions for Read/Reset, Auto Select for reading the Electronic Signature, Programming and Chip Erase are written to the device in cycles of commands to a Command Interface using standard microprocessor write timings. The M59BW102 features an interleaved access modality which allows extremely fast access time. The device is offered in TSOP40 (10 x 14mm) package.
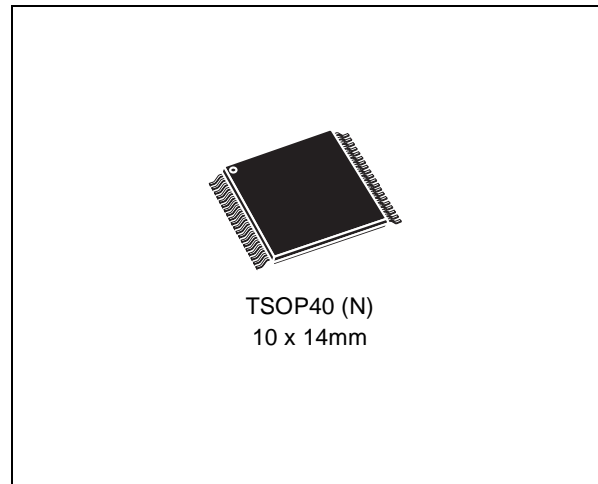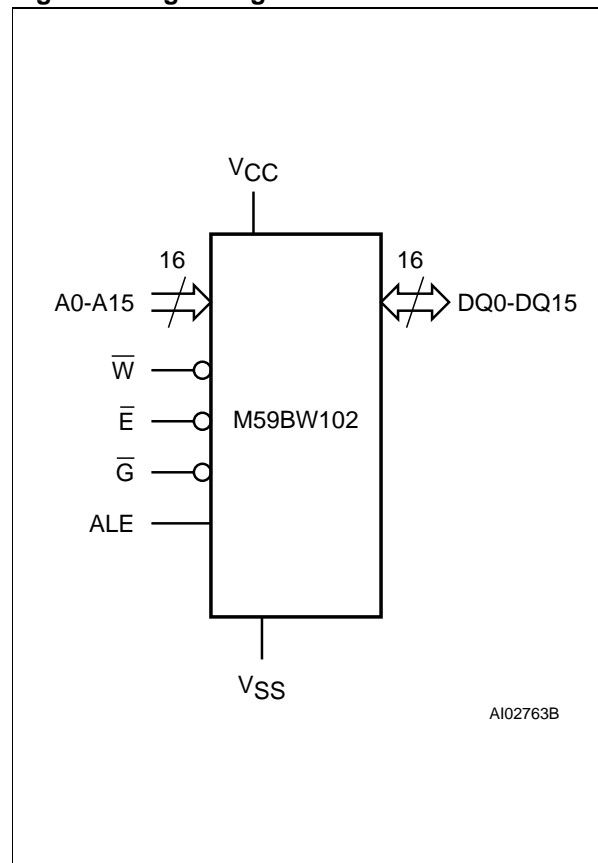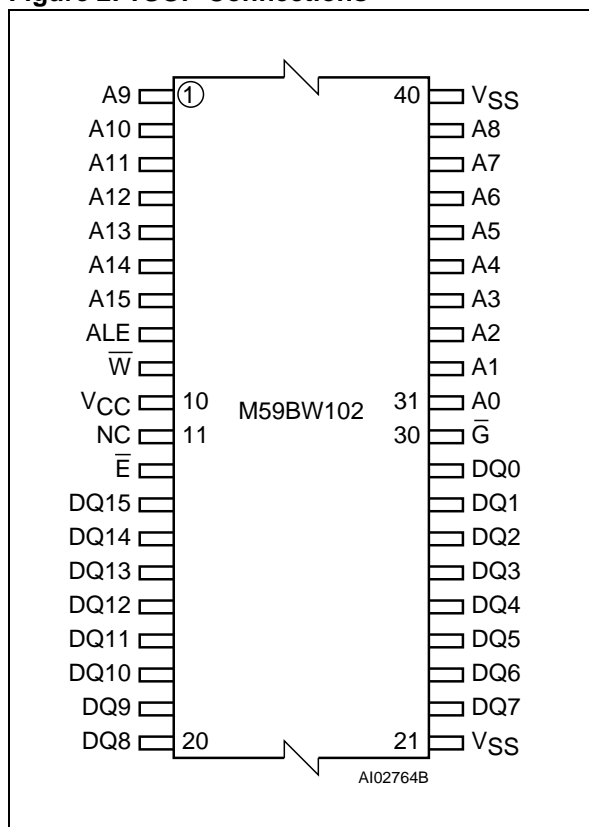
Figure 1. Logic Diagram

AI02763B

Figure 2. TSOP Connections

Table 1. Signal Names

A0-A15	Address Inputs
DQ0-DQ7	Data Inputs/Outputs, Command Inputs
DQ8-DQ15	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
ALE	Address Latch Enable
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

Organization

The M59BW102 is organized as 64K x16 bits. The memory uses the address inputs A0-A15 and the Data Inputs/Outputs DQ0-DQ15. Memory control is provided by Chip Enable $\overline{E}$, Output Enable $\overline{G}$, Address Latch Enable ALE and Write Enable $\overline{W}$ inputs.

Erase and Program operations are controlled by an internal Program/Erase Controller (P/E.C.). Status Register data output on DQ7 provides a Data Polling signal, and DQ6 and DQ2 provide Toggle signals to indicate the state of the P/E.C operations.

Bus Operations

The following operations can be performed using the appropriate bus cycles: Read (Array, Electronic Signature), Write command, Output Disable, Standby. See Tables 3 and 4.

Command Interface

Instructions, made up of commands written in cycles, can be given to the Program/Erase Controller through a Command Interface (C.I.). For added data protection, program or erase execution starts after 4 or 6 cycles. The first, second, fourth and fifth cycles are used to input Coded cycles to the C.I. This Coded sequence is the same for all Program/Erase Controller instructions. The 'Command' itself and its confirmation, when applicable, are given on the third, fourth or sixth cycles. Any incorrect command or any improper command sequence will reset the device to Read Array mode.

Instructions

Four instructions are defined to perform Read Array, Auto Select (to read the Electronic Signature), Program, Chip Erase. The internal P/E.C. automatically handles all timing and verification of the Program and Erase operations. The Status Register Data Polling, Toggle and Error bits may be read at any time, during programming or erase, to monitor the progress of the operation.

Instructions are composed of up to six cycles. The first two cycles input a Coded sequence to the Command Interface which is common to all instructions (see Table 7). The third cycle inputs the instruction set-up command. Subsequent cycles output the addressed data or Electronic Signature for Read operations. In order to give additional data protection, the instructions for Program and Chip Erase require further command inputs. For a Program instruction, the fourth command cycle inputs the address and data to be programmed. For an Erase instruction, the fourth and fifth cycles input a further Coded sequence before the command confirmation on the sixth cycle.

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{BIAS}	Temperature Under Bias	−50 to 125	°C
T_{STG}	Storage Temperature	−65 to 150	°C
V_{IO} [2]	Input or Output Voltage	−0.6 to 5	V
V_{CC}	Supply Voltage	−0.6 to 5	V
$V_{(A9, \overline{E}, \overline{G})}$ [2]	A9, $\overline{E}$, $\overline{G}$ Voltage	−0.6 to 13.5	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to −2V during transition and for less than 20ns.

Table 3. User Bus Operations [1]

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	ALE	A0	A1	A6	A9	A12	A15	DQ15-DQ0
Non Linear Access Mode	V_{IL}	V_{IL}	V_{IH}	Pulse	X	X	X	X	X	X	Data Output
Linear Access Cycle	V_{IL}	Rising Edge	V_{IH}	V_{IL}	X	x	X	X	X	X	Data Output
Write Word	V_{IL}	V_{IH}	V_{IL}	V_{IH}	A0	A1	A6	A9	A12	A15	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	X	X	Hi-Z
Standby	V_{IH}	X	X	X	X	X	X	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}.

Table 4. Read Electronic Signature (following AS instruction or with A9 = V_{ID})

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	Other Address	DQ15-DQ8	DQ7-DQ0
Manufact. Code	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Don't Care	00h	20h
Device Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Don't Care	00h	C1h

SIGNAL DESCRIPTIONS

See Figure 1 and Table 1.

Address Inputs (A0-A15). The address inputs for the memory array are latched during a write operation on the falling edge of Chip Enable $\overline{E}$ or Write Enable $\overline{W}$. When A9 is raised to V_{ID}, either a Read Electronic Signature Manufacturer or Device Code is enabled depending on the combination of levels on A0 and A1.

Data Inputs/Outputs (DQ0-DQ15). The input is data to be programmed in the memory array or a command to be written to the C.I. Both are latched on the rising edge of Chip Enable $\overline{E}$ or Write Enable $\overline{W}$. The output is data from the Memory Array, the Electronic Signature Manufacturer or Device codes, the Status register Data Polling bit DQ7, the Toggle Bits DQ6 and DQ2, the Error bit DQ5 or the Erase Timer bit DQ3. Outputs are valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High deselects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level.

Table 5. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Chip Erase Confirm
20h	Reserved
80h	Set-up Erase
90h	Read Electronic Signature
A0h	Program
F0h	Read Array/Reset

Output Enable ($\overline{G}$). The Output Enable gates the outputs through the data buffers during a read operation. When $\overline{G}$ and ALE are both High the outputs are High impedance.

Write Enable ($\overline{W}$). This input controls writing to the Command Register and Address and Data latches.

Address Latch Enable (ALE). This input controls the latching of address for reading. When pulsed, the device operates in the random or non linear access mode.

V_{CC} Supply Voltage. The power supply for all operations (Read, Program and Erase).

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

DEVICE OPERATIONS

See Tables 3 and 4.

Read (Non Linear Access Mode and Linear Access Cycle). The device is internally organized in two memory banks (named Even and Odd bank). A0 address bit is asserted as "priority" bit, so that when A0 = 0 the even bank is the current memory array under selection and the odd bank is masked. When A0 = 1 the odd bank is the current array under selection and even bank is masked.

To begin a random (or Non Linear) access mode (NLA), ALE is pulsed high and $\overline{E}$ is asserted low.

Two internal 15 bit counters store the current address for the odd and even banks and increment alternatively, under the priority bit control, during each subsequent cycle called sequential (or Linear) address cycle (LA). The linear cycle (LA) can be terminated if a new NLA starts or if $\overline{E}$ is asserted high, putting the device in stand-by mode. In this last case the linear cycle can be resumed if $\overline{E}$ is asserted low again and ALE is low.

During the LA mode all the memory can be swept, as there is no physical limits to the linear access output. When the last address of the memory is reached by the counters they start again from the first memory address and continue. The M59BW102 will provide data output during the LA cycle determined by $\overline{G}$ signal.

Each time ALE signal is pulsed and $\overline{G}$ signal is High, while the current address is loaded into the counters, the output buffers are put in Hi-Z condition and remain in this condition until the first new valid data comes. The M59BW102 operation in LA and NLA modes is explained in Figure 3 and the block diagram is shown in Figure 4.

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Address Latch Enable (ALE) is high, Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ whichever occurs last. Commands and Input Data are latched on the rising edge of $\overline{W}$ or $\overline{E}$ whichever occurs first.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ and the Address Latch Enable (ALE) are both High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when Chip Enable $\overline{E}$ is High and the P/E.C. is idle. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$, the Address Latch Enable (ALE) or the Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memory. The manufacturer's code for STMicroelectronics is 20h, the device code is C1h. These codes allow programming equipment or applications to automatically match their interface to the characteristics of the M59BW102. The Electronic Signature is output by a Read operation when the voltage applied to A9 is at V_{ID} and address inputs A1 is Low. The manufacturer code is output when the Address input A0 is Low and the device code when this input is High. Other Address inputs are ignored. The codes are output on DQ0-DQ7.

The Electronic Signature can also be read, without raising A9 to V_{ID}, by giving the memory the Instruction AS. The codes are output on DQ0-DQ7 with DQ8-DQ15 at 00h.

Table 6. Polling and Toggle Bits

Mode	DQ7	DQ6	DQ2
Program	$\overline{DQ7}$	Toggle	1
Erase	0	Toggle	Toggle

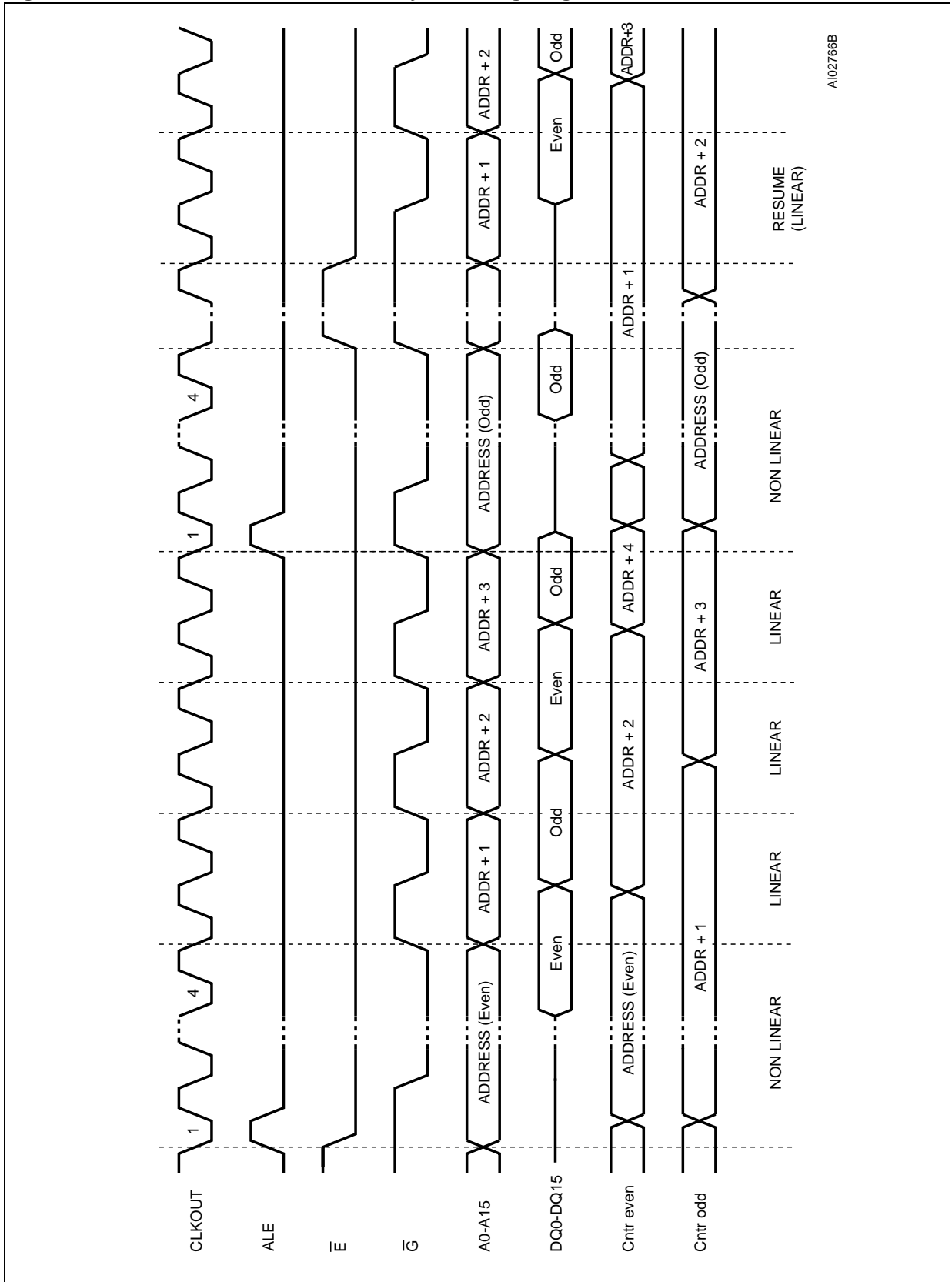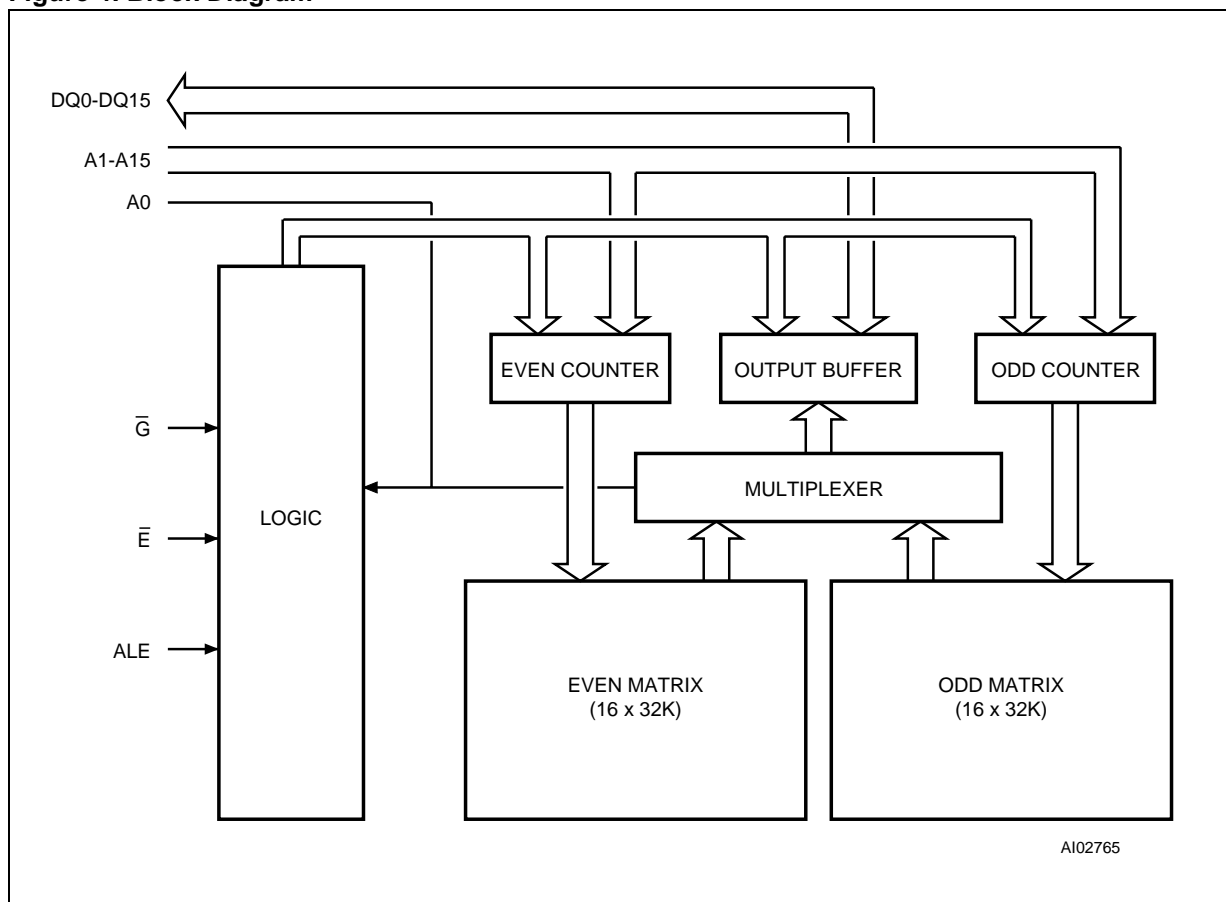**Figure 3. Non Linear and Linear Access Cycle Timing Diagram**

Figure 4. Block Diagram

INSTRUCTIONS AND COMMANDS

The Command Interface latches commands written to the memory. Instructions are made up from one or more commands to perform Read Memory Array, Read Electronic Signature, Program, Chip Erase. Commands are made of address and data sequences. The instructions require from 1 to 6 cycles, the first or first three of which are always write operations used to initiate the instruction. They are followed by either further write cycles to confirm the first command or execute the command immediately. Command sequencing must be followed exactly. Any invalid combination of commands will reset the device to Read Array. The increased number of cycles has been chosen to assure maximum data security. Instructions are initialised by two initial Coded cycles which unlock the Command Interface. In addition, for Erase, instruction confirmation is again preceded by the two Coded cycles.

Status Register Bits

P/E.C. status is indicated during execution by Data Polling on DQ7, detection of Toggle on DQ6 and

DQ2, or Error on DQ5 and Erase Timer DQ3 bits. Any read attempt from any address during Program or Erase command execution will automatically output these five Status Register bits. The P/E.C. automatically sets bits DQ2, DQ3, DQ5, DQ6 and DQ7. Other bits (DQ0, DQ1 and DQ4) are reserved for future use and should be masked. See Table 8.

Data Polling Bit (DQ7). When Programming operations are in progress, this bit outputs the complement of the bit being programmed on DQ7. During Erase operation, it outputs a '0'. After completion of the operation, DQ7 will output the bit last programmed or a '1' after erasing. Data Polling is valid and only effective during P/E.C. operation, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for erase. See Figure 11 for the Data Polling waveforms and Figure 12 for the Data Polling flowchart. A Valid Address is the address being programmed or any address while erasing the chip.

Toggle Bit (DQ6). When Programming or Erasing operations are in progress, successive attempts to read DQ6 will output complementary

Table 7. Instructions [1]

Mne.	Instr.	Cyc.		1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.	7th Cyc.
RD [2,4]	Read/Reset Memory Array	1+	Addr. [3,6]	X	Read Memory Array until a new write cycle is initiated.					
			Data	F0h						
		3+	Addr. [3,6]	555h	2AAh	X	Read Memory Array until a new write cycle is initiated.			
			Data	AAh	55h	F0h				
AS [4]	Auto Select	3+	Addr. [3,6]	555h	2AAh	555h	Read Electronic Signature until a new write cycle is initiated. See Note 5.			
			Data	AAh	55h	90h				
PG	Program	4	Addr. [3,6]	555h	2AAh	555h	Program Address	Read Data Polling or Toggle Bit until Program completes.		
			Data	AAh	55h	A0h	Program Data			
CE	Chip Erase	6	Addr. [3,6]	555h	2AAh	555h	555h	2AAh	555h	Note 7
			Data	AAh	55h	80h	AAh	55h	10h	

Note: 1. Commands not interpreted in this table will default to read array mode.
2. A wait of 10µs is necessary after a Read/Reset command if the memory was in an Erase or Program mode before starting any new operation.
3. X = Don't Care.
4. The first cycles of the RD or AS instructions are followed by read operations. Any number of read cycles can occur after the command cycles.
5. Signature Address bits A0, A1, at V_{IL} will output Manufacturer code (20h). Address bits A0 at V_{IH} and A1, at V_{IL} will output Device code.
6. For Coded cycles address inputs A11-A16 are don't care.
7. Read Data Polling, Toggle bits until Erase completes.

data. DQ6 will toggle following toggling of either $\overline{G}$, or $\overline{E}$ when $\overline{G}$ is low. The operation is completed when two successive reads yield the same output data. The next read will output the bit last programmed or a '1' after erasing. The toggle bit DQ6 is valid only during P/E.C. operations, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. See Figure 13 for Toggle Bit flowchart and Figure 14 for Toggle Bit waveforms.

Toggle Bit (DQ2). This toggle bit, together with DQ6, can be used to determine the device status during the Erase operations. During Chip Erase a read operation will cause DQ2 to toggle since chip is being erased. DQ2 will be set to '1' during program operation and when erase is complete.

Error Bit (DQ5). This bit is set to '1' by the P/E.C. when there is a failure of programming or chip erase that results in invalid data in the memory. In case of an error in program, the chip must be discarded. The DQ5 failure condition will also appear if a user tries to program a '1' to a location that is previously programmed to '0'. The error bit resets after a Read/Reset (RD) instruction. In case of success of Program or Erase, the error bit will be set to '0'.

Erase Timer Bit (DQ3). This bit is set to '0' by the P/E.C. when the Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the erase timeout period is finished, after 50µs to 120µs, DQ3 returns to '1'.

Coded Cycles

The two Coded cycles unlock the Command Interface. They are followed by an input command or a confirmation command. The Coded cycles consist of writing the data AAh at address 555h during the first cycle. During the second cycle the Coded cycles consist of writing the data 55h at address 2AAh. Address lines A0 to A10 are valid; other address lines are 'don't care'. The Coded cycles happen on first and second cycles of the command write or on the fourth and fifth cycles.

Table 8. Status Register Bits

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase Complete	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.
		'0'	Erase On-going	
		DQ	Program Complete	
		$\overline{DQ}$	Program On-going	
6	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase or Program On-going	Successive reads output complementary data on DQ6 while Programming or Erase operations are on-going. DQ6 remains at constant level when P/E.C. operations are completed.
		DQ	Program Complete	
		'-1-1-1-1-1-1-1-'	Erase Complete	
5	Error Bit	'1'	Program or Erase Error	This bit is set to '1' in the case of Programming or Erase failure.
		'0'	Program or Erase On-going	
4	Reserved			
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started.
		'0'	Erase Timeout Period On-going	
2	Toggle Bit	'-1-0-1-0-1-0-1-'	Chip Erase	Indicates the erase status.
		'1'	Program On-going or Erase Complete	
1	Reserved			
0	Reserved			

Note: Logic level '1' is High, '0' is Low. -0-1-0-0-1-1-1-0- represent bit value in successive Read operations.

Instructions

See Table 7.

Read/Reset (RD) Instruction. The Read/Reset instruction consists of one write cycle giving the command F0h. It can be optionally preceded by the two Coded cycles. Subsequent read operations will read the memory array addressed and output the data read. Read/Reset is not accepted in Program/Erase operation unless a fail occurred.

Auto Select (AS) Instruction. This instruction uses the two Coded cycles followed by one write cycle giving the command 90h to address 555h for command set-up. A subsequent read will output the manufacturer code and the device code depending on the levels of A0 and A1. The manufacturer code, 20h, is output when the addresses

lines A0 and A1 are Low, the device code, C1h is output when A0 is High with A1 Low.

Program (PG) Instruction. This instruction uses four write cycles. The Program command A0h is written to address 555h on the third cycle after two Coded cycles. A fourth write operation latches the Address on the falling edge of $\overline{W}$ or $\overline{E}$ and the Data to be written on the rising edge and starts the P/E.C. Read operations output the Status Register bits after the programming has started. Memory programming is made only by writing '0' in place of '1'. Status bits DQ6 and DQ7 determine if programming is on-going and DQ5 allows verification of any possible error.

Chip Erase (CE) Instruction. This instruction uses six write cycles. The Set-up command 80h is writ-

Table 9. AC Measurement Conditions

Load Capacitance (C_L)	30pF
Input Rise and Fall Times	$\leq$ 10ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Figure 5. AC Testing Input Output Waveform
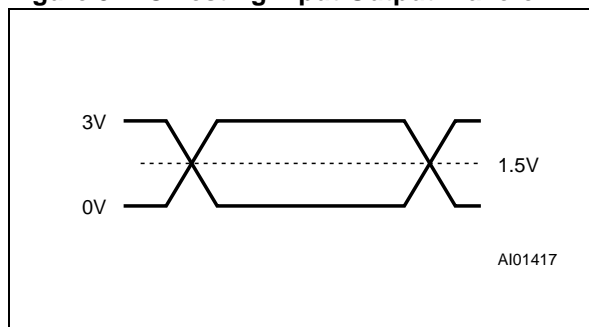
Figure 6. AC Testing Load Circuit
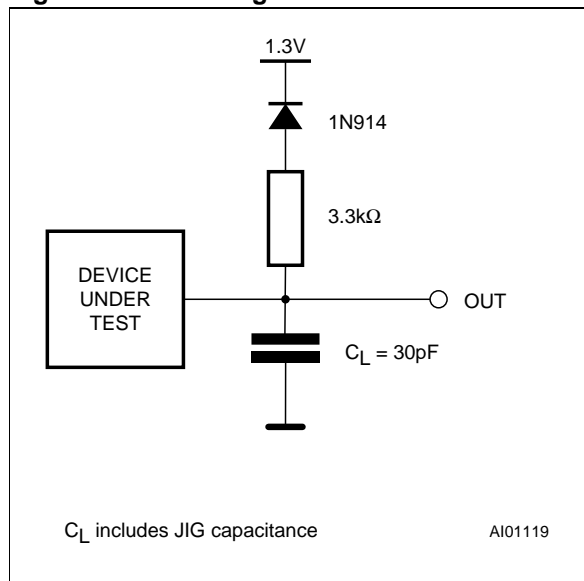
Table 10. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

ten to address 555h on the third cycle after the two Coded cycles. The Chip Erase Confirm command 10h is similarly written on the sixth cycle after another two Coded cycles. If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts and the device is reset to Read Array. It is not necessary to program the array with 0000h first as the P/E.C. will automatically do this before erasing it to FFFFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the Status Register bits. During the execution of the erase by the P/E.C., Data Polling bit DQ7 returns '0', then '1' on completion. The Toggle bits DQ2 and DQ6 toggle during erase operation and stop when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure.

POWER SUPPLY

Power Up

The memory Command Interface is reset on power up to Read Array. Either $\overline{E}$ or $\overline{W}$ must be tied to V_{IH} during Power Up to allow maximum security and the possibility to write a command on the first rising edge of $\overline{E}$ and $\overline{W}$. Any write cycle initiation is blocked when V_{CC} is below V_{LKO}.

Supply Rails

Normal precautions must be taken for supply voltage decoupling; each device in a system should have the V_{CC} rail decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{CC} program and erase currents required.

Table 11. DC Characteristics
(T_A = 0 to 70°C; V_{CC} = 3.0V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±1	µA
I_{CC1}	Supply Current (Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		10	mA
I_{CC2}	Supply Current (Standby)	ALE, $\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC3} [1]	Supply Current (Program or Erase)	Byte program or Chip Erase in progress		20	mA
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA		0.45	V
V_{OH}	Output High Voltage	I_{Oh} = −100µA	V_{CC} − 0.4V		V
V_{ID}	A9, $\overline{E}$, $\overline{G}$ High Voltage		11.5	12.5	V
I_{ID}	A9, $\overline{E}$, $\overline{G}$ High Current	A9, $\overline{E}$, $\overline{G}$ = V_{ID}		100	µA
V_{LKO} [1]	Supply Voltage (Erase and Program lock-out)		1.8	2.3	V

Note: 1. Sampled only, not 100% tested.

Table 12. Sequential Read Mode AC Characteristics
(T_A = 0 to 70°C)

Symbol	Alt	Parameter	Test Condition	M59BW102 25 V_{CC} = 3.0V to 3.6V Min	Typ	Max	Unit
t_{CYCLE}	t_{CY}	Sequential Cycle	$\overline{E} = V_{IL}$, ALE = V_{IL}	25			ns
t_{GHGL}	t_{GW}	Output Enable High to Output Enable Low	$\overline{G}$ = Pulse	13			ns
t_{GLGH}	t_{GL}	Output Enable Low to Output Enable High	$\overline{G}$ = Pulse	12			ns
t_{GHEL}	t_{ATT}	Output Enable High to Chip Enable Low		−2			ns
t_{GHEH}	t_{SBY}	Output Enable High to Chip Enable High		−2			ns
t_{EHALH}	t_{AV}	Chip Enable High to Address Latch Enable High		3			ns
t_{GHALH}	t_{GS}	Output Enable High to Address Latch Enable High (following cycle)		0			ns
t_{GHQV} [1]	t_{GACC}	Output Enable High to Output Valid				20	ns
t_{ELQV} [1]	t_{EACC}	Chip Enable Low to Output Valid				20	ns
t_{EHQZ}	t_{EDF}	Chip Enable High to Output Hi-Z				12	ns
t_{ALHQZ}	t_{ADF}	Address Latch Enable High to Output Hi-Z				20	ns

Note: 1. This timing refers to a Load Capacitance (C_L) of 30pF. If C_L is higher, add 1 ns for each extra 10pF.

Table 13. Random Read Mode AC Characteristics
$(T_A = 0 \text{ to } 70°C)$

Symbol	Alt	Parameter	Test Condition	M59BW102 25 $V_{CC} = 3.0V \text{ to } 3.6V$			Unit
				Min	Typ	Max	
t_{ALHALL}	t_{ALW}	Address Latch Enable High to Address Latch Enable Low	ALE = Pulse	10			ns
t_{ELALL}	t_E	Chip Enable Low to Address Latch Enable Low		10			ns
t_{AXALL}	t_{AS}	Address Transition to Address Latch Enable Low		6			ns
t_{EHALH}	t_{ELV}	Chip Enable High to Address Latch Enable High		3			ns
t_{ALLGL}	t_{AG}	Address Latch Enable Low to Output Enable Low		7.5			ns
t_{GHALH}	t_{QP}	Output Enable High to Address Latch Enable High		0			ns
t_{GHGL}	t_{GW}	Output Enable High to Output Enable Low	$\overline{G}$ = Pulse	14			ns
t_{GLGH}	t_{GL}	Output Enable Low to Output Enable High		48			ns
t_{GLQV} [1]	t_{GACC}	Output Enable Low to Output Valid				30	ns
t_{ELQV} [1]	t_{EACC}	Chip Enable Low to Output Valid				55	ns
t_{GHEL}	t_{GE}	Output Enable High to Chip Enable Low		−2			ns
t_{EHQZ}	t_{EDF}	Chip Enable High to Output Hi-Z				12	ns
t_{ALHQZ}	t_{ADF}	Address Latch Enable High to Output Hi-Z				20	ns
t_{QVGH}	t_{QV}	Output Valid to Output Enable High		10			ns
t_{GHEH}	t_{GE}	Output Enable High to Chip Enable High		0			ns
t_{ELGL}	t_{EGL}	Chip Enable Low to Output Enable Low		13			ns
t_{EHQV}		Chip Enable High to Data Hold		0			ns
t_{ALLAX}		Address Latch Enable Low to Address Transition		30			ns

Note: 1. This timing refers to a Load Capacitance (C_L) of 30pF. If C_L is higher, add 1ns for each extra 10pF.

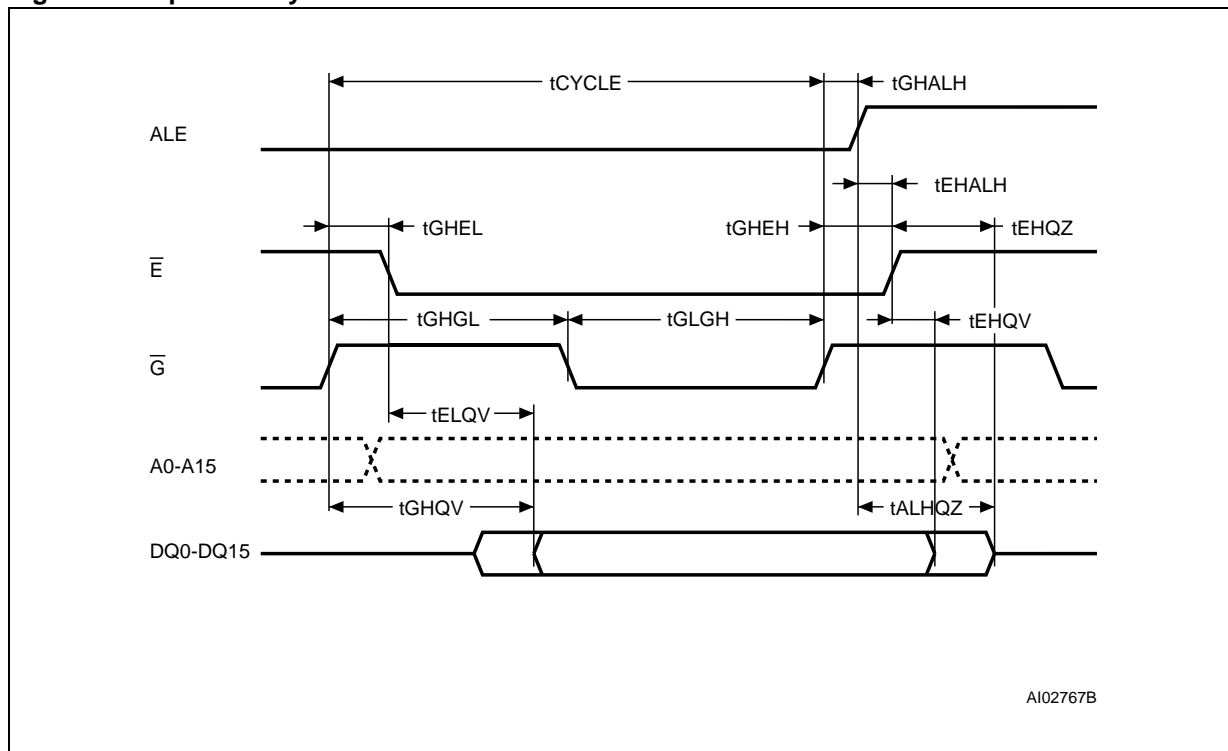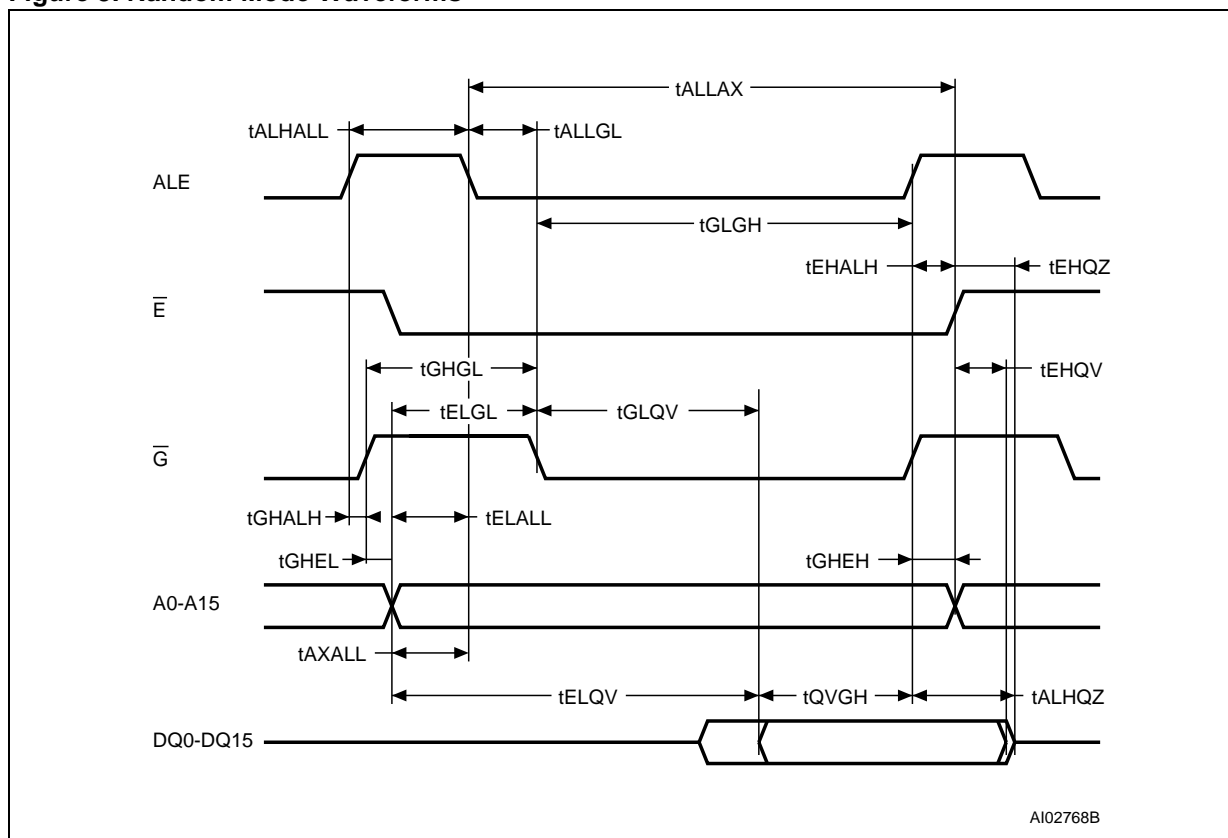**Figure 7. Sequential Cycle Waveforms**

AI02767B

Figure 8. Random Mode Waveforms

AI02768B

Table 14. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C)

Symbol	Alt	Parameter	M59BW102 25 V_{CC} = 3.0V to 3.6V		Unit
			Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	55		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	30		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	25		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	35		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		µs
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		ns

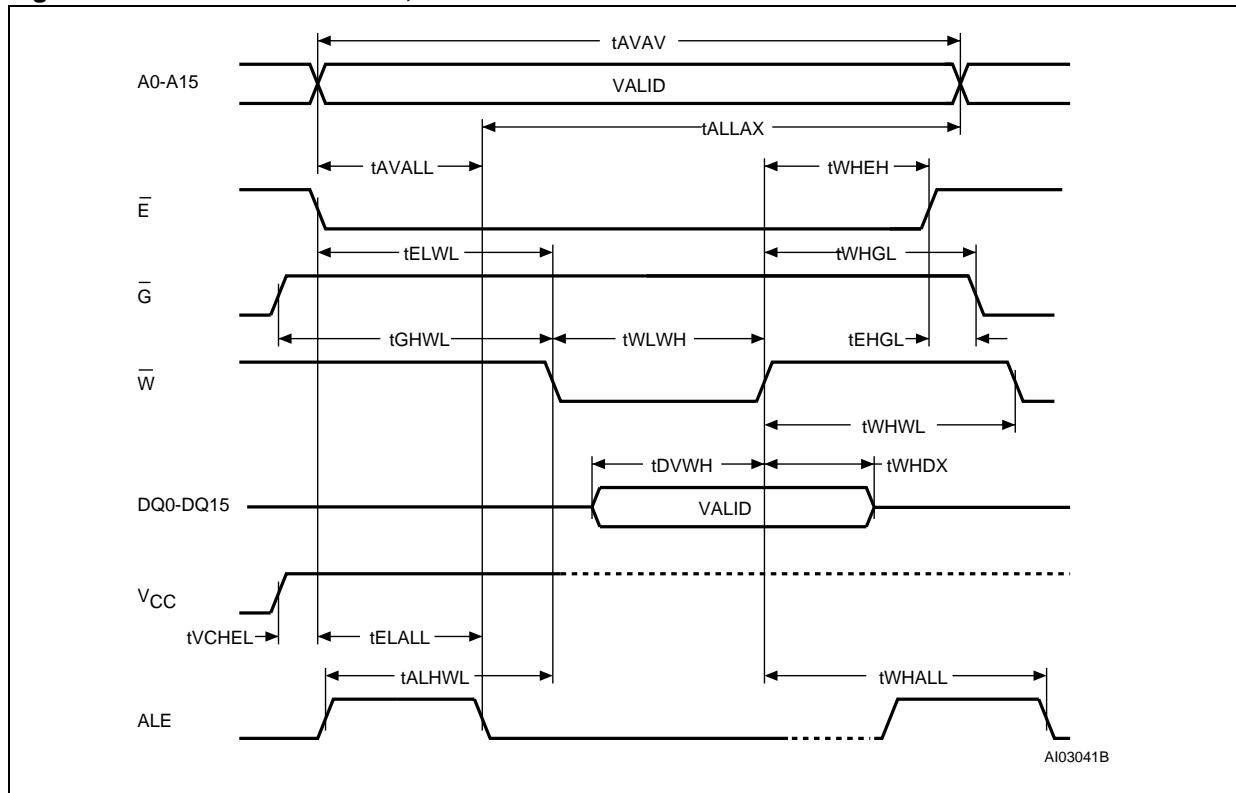### Figure 9. Write AC Waveforms, $\overline{W}$ Controlled
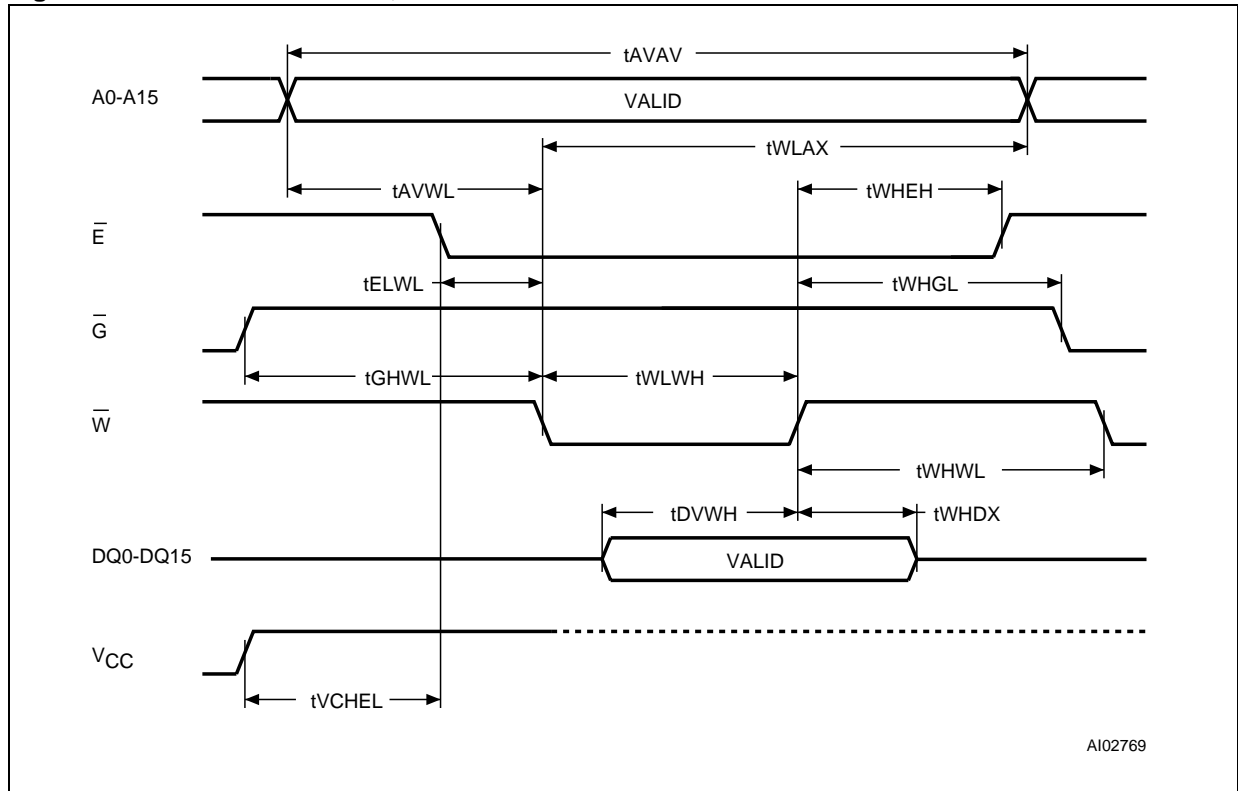
Note: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$; ALE must be High.

Table 15. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C)

Symbol	Alt	Parameter	M59BW102 25 V_{CC} = 3.0V to 3.6V Min	M59BW102 25 V_{CC} = 3.0V to 3.6V Max	Unit
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	55		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	30		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	25		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	35		ns
t_{GHEL}		Output Enable High to Chip Enable Low	0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		µs
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		ns

Figure 10. Write AC Waveforms, $\overline{E}$ Controlled
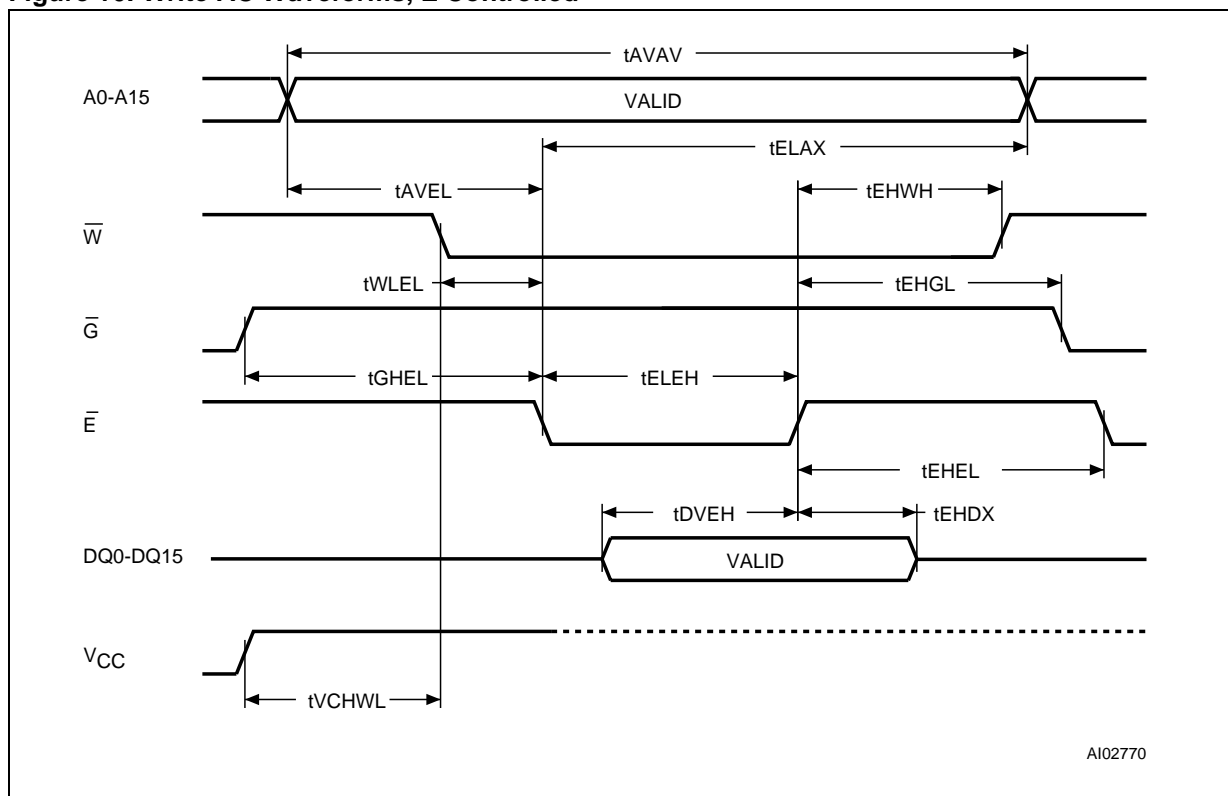
Note: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$; ALE must be High.

Table 16. Write AC Characteristics, Write Enable Controlled and Address Latch Enable Pulsed
(T_A = 0 to 70°C)

Symbol	Alt	Parameter	M59BW102 25 V_{CC} = 3.0V to 3.6V		Unit
			Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	55		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	30		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	25		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		ns
t_{WHWL} [1]	t_{WPH}	Write Enable High to Write Enable Low	20		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		µs
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		ns
t_{ALHWL}		Address Latch Enable High to Write Enable Low	10		ns
t_{AVALL}		Address Valid to Address Latch Enable Low	5		ns
t_{ELALL}		Chip Enable Low to Address Latch Enable Low	10		ns
t_{ALLAX}		Address Latch Enable Low to Address Transition	35		ns
t_{WHALL} [1]		Write Enable High to Address Latch Enable Low	50		ns
t_{EHGL}		Chip Enable High to Output Enable Low	10		ns

Note: 1. These parameters are applicable only if the following cycle is for the same device.

Figure 11. Write AC Waveforms, $\overline{W}$ Controlled and Address Latch Enable Pulsed
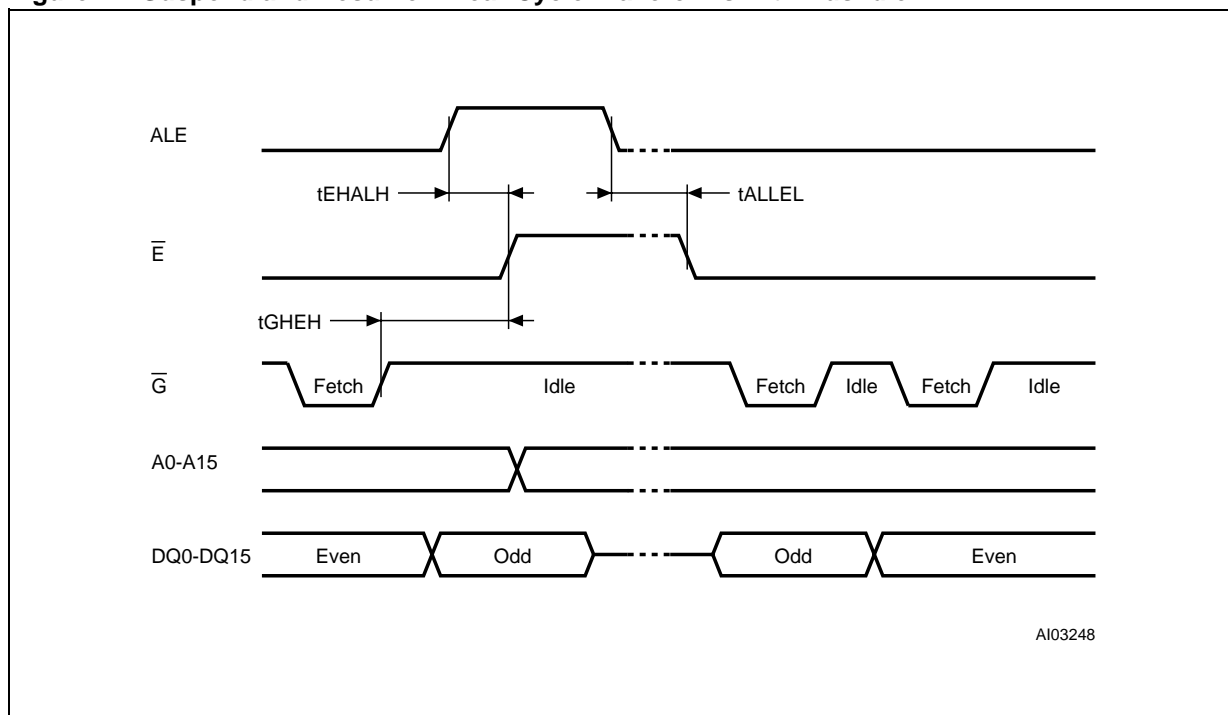

Note: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$.

Table 17. Suspend and Resume Last Linear Cycle Characteristics
(T_A = 0 to 70°C)

Symbol	Alt	Parameter	M59BW102 25 V_{CC} = 3.0V to 3.6V		Unit
			Min	Max	
t_{ALLEL}		Address Latch Enable Low to Chip Enable Low	15		ns

Figure 12. Suspend and Resume Linear Cycle Waveforms with Bus Idle

Table 18. Suspend and Resume Next Linear Cycle Characteristics
(T_A = 0 to 70°C)

Symbol	Alt	Parameter	M59BW102 25 V_{CC} = 3.0V to 3.6V		Unit
			Min	Max	
t_{ALLEL}		Address Latch Enable Low to Chip Enable Low	15		ns

Figure 13. Suspend and Resume Linear Cycle Waveforms without Bus Idle
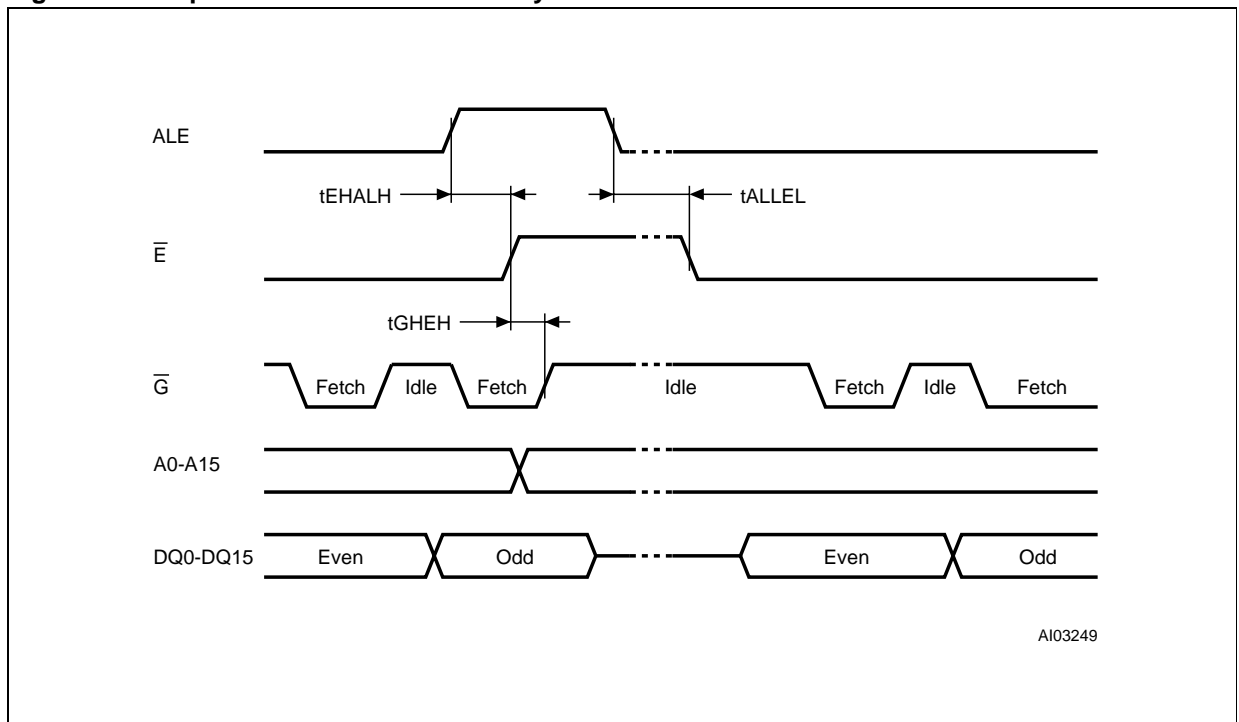
Table 19. Data Polling and Toggle Bit AC Characteristics [1]

(T_A = 0 to 70°C)

Symbol	Parameter	M59BW102 25 V_{CC} = 3.0V to 3.6V		Unit
		Min	Max	
t_{WHQ7V}	Write Enable High to DQ7 Valid (Program, $\overline{W}$ Controlled)	10	2400	µs
	Write Enable High to DQ7 Valid (Chip Erase, $\overline{W}$ Controlled)	1	30	sec
t_{EHQ7V}	Chip Enable High to DQ7 Valid (Program, $\overline{E}$ Controlled)	10	2400	µs
	Chip Enable High to DQ7 Valid (Chip Erase, $\overline{E}$ Controlled)	1	30	sec
t_{Q7VQV}	DQ7 Valid to Output Valid (Data Polling)		25	ns
t_{WHQV}	Write Enable High to Output Valid (Program)	10	2400	µs
	Write Enable High to Output Valid (Chip Erase)	1	30	sec
t_{EHQV}	Chip Enable High to Output Valid (Program)	10	2400	µs
	Chip Enable High to Output Valid (Chip Erase)	1	30	sec

Note: 1. All other timings are defined in Read AC Characteristics table.

Figure 14. Data Polling DQ7 AC Waveform

Note: ALE must be high.
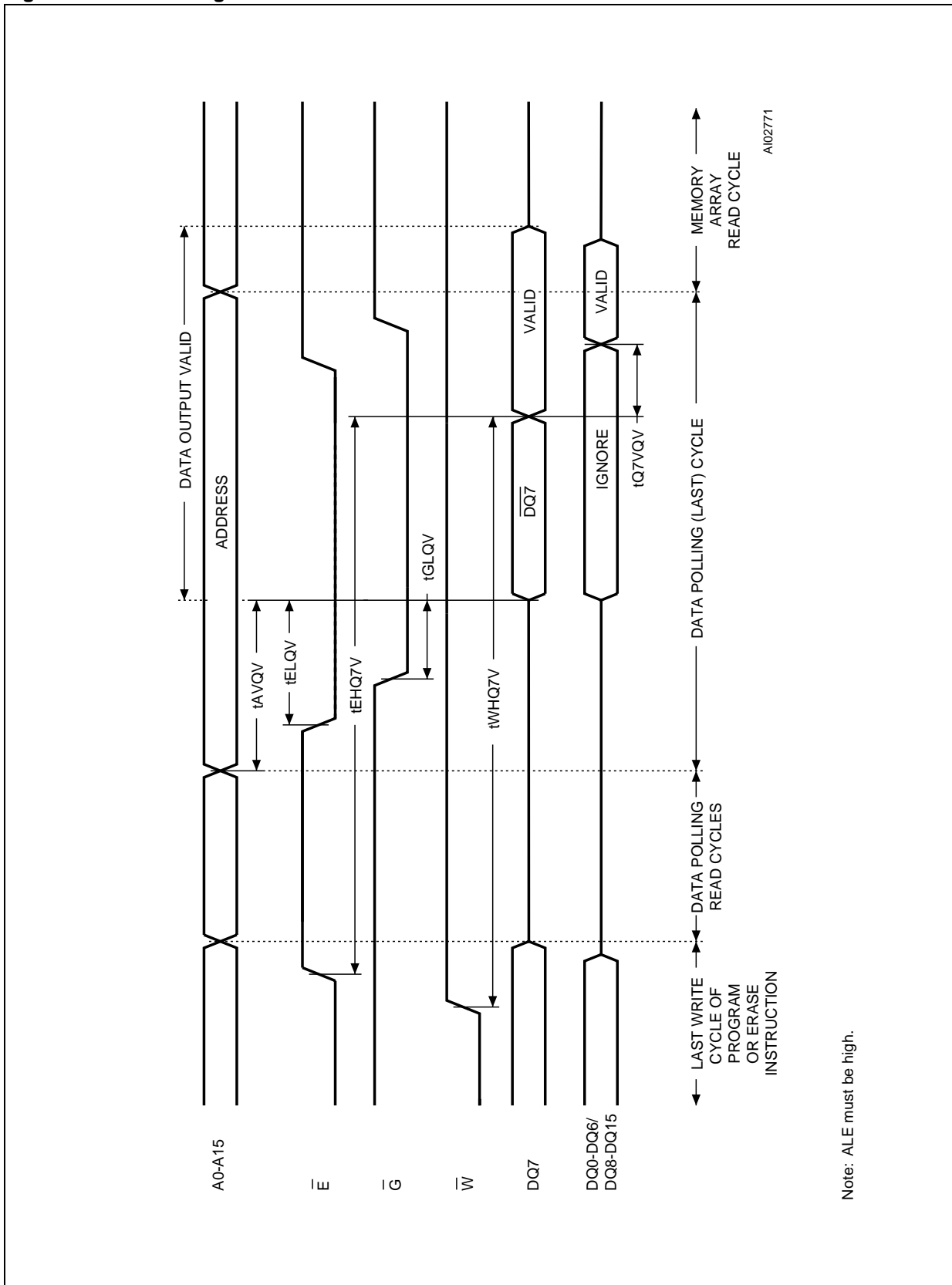
Figure 15. Data Polling Flowchart

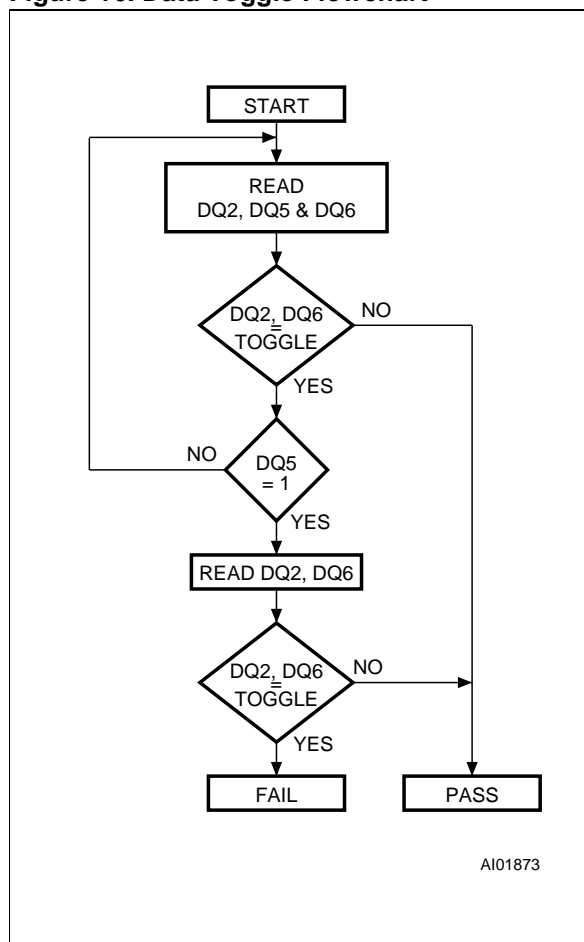AI01369B
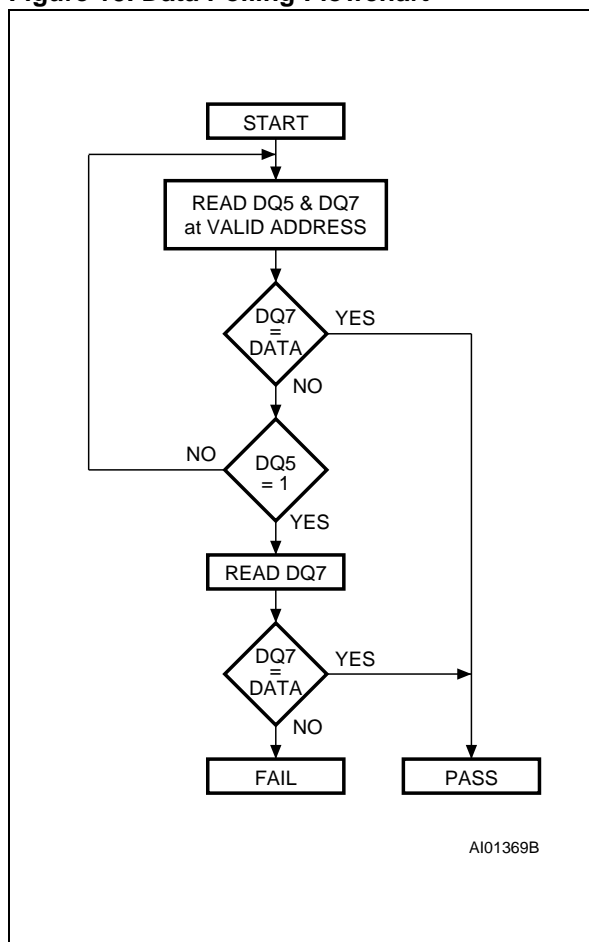
Figure 16. Data Toggle Flowchart

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Table 20. Program, Erase Times and Program, Erase Endurance Cycles
(T_A = 0 to 70°C; V_{CC} = 3.0V to 3.6V)

Parameter	M59BW102			Unit
	Min	Typ	Typical after 100k W/E Cycles	
Chip Erase (Preprogrammed)		0.7	0.7	sec
Chip Erase		1.5	1.5	sec
Chip Program		0.7	0.7	sec
Word Program		10	10	µs
Program/Erase Cycles	100,000			cycles

Figure 17. Data Toggle DQ6, DQ2 AC Waveforms
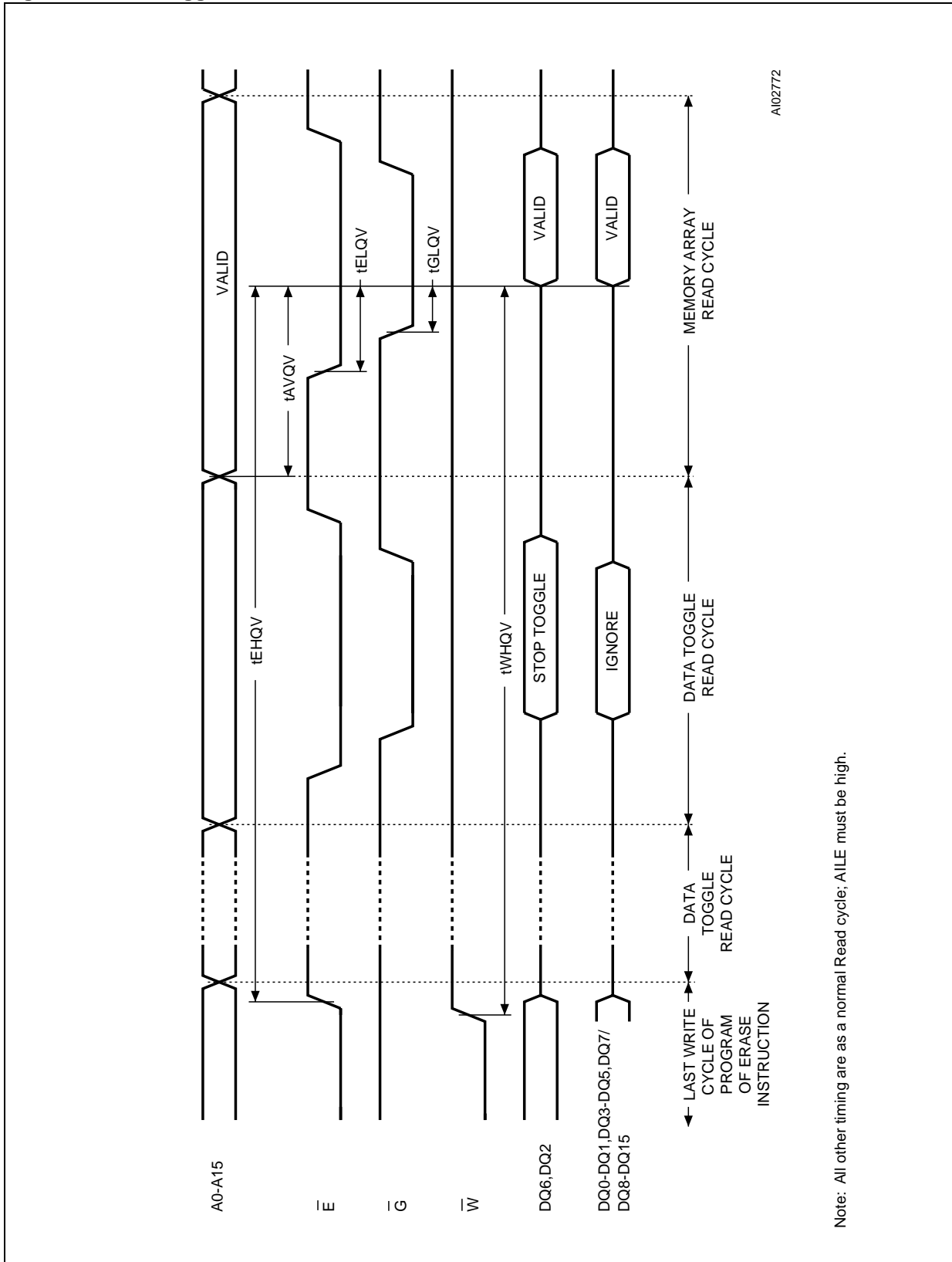
Note: All other timing are as a normal Read cycle; AILE must be high.

Table 21. Ordering Information Scheme

Example: M59BW102   25   N   1   T

Device Type

M59

Architecture

B = Burst Mode

Operating Voltage

W = V_{CC} = 2.7 to 3.6V

Device Function

102 = 1 Mbit (64Kb x16)

Speed

25 = 25 ns sequential cycle time, 55 ns random access time

Package

N = TSOP40: 10 x 14 mm

Temperature Range

1 = 0 to 70 °C

Option

T = Tape & Reel Packing

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 22. TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 14 mm, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.0472
A1		0.05	0.15		0.0020	0.0059
A2		0.95	1.05		0.0374	0.0413
B		0.17	0.27		0.0067	0.0106
C		0.10	0.21		0.0039	0.0083
D		13.80	14.20		0.5433	0.5591
D1		12.30	12.50		0.4843	0.4921
E		9.90	10.10		0.3898	0.3976
e	0.50	–	–	0.0197	–	–
L		0.50	0.70		0.0197	0.0276
α		0°	5°		0°	5°
N		40			40	
CP			0.10			0.0039

Figure 18. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20 mm, Package Outline

Drawing is not to scale.