Features

- 4-bit HARVARD Architecture
- 4k × 8-bit Application ROM
- 256 × 4-bit RAM
- 32 × 16-bit EEPROM
- 10 Bi-directional I/Os
- 4 External Interrupt Inputs (SSO20)
- 8 Interrupt Levels
- 2 × 8-bit Multifunction Timer/Counter
- Interval Timer with Watchdog
- Two-Wire Interface (TWI)
- Voltage Supervisor
- On-chip RC Oscillator
- On-chip Crystal Oscillator

Pb Lead Free

Benefits

- Contactless Power Supply and Communication Interface
- Power Management for Contactless and Battery Power Supply
- Shift-register-supported Modulator and Demodulator Stages
- Low Power Consumption
- Active Mode < 300 µA at 2V and 1 MHz System Clock Frequency (2 µs Instruction Cycle)
- Power-down Mode < 1 µA
- Supply Voltage 2.0V to 6.5V
- High-level Language Programming in qFORTH
- Operating Speed: 1 µs to 10 µs Instruction Cycle (2 µs at V_{DD} = 2V)

1. Description

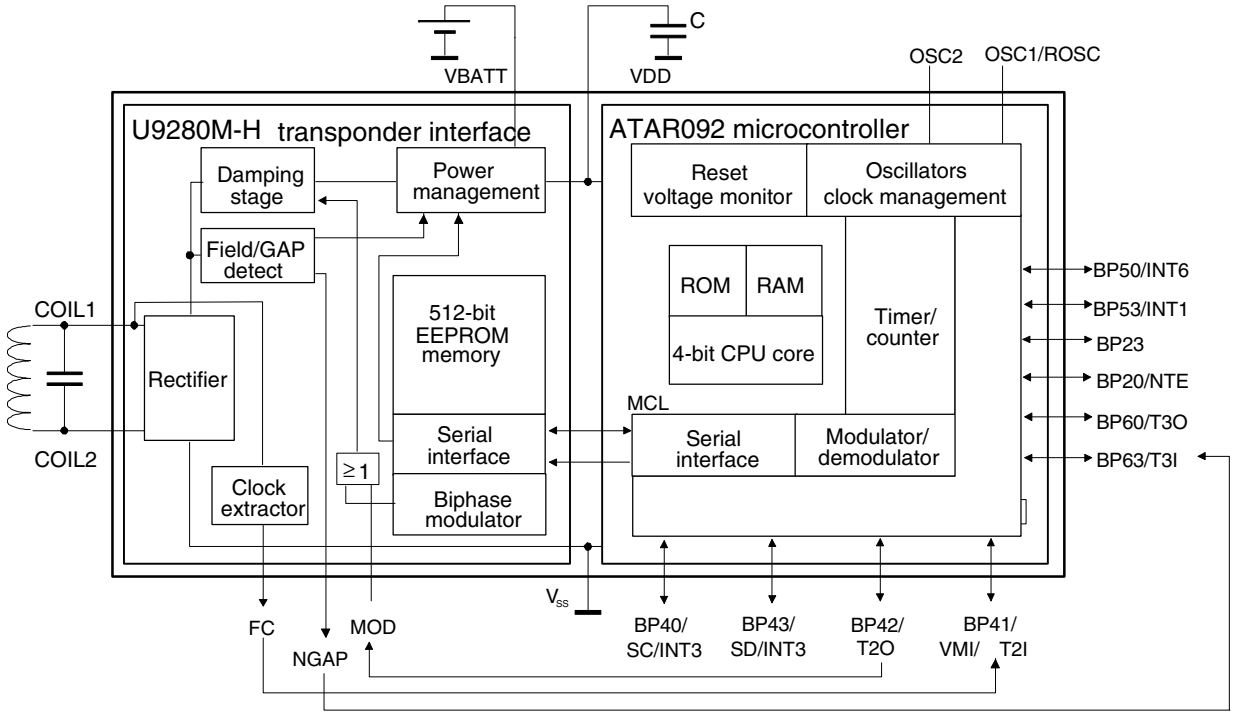
The U9280M-H IC is a multi-chip module for remote control and contactless ID systems. It consists of the ATAR092 microcontroller and U3280M transponder interface circuit with EEPROM. A coil connected to the transponder interface serves as a wireless bi-directional communication interface as well as a power supply for the microcontroller and the interface. As a transponder, the device is supplied by a magnetic RF field applied at the coil. For IR- or RF-transmitter applications, it can be supplied by a battery. The microcontroller supports, with its built-in timers, a wide range of IR- and RF-transmission modes such as burst-modulation modes, PWM-, NRZ-, Manchester- and Bi-phase coding.

Microcontroller with Transponder Interface

U9280M-H

Rev. 4591B–RFID–09/05

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SSO20

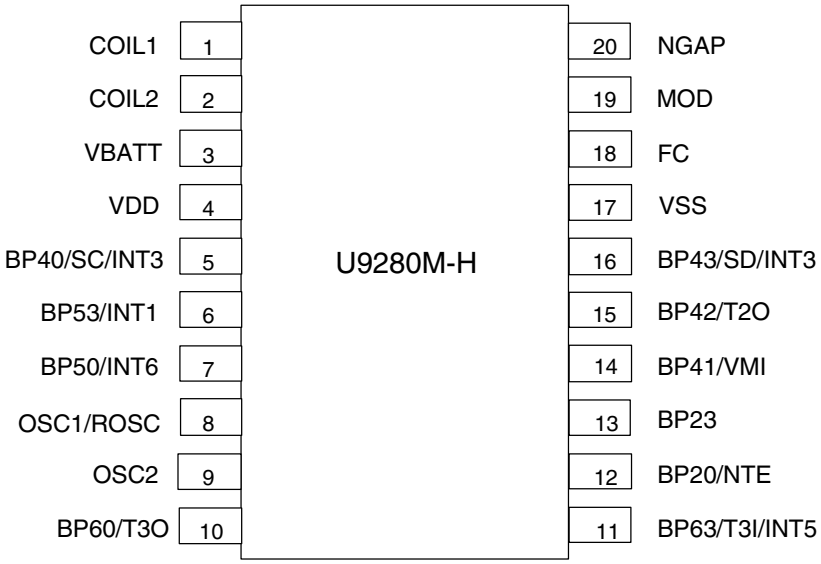


Table 2-1. Pin Description

Pin	Symbol	Function
1	COIL1	Coil input 1, Pin to connect an LC antenna for communication and field supply
2	COIL2	Coil input 2, Pin to connect an LC antenna for communication and field supply
3	VBATT	Power-supply voltage input to connect a battery
4	VDD	Power-supply voltage for the microcontroller and EEPROM. At this pin a capacitor (0.5 µF to 10 µF) must be connected to buffer the voltage during field supply and to block the V_{DD} of the microcontroller.
5	BP40/SC/INT3	I/O-port line/serial clock line/INT3 input (falling edge sensitive)
6	BP53/INT3	I/O-port line/INT3 interrupt input (falling or rising edge sensitive)
7	BP50/INT6	I/O-port line/INT6 interrupt input (falling or rising edge sensitive)
8	OSC1/ROSC	Oscillator- or external system-clock input/input for RC-oscillator resistor
9	OSC2	Oscillator output
10	BP60/T3O	Bi-directional I/O-line/Timer 3 output/modulator output
11	BP63/T3I/INT5	I/O-port line/INT5 interrupt input/Timer 3 input/demodulator input
12	BP20/NTE	BP20-I/O-port line/test mode input. This input is used to control the test modes. During POR it must not be connected with a low impedance to $V_{DD.}$
13	BP23	I/O-port line
14	BP41/VMI	I/O-port line/Voltage monitor input/Timer 2 input
15	BP42/T2O	I/O-port line/Timer 2 output/modulator output
16	BP43/SD/INT3	I/O-port line/serial data line/INT3 input (falling edge sensitive)
17	VSS	Circuit ground
18	FC	Field clock output of the clock extractor
19	MOD	Modulation input - front end. Must be connected to the modulator output T2O.
20	NGAP	Gap detect output - front end. Must be connected to the demodulator input T3I.

3. Functional Description

The U9280M-H multi-chip module contains a microcontroller and a transponder IC mounted in a single package. Everything necessary for remote control and wireless identification systems is integrated: Inputs to connect keys, outputs to control an IR- or RF transmitter and to drive indicator LEDs, an EEPROM to store key code and identifiers, and an interface for contactless communication and a power supply.

The U3280M is a transponder interface consisting of an analog front end for contactless data communication and power supply, and a serial 512-bit EEPROM. In addition, it includes power management to switch the battery or magnetic-field power supply. For modulation and demodulation of the magnetic field, the device has input and output pins to connect the microcontroller. The MOD, NGAP and FC Pins can be connected externally to the modulator, demodulator and timer I/O pins of the microcontroller. Access to the EEPROM is possible via a two-wire serial interface. The ATAR092 microcontrollers are equipped with compatible two-wire serial interface to communicate with the U3280M. In the U9280M-H the serial interfaces of the transponder interface and the microcontroller are linked internally.

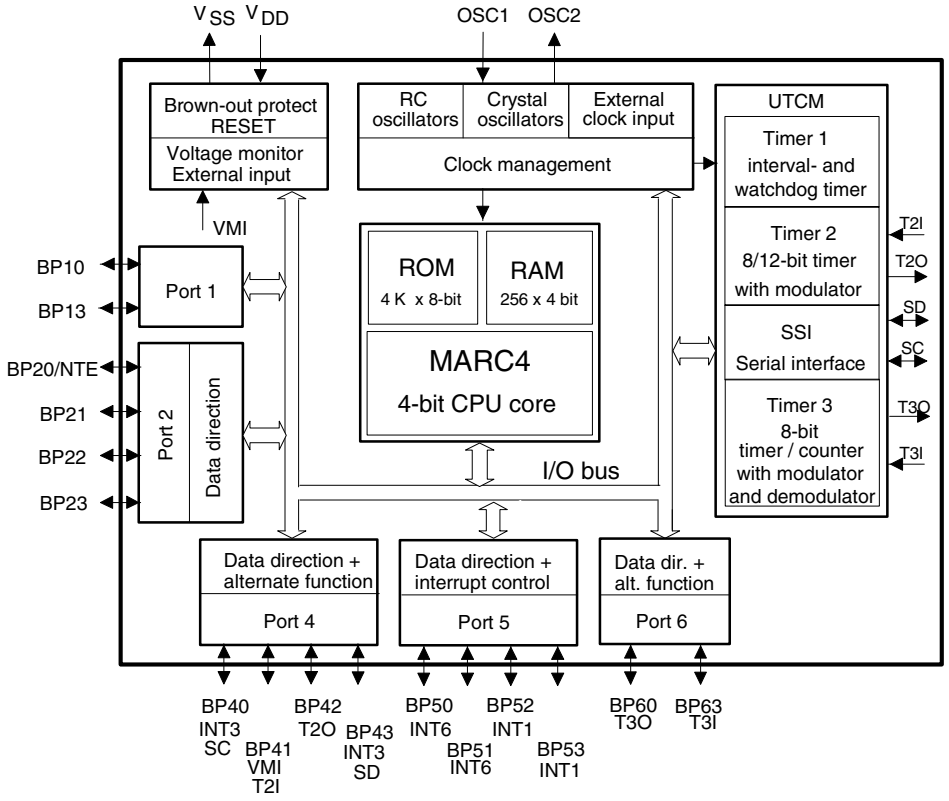
3.1 ATAR092

The ATAR092 microcontroller is a member of the Atmel's 4-bit single-chip microcontroller family. It is especially designed for remote-control applications. It consists of an advanced stack-based 4-bit CPU core with 4K ROM, 256 nibble of RAM and on-chip peripherals. The CPU is based on the HARVARD architecture and contains an interrupt controller with 8 prioritized interrupt levels.

The peripherals include parallel I/O ports, two 8-bit programmable multifunction timer/counters, a two-wire serial interface, an interval timer with watchdog function and a voltage supervisor. The serial interface supports, together with the timers, a modulator and demodulator stage for Manchester, Bi-phase and pulse-width modulation and demodulation. The integrated clock generator contains a RC-, a 32-kHz crystal, a 4-MHz crystal oscillator and a programmable input to use an external clock.

Note: In the U9280M-H not all I/O pins of the ATAR092 are available (see Table 2-1 on page 3). The microcontroller is fully described in the MARC4 ATAR092 data sheet.

Figure 3-1. Block Diagram ATAR092



3.2 The U3280M Transponder Interface

The transponder interface contains a rectifier stage to rectify the AC from the coil inputs and to supply itself and an additional microcontroller device with power from an LC-resonant circuit at the coil inputs. It is also possible to supply the device via the V_{Batt} -input with DC from a battery. The built-in power management switches automatically between battery supply (V_{Batt} pin) and coil supply. It switches to coil supply if a field is applied at the coil and switches back to battery if the field is removed.

The voltage from the coil or the V_{Batt} pin is output at the V_{DD} pin to supply the microcontroller device. At the V_{DD} pin a capacitor must be connected to smooth and buffer the supply voltage for the transponder interface and the microcontroller. This capacitor is also used to buffer the supply voltage during communication (damping and gaps in the field).

For communication, a damping-stage and a gap-detect circuitry is on the chip. By means of the damping stage the coil voltage can be modulated to transmit data via the field. It can be controlled with the modulator input (MOD pin) via the microcontroller. The gap detection circuitry detects gaps in the field and outputs the gap/field signal at the gap detect output (NGAP pin). It can be used to receive data via a modulated field and to check if a field is applied at the coil.

For the storage of data such as key codes, identifiers and configuration bits, a 512-bit EEPROM is available on the chip. It can be read and written to by the microcontroller via a TWI-compatible two-wire serial interface. The serial interface, the EEPROM and the microcontroller are supplied with the voltage at the V_{DD} pin. That means the microcontroller can read and write to the EEPROM if the supply voltage is in the operating range.

The U3280M contains additional operating modes to support a wide range of applications. These modes can be controlled via the serial interface. The power management can be switched off by software to disable the automatic switching between battery and field. This supports applications with battery supply only.

There is an on-chip Bi-phase and Manchester modulator. It can be selected and controlled via the serial interface with a special mode control byte. If this modulator is used the external connection to the modulator input is not necessary.

3.3 Modulation

The transponder interface can modulate the magnetic field by a modulator to transmit data to a base station. It modulates the coil voltage by varying the coil's load. The modulator can be controlled via the MOD pin. A high level 1 increases the current into the coil inputs and damps the coil voltage. A low level 0 decreases the current and increases the coil voltage. The modulator generates a voltage stroke of about 2 V_{pp} at the coil. A high level at the MOD input makes the maximum of the field energy available at V_{DD}. During a reset a high level at the MOD input causes the optimum conditions for starting the device and charging the capacitor at V_{DD} after the field is applied at the coil.

3.3.1 Digital Input to Control the Damping Stage (MOD)

Mod = 0: coil undamped

$$V_{COIL\_peak} = V_{DD} \times \sqrt{2} + V_{CMS} = V_{CU}$$

Mod = 1: coil damped

$$V_{COIL\_peak} = V_{DD} \times \sqrt{2} = V_{CD}$$

$V_{CMS} = V_{CID}$: modulation voltage stroke at coil inputs

Note: If the automatic power management is disabled the internal front end V_{DD} is limited at V_{DDC}. In this case the value V_{DDC} must be used in the formula above.

3.4 Field Clock

The field clock extractor of the interface makes the field clock available for the microcontroller. It can be used to supply timer inputs to synchronize modulation and demodulation with the field clock.

3.5 Gap Detect

The transponder interface can also receive data. The base station modulates the data with short gaps in the field. The gap-detection circuit detects these gaps in the magnetic field and outputs the gap/field signal at the NGAP pin. A high level indicates that a field is applied at the coil and a low level indicates a gap or that the field is off. The microcontroller must demodulate the incoming data stream at one of its inputs.

3.5.1 Digital Output of the Gap Detection Stage (NGAP)

NGAP = 0: gap detected/no field

$$V_{COIL\_peak} = V_{FDOFF}$$

NGAP = 1: field detected

$$V_{COIL\_peak} = V_{FDON}$$

Note: No amplifier is used in the gap detection stage. A digital Schmitt trigger evaluates the rectified and smoothed coil voltage.

3.6 Wake-up Signal

If a field is applied at the coil of the transponder interface the microcontroller can be woken up with the wake signal at the NGAP pin. For that purpose the NGAP pin must be connected to an interrupt input of the microcontroller. A high level at the NGAP output indicates an applied field and can be used as a wake signal for the microcontroller via an interrupt. If no battery voltage is available at V_{Batt} the controller starts with a power-on-reset after the voltage of the buffer capacitor at V_{DD} is loaded by the field above the power-on-reset level.

The wake signal is generated if the power management switches to field supply. The field detection stage of the power management has low-pass characteristics to avoid the generation of wake signals and unnecessary switching between battery and field supply in case of interferences at the coil inputs.

3.7 U3280M Signals and Timing

Figure 3-2. Modulation

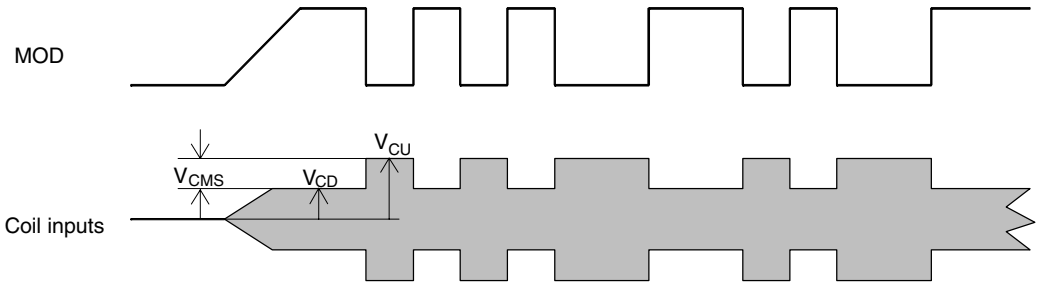
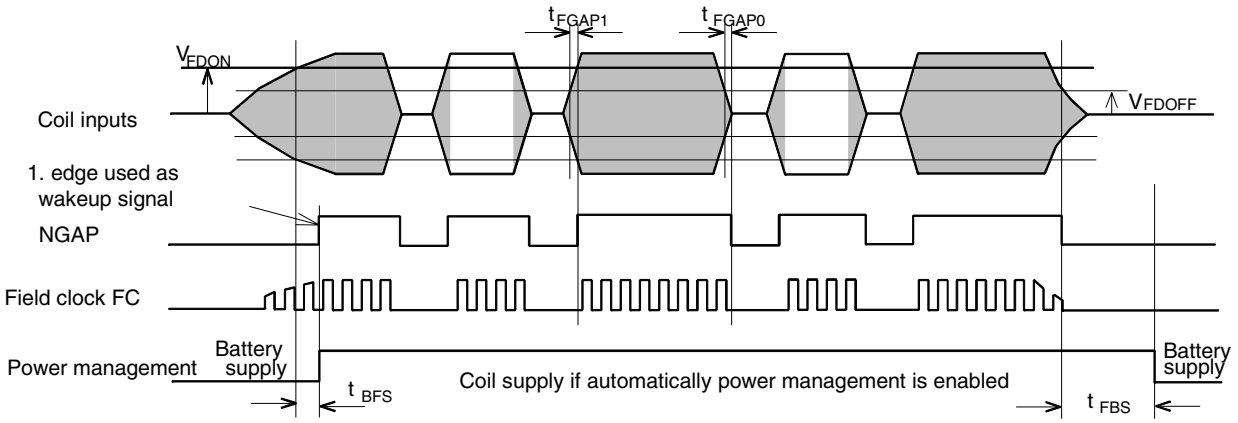


Figure 3-3. Gap Detection and Battery to Field Switching



3.8 Power Supply

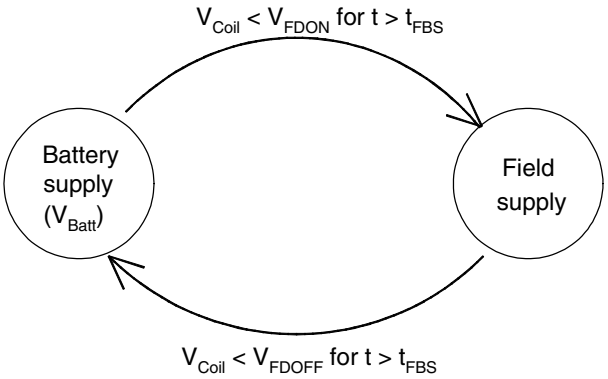
The U3280M has a power management that handles two power-supply sources. Normally, the IC is supplied by a battery at the V_{Batt} pin. If a magnetic field is applied at the LC-resonant circuit of the device the field detection circuit switches from V_{Batt} to field supply. During field supply the V_{DD} voltage is limited to 3V.

The V_{DD} pin is used to connect a capacitor to smooth the voltage from the rectifier and to buffer the power when the field is modulated by gaps and damping. The EEPROM and the microcontroller always operate with the voltage at the V_{DD} pin.

3.8.1 Automatic Power Management

There are different conditions to switch from the battery to field generated voltage and vice versa.

Figure 3-4. Switch Conditions for Power Management



The power management switches automatically from battery to field if the rectified voltage (V_{coil}) from the coil inputs becomes higher than field-on-detection voltage ($V_{FDON)}$ even if no battery voltage is available ($0 < V_{Batt} < 1.8V$). It switches back to battery if the coil voltage becomes lower than the field-off-detection voltage (V_{FDOFF}).

The field-detection stage of the power management has low-pass characteristics to suppress noise. An applied field needs a time delay t_{BFS} (battery-to-field switch delay) to change the power supply. If the field is removed from the coil the power management will generate a reset of the microcontroller.

3.8.2 Controlling Power Management via the Serial Interface

The automatic mode of the power management can be switched off and on by a command from the microcontroller. If the automatic mode is switched off the IC is always supplied by the battery up to the next power-on reset or to a switch-on command. The power management-on and -off command must be transferred via the serial interface.

If the power management is switched off and the device is supplied from the battery it can communicate via the field without loading the field. This mode can be used to realize applications with a battery supply if the available field is too weak to supply the IC with power.

3.8.3 Buffer Capacitor CB

The buffer capacitor connected at V_{DD} is used to buffer the supply voltage for the microcontroller and the EEPROM during field supply. It smooths the rectified AC from the coil and buffers the supply voltage during modulation and gaps in the field. The size of this capacitor depends on the application. It must be of a dimension so that during modulation and gaps the ripple on the supply voltage is in the range of 100 to 300 mV. During gaps and damping the capacitor is used to supply the device, that means the size of the capacitor depends on the length of the gaps and damping cycles.

Example: For a supply current of 350 µA, 200 mV ripple at V_{DD}

Table 3-1. Buffer Capacitor

Time with no Field Supply	Necessary CB
250 µs	470 nF
500 µs	1000 nF

3.9 Serial Interface

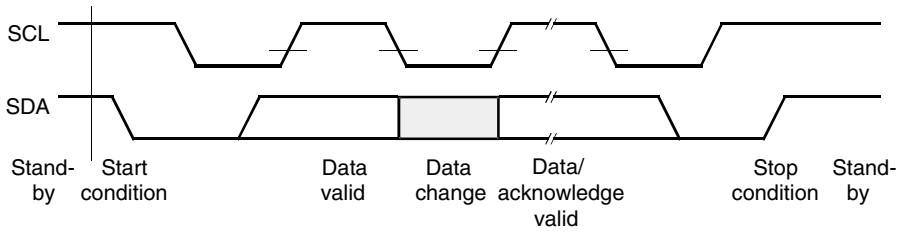
The transponder interface has an serial interface to the microcontroller for read and write accesses to the EEPROM. In a special mode the serial interface can also be used to control the Bi-phase/Manchester modulator or the power management of the U3280M.

The serial interface of the U3280M device must be controlled by a master device (normally the ATAR09x microcontroller) which generates the serial clock and controls the access via the SCL- and SDA-line. SCL is used to clock the data in and out of the device. SDA is a bi-directional line used to transfer data into and out of the device. The following protocol is used for data transfers.

3.9.1 Serial Protocol

- Data states on the SDA line changing only while SCL is low.
- Changes in the SDA line while SCL is high will be interpreted as a START or STOP condition.
- A START condition is defined as a high-to-low transition on the SDA-line while the SCL-line is high.
- A STOP condition is defined as a low-to-high transition on the SDA-line while the SCL-line is high.
- Each data transfer must be initialized with a START condition and terminated with a STOP condition. The START condition wakes the device from standby mode and the STOP condition returns the device to stand-by mode.
- A receiving device generates an acknowledge (A) after the reception of each byte. For that the master device must generate an extra clock pulse. If the reception was successful the receiving master or slave device pulls down the SDA-line during that clock cycle. If in transmit mode an acknowledge is not detected (N) by the interface, it will terminate further data transmissions and will go into receive mode. A master device must finish its read operation by a Not-acknowledge and then issue a stop condition to place the device into a known state.

Figure 3-5. Serial Protocol



3.9.2 Control Byte Format

	EEPROM address					Mode control bits		Read/Write	
Start	A4	A3	A2	A1	A0	C1	C0	R/W	Ackn

The control byte follows the start condition and consists of the 5-bit row address, 2 mode control bits and the read/not write-bit.

3.9.3 Data Transfer Sequence

Start	Control byte	Ackn.	Data byte	Ackn.	Data byte	Ackn.	Stop

- Before the START condition and after the STOP condition the device is in standby mode and the SDA-line is switched to input with a pull-up resistor.
- The START condition follows a control byte that determines the following operation. Bit 0 of the control byte is used to control the following transfer direction. A 0 defines a write access and a 1 a read access.

3.10 EEPROM

The EEPROM has a size of 512 bits and is organized as a 32 × 16-bit matrix. To read and write data to and from the EEPROM the serial interface must be used. The interface supports one and two byte write accesses and one to n-byte read accesses to the EEPROM.

3.10.1 Operating Modes

The operating modes of the EEPROM are defined via the control byte. The control byte contains the row address, the mode control bits and the read/write bit that is used to control the direction of the following transfer. A 0 defines a write access and a 1 a read access. The five address bits select one of the 32 rows of the EEPROM memory to be accessed. For all accesses the complete 16-bit word of the selected row is loaded into a buffer. The buffer must be read or overwritten via the serial interface. The two mode control bits C1 and C2 define in which order the accesses to the buffer are performed: High byte – low byte or low byte – high byte. The EEPROM also supports autoincrement and autodecrement read operations. After sending the start address with the corresponding mode, consecutive memory cells can be read row by row without transmission of the row addresses.

Two special control bytes enable the complete initialization of EEPROM with a 0 or with a 1.

3.10.2 Write Operations

The EEPROM allows 8-bit and 16-bit write operations. A write access starts with the START condition followed by a write control byte and one or two data bytes from the master. It is completed via the STOP condition from the master after the acknowledge cycle.

If the EEPROM receives the control byte, it loads the content of the addressed memory cell into a 16-bit read/write buffer. After the first data byte has been received the EEPROM starts the internal programming cycle. It consists of an erase cycle (write “zeros”) and the write cycle (write “ones”). Each cycle takes about 10 ms. The write cycle is started after the stop condition and the complete buffer is stored back automatically to the EEPROM. That means for two-byte write operations, the second byte must be transferred within the erase cycle otherwise only the first byte will be stored in the EEPROM and the second byte will be ignored.

3.10.3 Acknowledge Polling

If the EEPROM is busy with an internal write cycle, all inputs are disabled and the EEPROM will not acknowledge until the write cycle is finished. This can be used to detect the end of the write cycle. The master must perform acknowledge polling by sending a start condition followed by the control byte. If the device is still busy with the write cycle, it will not return an acknowledge and the master has to generate a stop condition or perform further acknowledge polling sequences. If the cycle is complete, it returns an acknowledge and the master can proceed with the next read or write cycle.

Write One Data Byte

Start	Control byte	A	Data byte 1	A	Stop

Write Two Data Bytes

Start	Control byte	A	Data byte 1	A	Data byte 2	A	Stop

Write Control Byte Only

Start	Control byte	A	Stop

Note: A = acknowledge

3.10.4 Write Control Bytes

	MSB							LSB
Write low byte first	A4	A3	A2	A1	A0	C1	C0	R/W
	Row address					0	1	0

Byte order	LB(R)	HB(R)

	MSB							LSB
Write high byte first	A4	A3	A2	A1	A0	C1	C0	R/W
	Row address					1	0	0

Byte order	HB(R)	LB(R)

Note: HB: high byte; LB: low byte; R: row address

3.10.5 Read Operations

The EEPROM allows byte-, word- and current address read operations. The read operations are initiated in the same way as write operations. Every read access is initiated by sending the START condition followed by the control byte which contains the address and the read mode. After the device receives a read command it returns an acknowledge, loads the addressed word into the read/write buffer and sends the selected data byte to the master. The master has to acknowledge the received byte if it wants to proceed with the read operation. If two bytes are read out from the buffer the device increments respectively, decrements the word address automatically and loads the buffer with the next word. The read mode bits determines if the low or high byte is read first from the buffer and if the word address is incremented or decremented for the next read access. If the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The master can terminate the read operation after every byte by not responding with an acknowledge (N) and by issuing a stop condition.

Read One Data Byte

Start	Control byte	A	Data byte 1	N	Stop

Read Two Data Bytes

Start	Control byte	A	Data byte 1	A	Data byte 2	N	Stop

Read n Data Bytes

Start	Control byte	A	Data byte 1	A	Data byte 2	A	–	Data byte n	N	Stop

Note: A -> acknowledge, N -> no acknowledge

3.10.6 Read Control Bytes

Read low byte first, address increment

MSB							LSB
A4	A3	A2	A1	A0	C1	C0	R/W
Row address					0	1	1

Byte order	LB(R)	HB(R)	LB(R+1)	HB(R+1)	–	LB(R+n)	HB(R+n)

Read high byte first, address decrement

MSB							LSB
A4	A3	A2	A1	A0	C1	C0	R/W
Row address					1	0	1

Byte order	HB(R)	LB(R)	HB(R-1)	LB(R-1)	–	HB(R-n)	LB(R-n)

Note: HB: high byte; LB: low byte, R: row address

3.10.7 Initialization after a Reset Condition

The EEPROM with the serial interface has its own reset circuitry. In systems with microcontrollers that have their own reset circuitry for power-on reset, watchdog reset or brown-out reset, it may be necessary to bring the EEPROM into a known state independent of its internal reset. This is performed by reading one byte without acknowledging and then generating a stop condition.

3.10.8 Special Modes

By means of special control bytes, the serial interface can be used to control the modulator stage or power management. The EEPROM access and the serial interface are disabled in these modes until the next STOP condition. If no START or STOP condition is generated, the SCL and SDA line can be used for the modulator stage. SCL is used for the modulator clock and SDA is used for the data. In that mode, the same conditions for clock and data changing normally are valid. The SCL and SDA line can be used for continuous bit transfers, an acknowledge cycle after 8 bits must not be generated.

Table 3-2. Special Modes

Control Byte	Description
1100x111b	Bi-phase modulation
1101x111b	Manchester modulation
11xx0111b	Switch power management off: disables switching from battery to field supply
11xx1111b	Switch power management on: enables automatically switching between battery and field supply
xxxxx110b	Reserved

3.10.9 Data Transfer Sequence for Bi-phase and Manchester Modulation:

Start	Control byte	Ackn	Bit 1	Bit 2	Bit 3	...	Bit n	Stop

Note: After a reset of the microcontroller, it is not known if the transponder interface has been reset, too. It could still be in a receive or transmit cycle. To place the serial interface of the device into a known state, the microcontroller should read one byte from the device without acknowledge and generate a stop condition.

3.11 Power-on Reset

The analog front end starts working with the applied field. The EEPROM with the serial interface has its own reset circuitry. (The reset level of the front end is below the reset level of the ATAR092)

The microcontroller has a power-on reset circuitry with a brown-out detection. One of two reset voltage levels [1.8V/2.0V] can be selected via the software (see the ATAR092 data sheet). If a fast instruction cycle (< 2 µs) is used the higher reset level should be selected.

After a watchdog or brown-out detection reset, the serial interface and the EEPROM should be reset by reading one byte from the transponder interface device without acknowledging and generation of a STOP condition. That places the serial interface and EEPROM into a known state.

4. Electrical Characteristics – Common Features U9280M-H

- Operating Temperature Range: –40° C to +85° C
- Operating Voltage Range (V_{Batt}): 2.0V to 6.5V
  - – Low Power Consumption:
  - – 600 µA at 6.5V in Operating Mode (with 2 µs Instruction Cycle)
  - – 200 µA at 2.0V in Operating Mode (with 2 µs Instruction Cycle)
  - – 1 µA at 2.0V in Stop Mode
- Power Supply: Contactless (Coil 125 kHz) and Battery Supply

5. Absolute Maximum Ratings

Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating condition for an extended period may affect device reliability. All inputs and outputs are protected against high electrostatic voltages or electric fields. However, precautions to minimize the build-up of electrostatic charges during handling are recommended. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., V_{DD}).

Voltages are given relative to V_{SS}

Parameters	Symbol	Value	Unit
Supply voltage	V_{Batt}, V_{DD}	0 to +7 with reverse protection	V
Maximum current out of the V_{SS} pin		15	mA
Maximum current out of the V_{Batt} pin		15	mA
Input voltage (on any pin)	V_{IN}	$V_{SS} - 0.6 < V_{IN} < V_{DD} + 0.6$	V
Input/output clamp current ($V_{SS} > V_i/V_o > V_{DD}$)	I_{IK}/IOK	±15	mA
Minimum ESD protection (100 pF through 1.5 kΩ)		±2	kV
Minimum ESD protection Coil 1 and Coil 2 inputs (100 pF through 1.5 kΩ)		±1	kV
Operating temperature range	T_{amb}	–40 to +85	°C
Storage temperature range	T_{stg}	–40 to +125	°C
Soldering temperature ($t \leq 10s$)	T_{sd}	260	°C

6. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO20	R_{thJA}	140	K/W

7. Common DC Characteristics

V_{SS} = 0V, T_{amb} = –40°C to +85°C unless otherwise specified

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
Power Supply						
Operating voltage at V_{Batt}		V_{Batt}	2.0		6.5	V
Operating voltage at V_{DD}		V_{DD}	V_{POR}		6.5	V
Active current CPU active	f_{SYSCL} = 1 MHz					
	V_{DD} = 2.0V	I_{DD}		200	250	µA
	V_{DD} = 3.0V			300		µA
	V_{DD} = 6.5V			600	800	µA
Power down current (CPU sleep, RC oscillator active, 4-MHz quartz oscillator active)	f_{SYSCL} = 1 MHz			1.0		
	V_{DD} = 2.0V	I_{PD}		40	70	µA
	V_{DD} = 3.0V			100		µA
	V_{DD} = 6.5V			250	400	µA
Sleep current (CPU sleep, 32-kHz quartz-oscillator inactive 4-MHz quartz-oscillator inactive)	V_{DD} = 6.5V	I_{Sleep}		1.0	2.0	µA
Reset current	$V_{DD} < V_{POR}$	I_{Reset}		150		µA

8. DC Characteristics – Microcontroller ATAR092

V_{SS} = 0V, T_{amb} = –40°C to +85°C unless otherwise specified

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
Brown-out Protection Reset Threshold Voltage						
Reset threshold voltage	BOT = 1	V_{POR}	155	1.7	1.85	V
Reset threshold voltage	BOT = 0	V_{POR}	1.85	2.0	2.2	V
Reset hysteresis		V_{POR}		50		mV
Voltage Monitor Threshold Voltage						
VM high threshold voltage	V_{DD} > VM, VMS = 1	V_{MThh}		3.0	3.25	V
VM high threshold voltage	V_{DD} < VM, VMS = 0	V_{MThh}	2.8	3.0		V
VM middle threshold voltage	V_{DD} > VM, VMS = 1	V_{MThm}		2.6	2.8	V
VM middle threshold voltage	V_{DD} < VM, VMS = 0	V_{MThm}	2.4	2.6		V
VM low threshold voltage	V_{DD} > VM, VMS = 1	V_{MThl}		2.2	2.4	V
VM low threshold voltage	V_{DD} < VM, VMS = 0	V_{MThl}	2.0	2.2		V
External Input Voltage						
VMI rising edge threshold	VMS = 1, V_{DD} = 3V	V_{VMI}		1.3	1.4	V
VMI falling edge threshold	VMS = 0, V_{DD} = 3V	V_{VMI}	1.2	1.3		V

8. DC Characteristics – Microcontroller ATAR092 (Continued)

V_{SS} = 0V, T_{amb} = –40°C to +85°C unless otherwise specified

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
All Bi-directional Ports						
Input voltage LOW	V_{DD} = 1.8V to 6.5V	V_{IL}	V_{SS}		$0.2 \times V_{DD}$	V
Input voltage HIGH	V_{DD} = 1.8V to 6.5V	V_{IH}	$0.8 \times V_{DD}$		V_{DD}	V
Input LOW current (pull-up)	V_{DD} = 2.0V, V_{DD} = 3.0V, V_{IL}= V_{SS} V_{DD} = 6.5V	I_{IL}	–2.0 –50	–4.0 –20 –100	–12 –200	µA µA µA
Input HIGH current (pull-down)	V_{DD} = 2.0V, V_{DD} = 3.0V, V_{IH} = V_{DD} V_{DD} = 6.5V	I_{IH}	2.0 50	4.0 20 100	12 200	µA µA µA
Input LOW current (strong pull-up)	V_{DD} = 2.0V, V_{IL}= V_{SS} V_{DD} = 6.5V	I_{IL}	–20 –300	–50 –600	–100 –1200	µA µA
Input LOW current (strong pull-down)	V_{DD} = 2.0V, V_{IH} = V_{DD} V_{DD} = 6.5V	I_{IH}	20 300	50 600	100 1200	µA µA
Input leakage current	V_{IL}= V_{SS}	I_{IL}			100	nA
Input leakage current	V_{IH}= V_{DD}	I_{IH}			100	nA
Output LOW current	V_{OL} = 0.2 V_{DD} V_{DD} = 2.0V V_{DD} = 3.0V, V_{DD} = 6.5V	I_{OL}	 0.6 8	 1.2 5 15	 2.5 22	 mA mA mA
Output HIGH current	V_{OH} = 0.8 V_{DD} V_{DD} = 2.0V V_{DD} = 3.0V, V_{DD} = 6.5V	I_{OH}	 –0.6 –8	 –1.2 –5 –16	 –2.5 –24	 mA mA mA

Note: The BP20/NTE pin has a strong pull-up resistor during the reset-phase of the microcontroller.

9. AC Characteristics – Operation Cycle Time

Supply voltage V_{DD} = 1.8V to 6.5V, V_{SS} = 0V, T_{amb} = –40°C to +85°C unless otherwise specified

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
System clock cycle	V_{DD} = 1.8V to 6.5V T_{amb} = –40°C to +85°C	t_{SYSCL}	500		2000	ns
	V_{DD} = 2.4V to 6.5V T_{amb} = –40°C to +85°C	t_{SYSCL}	250		2000	ns
Timer 2 Input Timing Pin T2I						
Timer 2 input clock		f_{T2I}			5	MHz
Timer 2 input LOW time		t_{T2IL}	100			ns
Timer 2 input HIGH time		t_{T2IH}	100			ns
Timer 3 Input Timing Pin T3I						
Timer 3 input clock		f_{T3I}			SYSCL/2	
Timer 3 input LOW time		t_{T3IL}	$2 \times t_{SYSCL}$			ns
Timer 3 input HIGH time		t_{T3IH}	$2 \times t_{SYSCL}$			ns
Interrupt Request Input Timing						
Interrupt request LOW time		t_{IRL}	100			ns
Interrupt request HIGH time		t_{IRH}	100			ns
External System Clock						
EXSCL at OSC1	ECM = EN Rise/fall time < 10 ns	f_{EXSCL}	0.5		4	MHz
EXSCL at OSC1	ECM = DI Rise/fall time < 10 ns	f_{EXSCL}	0.02		4	MHz
Input HIGH time	Rise/fall time < 10 ns	t_{IH}	0.1			µs
Reset Timing						
Power-on reset time	$V_{DD} > V_{POR}$	t_{POR}		1.5	5	ms
RC Oscillator 1						
Frequency		f_{RcOut1}		3.8		MHz
Stability	V_{DD} = 2.0V to 6.5V	$\Delta f/f$			±50	%
Temperature coefficient		$\Delta f/f/°C$		0.15		%
RC Oscillator 2 – External Resistor						
Frequency	R_{ext} = 170 kΩ R_{ext} = 720 kΩ	f_{RcOut2} f_{RcOut2}		4 1		MHz
Stability	V_{DD} = 2.0V to 6.5V	$\Delta f/f$			±15	%
Stabilization time		t_S			10	µs
4-MHz Crystal Oscillator (Operating Range 2.2V to 6.5V)						
Frequency		f_X		4		MHz
Start-up time		t_{SQ}		5		ms
Stability		$\Delta f/f$	–10		+10	ppm
Integrated input/output capacitances (mask programmable)	C_{IN}/C_{OUT} programmable in steps of 2 pF	C_{IN} C_{OUT}	0 0		20 20	pF pF

9. AC Characteristics – Operation Cycle Time (Continued)

Supply voltage V_{DD} = 1.8V to 6.5V, V_{SS} = 0V, T_{amb} = –40°C to +85°C unless otherwise specified

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
32-kHz Crystal Oscillator (Operating Range 2.0V to 6.5V)						
Frequency		f_X		32.768		kHz
Start-up time		t_{SQ}		0.5		s
Stability		$\Delta f/f$	–10		+10	ppm
Integrated input/output capacitances (mask programmable)	C_{IN}/C_{OUT} programmable in steps of 2 pF	C_{IN} C_{OUT}	0 0		20 20	pF pF
External 32-kHz Crystal Parameters						
Crystal frequency		f_X		32.768		kHz
Serial resistance		RS		30	50	kΩ
Static capacitance		C0		1.5		pF
Dynamic capacitance		C1		3		fF
External 4 MHz Crystal Parameters						
Crystal frequency		f_X		4.0		MHz
Serial resistance		RS		40	150	Ω
Static capacitance		C0		1.4	3	pF
Dynamic capacitance		C1		3		fF

Figure 9-1. Crystal and Equivalent Circuit

10. DC Characteristics –Transponder Interface U3280M

Supply voltage V_{DD} = 1.8V to 6.5V, V_{SS} = 0V, T_{amb} = –40°C to +85°C unless otherwise specified

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
Power Supply						
Operating voltage at V_{Batt}		V_{Batt}	2.0		6.5	V
Operating voltage at V_{DD} during battery supply		V_{DDB}		$V_{Batt} - V_{SD}$		V
V_{DD} limiter voltage during coil supply		V_{DDC}	2.4	2.9	3.2	V
Power Management						
Field on detection voltage	V_{DD} > 1.8V	V_{FDon}	2.2	2.5	2.9	V
Field off detection voltage	V_{DD} > 1.8V	V_{FDoff}		0.8		V
Voltage drop at power-supply switch	I_S = 1 mA, V_{Batt} = 2V	V_{SD}			300	mV
Coil Input Coil 1, Coil 2						
Coil input current		I_{CI}			20	mA
Coil voltage stroke during modulation	V_{CU} > 5V	V_{CMS}	1.8		4.0	V
Input capacitance		C_{IN}		30		pF
MOD Pin						
Input LOW voltage		V_{IL}	V_{SS}		$0.2 \times V_{DD}$	V
Input HIGH voltage		V_{IH}	$0.8 \times V_{DD}$		V_{DD}	V
Input leakage current		I_{lleak}		10		nA
NGAP/FC Pin						
Output LOW current	V_{DD} = 2.0V $V_{OL} = 0.2 \times V_{DD}$	I_{OL}	0.08	0.2	0.3	mA
Output HIGH current	V_{DD} = 2.0V $V_{OH} = 0.8 \times V_{DD}$	I_{OH}	–0.06	–0.15	–0.25	mA
EEPROM						
Operating current during erase/write cycle	V_{DD} = 2V	I_{WR}			450	µA

11. AC Characteristics – Transponder Interface U3280M

Supply voltage V_{DD} = 1.8V to 6.5V, V_{SS} = 0V, T_{amb} = –40°C to +85°C unless otherwise specified

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Serial Interface Timing (Internal)						
SCL clock frequency (intern)		f_{SC}			500	kHz
Serial Timing (if SCL and SDA Available Extern)						
SCL clock frequency (extern)		f_{SCL}	0		100	kHz
Clock low time		t_{LOW}	4.7			µs
Clock high time		t_{HIGH}	4.0			µs
SDA and SCL rise time		t_R			1000	ns
SDA and SCL fall time		t_F			300	ns
Start condition setup time		t_{SUSTA}	4.7			µs
Start condition hold time		t_{HDSTA}	4.0			µs
Data input setup time		t_{SUDAT}	250			ns
Data input hold time		t_{HDDAT}	0			ns
Stop condition setup time		t_{SUSTO}	4.7			µs
Bus free time		t_{BUF}	4.7			µs
Input filter time		t_I			100	ns
Data output hold time		t_{DH}	300		1000	ns
Coil Inputs						
Coil frequency		f_{COIL}		125		kHz
Gap Detection						
Delay field off to gap = 0	$V_{CoilGap} < 0.7\ V_{DC}$	t_{FGAP0}	10		50	µs
Delay field on to gap = 1	$V_{CoilField} > 3\ V_{DC}$	t_{FGAP1}	1		10	µs
Power Management						
Battery to field switch delay		t_{BFS}	160		650	µs
Field to battery switch delay		t_{FBS}		10	60	ms
EEPROM						
Endurance	Erase/write-cycles	ED	500,000	1,000,000		E/W-cycles
Data erase/write cycle time	for 16 bits access	t_{DEW}		9	12	ms
Data erase time		t_{DE}	2		$1/2 \times t_{DEW}$	ms
Data retention time	T_{amb} = 25°C	t_{DR}	10			years
Power-up to read operation		t_{PUR}			0.2	ms
Power-up to write operation		t_{PUW}			0.2	ms

12. Ordering Information

Please select the option settings from the list below and insert in ROM CRC.

	Output	Input
Port 1		
BP10	[X] CMOS	[X] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong
BP13	[X] CMOS	[X] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong
Port 2		
BP20	[ ] CMOS	[ ] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
BP21	[X] CMOS	[X] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong
BP22	[X] CMOS	[X] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong
BP23	[ ] CMOS	[ ] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong
Port 4		
BP40	[ ] CMOS	[ ] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong
BP41	[ ] CMOS	[ ] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong
BP42	[ ] CMOS	[ ] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong
BP43	[ ] CMOS	[ ] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong

	Output	Input
Port 5		
BP50	[ ] CMOS	[ ] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong
BP51	[X] CMOS	[X] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong
BP52	[X] CMOS	[X] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong
BP53	[ ] CMOS	[ ] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong
Port 6		
BP60	[ ] CMOS	[ ] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong
BP63	[ ] CMOS	[ ] Pull-up
	[ ] Open drain [N]	[ ] Pull-down
	[ ] Open drain [P]	[ ] Pull-up strong
		[ ] Pull-down strong

OSC1	
	[ ] No integrated capacitance
	[ ] Internal capacitance [_____pF]
OSC2	
	[ ] No integrated capacitance
	[ ] Internal capacitance [_____pF]

ECM (External Clock Monitor)	
	[ ] Enable
	[ ] Disable

File: _____ . HEX CRC: _____ . HEX

Aproval Date: _____ Signature: _____

13. Ordering Information (Continued)

Extended Type Number	Package	Remarks
U9280M-H-xxxz-FSG3Y	SSO20	> 200 kpcs annually taped and reeled, Pb-free

13.1 Customer ROM mask

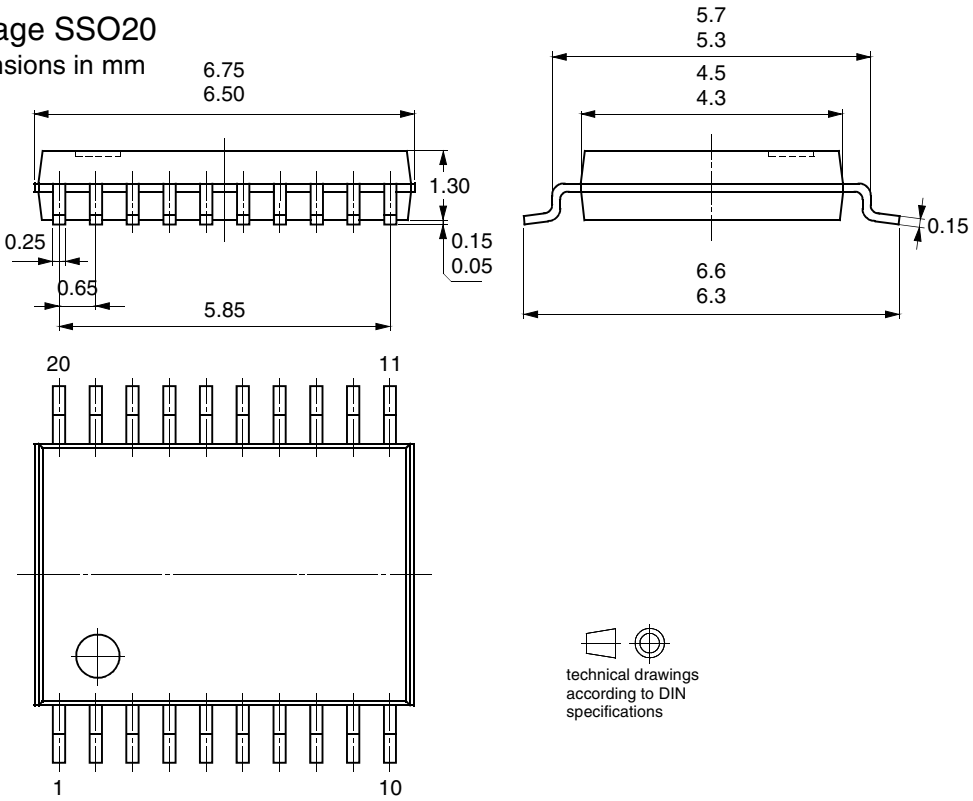
- To be defined by the customer
- Lead time: 18 weeks after ROM mask programming and reception of the order

13.2 Flash Version

As flash version of the U9280M-H the MARC4 ATAR892 is used (available from stock).

14. Package Information

Package SSO20
Dimensions in mm



15. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4591B-RFID-09/05	• Put datasheet in a new template • Pb-free Logo on page 1 added • Ordering Information on page 23 changed

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