TFT LCD Tentative Specification

MODEL NO.: V470K1 - L01

Customer: _____

Approved by: _____

Note:

Approved By	TV Head Division
	LY Chen

Reviewed By	QRA Dept.	Product Development Div.
	Tomy Chen	WT Lin

Prepared By	LCD TV Marketing and Product Management Div.	
	Ken Wu	Marcus Chang

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver. 0.0	Jan.4,'07	All	All	Tentative Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V470K1-L01 is a 47" TFT Liquid Crystal Display module with 24-CCFL Backlight unit and 4ch-LVDS interface. This module supports 2560 x 1440 QFHD format and can display true 16.7M colors (8-bit/color). The inverter module for backlight is built-in.

1.2 FEATURES

- High brightness (450 nits)
- High contrast ratio (1500:1), Dynamic contrast x 4
- Fast response time (Gray to gray average 6.5ms)
- High color saturation (NTSC 92%)
- QHDTV (2560 x 1440 pixels) resolution, future TV format
- LVDS (Low Voltage Differential Signaling) interface
- Ultra wide viewing angle: LCS MVA technology
- RoHS compliance

1.3 APPLICATION

- High-end Living Room TVs.
- Digital Home TVs
- Public Display Application.
- Home Theater Application.
- High level Application.(Medical,movie,3D….)

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	1040.64(H) x 585.36(V) (47" diagonal)	mm	(1)
Bezel Opening Area	1050.6(H) x 594.4(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	2560x R.G.B. x 1440	pixel	-
Pixel Pitch	0.4065 (H) x 0.4065(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	HC+LR coating	-	(2)

Note (1) Please refer to the attached drawings in chapter 11 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	1095	1096	1097	mm	(1), (2)
	Vertical (V)	639	640	641	mm	
	Depth (D)	47.1	48.1	49.1	mm	
Weight			18500		g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol		Value		Unit	Note
			Min.	Max.		
Storage Temperature	T_{ST}		-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}		0	45	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	X, Y axis	-	50	G	(3), (5)
		Z axis	-	35	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}		-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

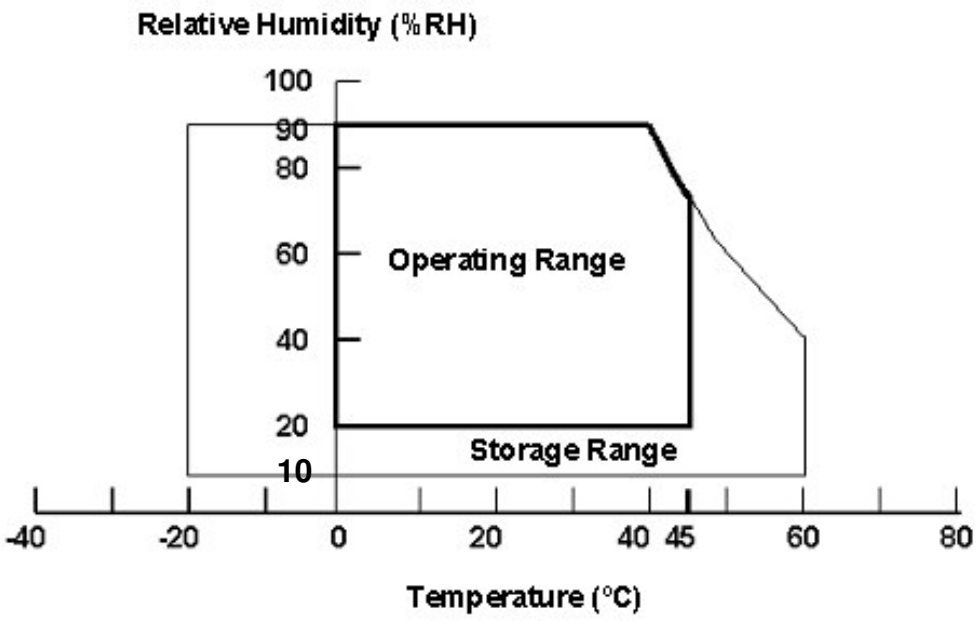
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, and ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture. The module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.2	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	5000	V_{RMS}	
Power Supply Voltage	V_{BL}	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control, Internal PWM Control, External PWM Control and Internal/External PWM Selection.

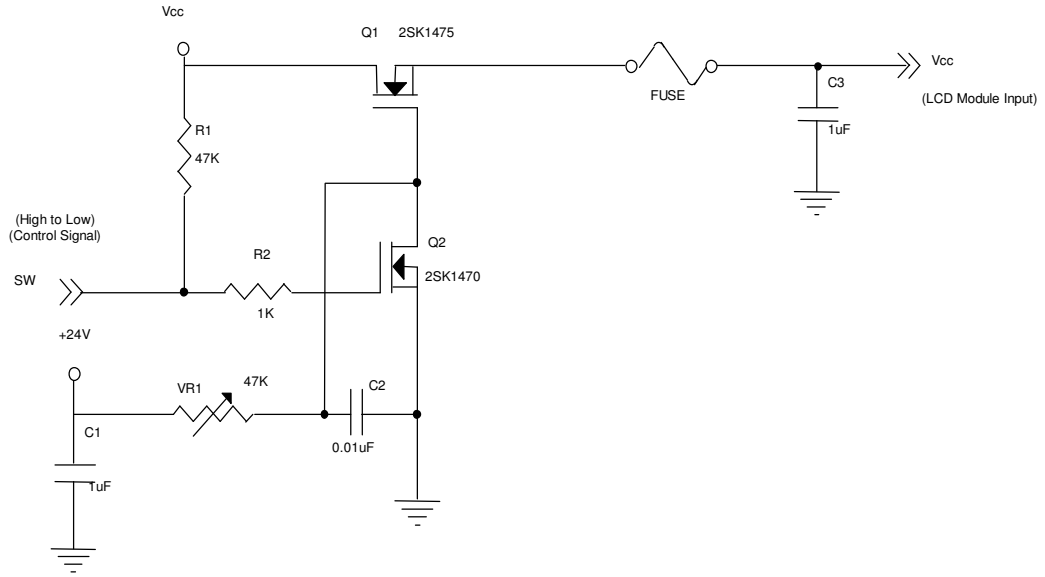
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE (Ta = 25 ± 2 ºC)

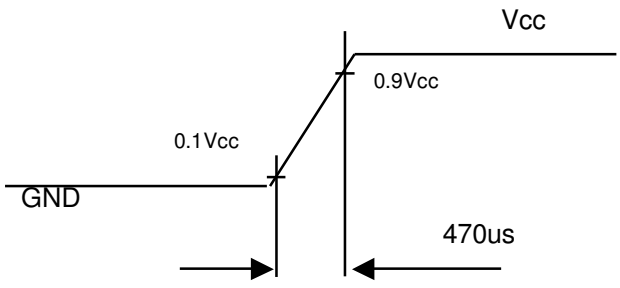
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Power Supply Ripple Voltage		V_{RP}	-	-	300	mV	
Rush Current		I_{RUSH}	-	-	3.0	A	(2)
Power Supply Current	White	-		1.6	2.2	A	
	Black	-		0.7		A	
	Vertical Stripe	-		1.3		A	(3)
LVDS Interface	Differential Input High Threshold Voltage	V_{LVTH}	-	-	100	mV	
	Differential Input Low Threshold Voltage	V_{LVTL}	-100	-	-	mV	
	Common Input Voltage	V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

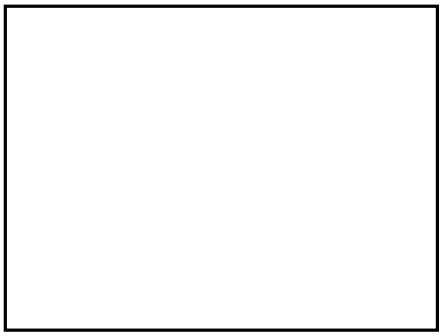


Vcc rising time is 470us



Note (3)&(4) The specified power supply current is under the conditions at Vcc = 18 V(Note(3)), Vcc = 12V(Note(4)), Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

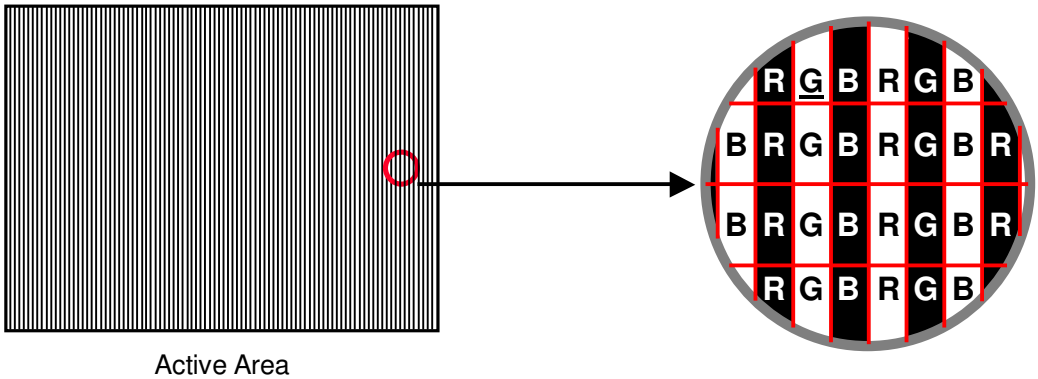


Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT UNIT

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	-	1530	-	V_{RMS}	-
Lamp Current	I_L	5.3	5.8	6.3	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	2350	V_{RMS}	(2), Ta = 0 ºC
		-	-	2150	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_L	40	-	80	KHz	(3)
Lamp Life Time	L_{BL}	50,000	-	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	211	221	W	(5), I_L = 5.8mA
Power Supply Voltage	V_{BL}	22.8	24	25.2	V_{DC}	
Power Supply Current	I_{BL}	-	8.8		A	Non Dimming
Input Ripple Noise	-	-	-	912	mV_{P-P}	V_{BL}=22.8V
Backlight Turn on Voltage	V_{BS}	2350	-	-	V_{RMS}	Ta = 0 ºC
		2150	-	-	V_{RMS}	Ta = 25 ºC
Oscillating Frequency	F_W	44	47	50	kHz	
Dimming frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	-	20	-	%	

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.:

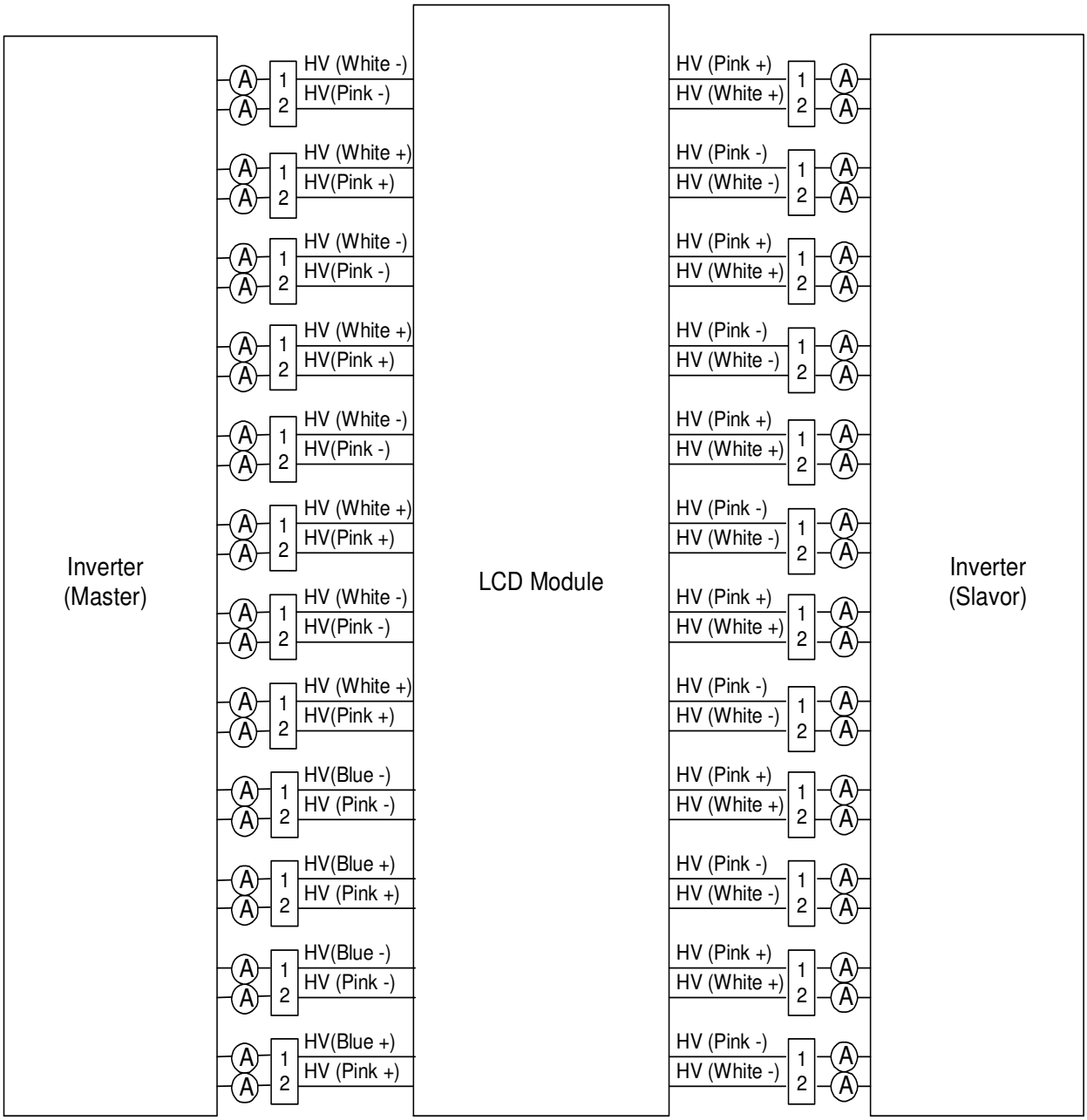
Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and I_L = 5 ~ 6 mArms.

Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6) The measurement condition of Max. value is based on 47" backlight unit under input voltage 24V, average lamp current 5.8 mA and lighting 30 minutes later.


Inverter (Master)
LCD Module
Inverter (Slavor)
HV (White -)
HV(Pink -)
HV (White +)
HV(Pink +)
HV(Blue -)
HV (Pink -)
HV(Blue +)
HV (Pink +)
A
1
2

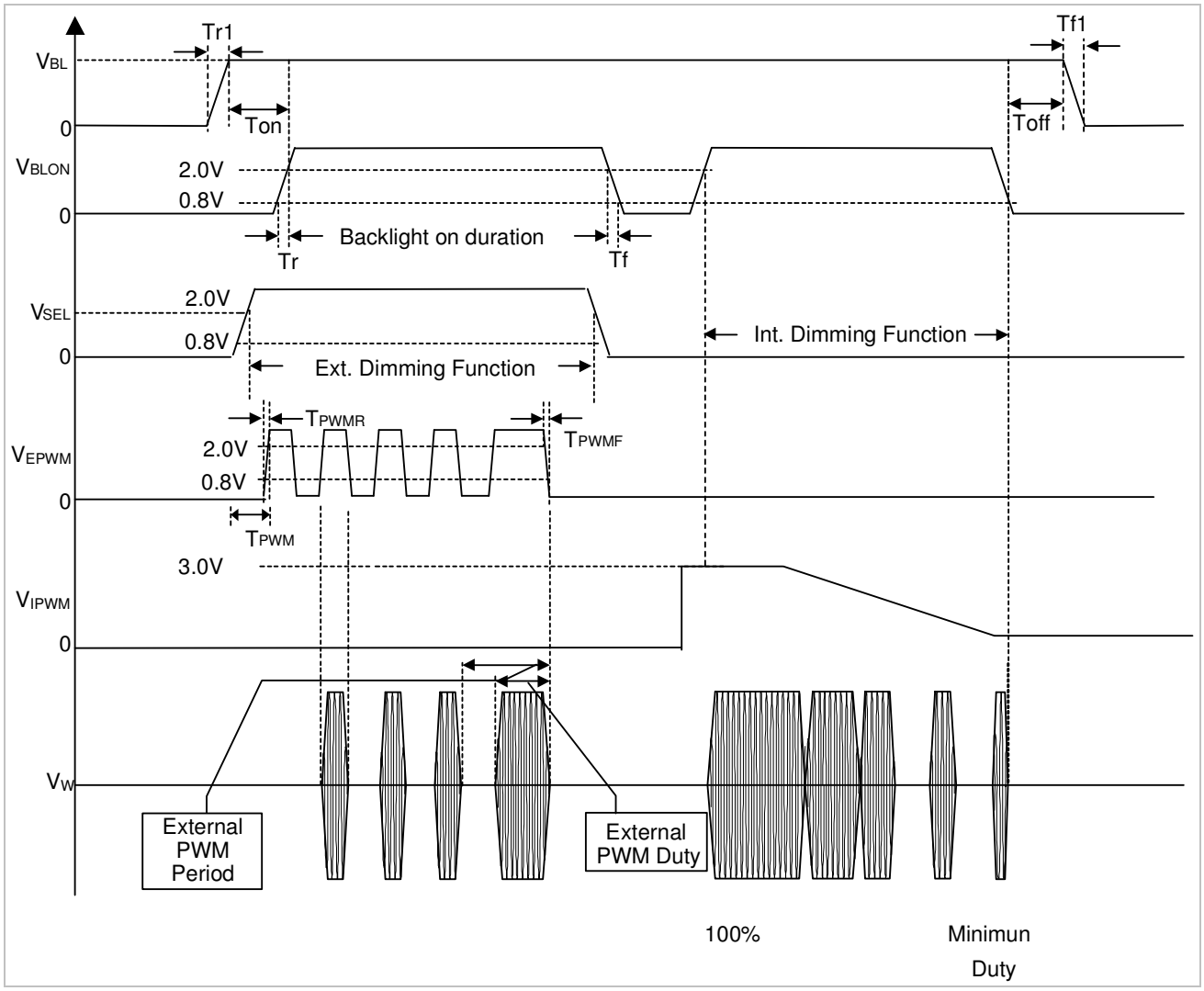
3.2.3 INVERTER INTERTFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal/External PWM Select Voltage	HI	V_{SEL}	—	2.0	—-	5.0	V	
	LO		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	V_{SEL} = L	—	—	3.0	V	maximum duty ratio
	MIN			—	0	—	V	minimum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	V_{SEL} = H	2.0	—	5.0	V	duty on
	LO			0	—	0.8	V	duty off
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
VBL Rising Time		Tr1	—	30	—	50	ms	
VBL Falling Time		Tf1	—	30	—	50	ms	
PWM Delay Time		T_{PWM}	—	100	—	300	mS	
Input impedance		R_{IN}	—	1	—	—	MΩ	
BLON Delay Time		T_{on}	—	1	—	—	ms	
BLON Off Time		T_{off}	—	1	—	—	ms	

Note (1) The SEL signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM selection (SEL) during backlight turn on period.

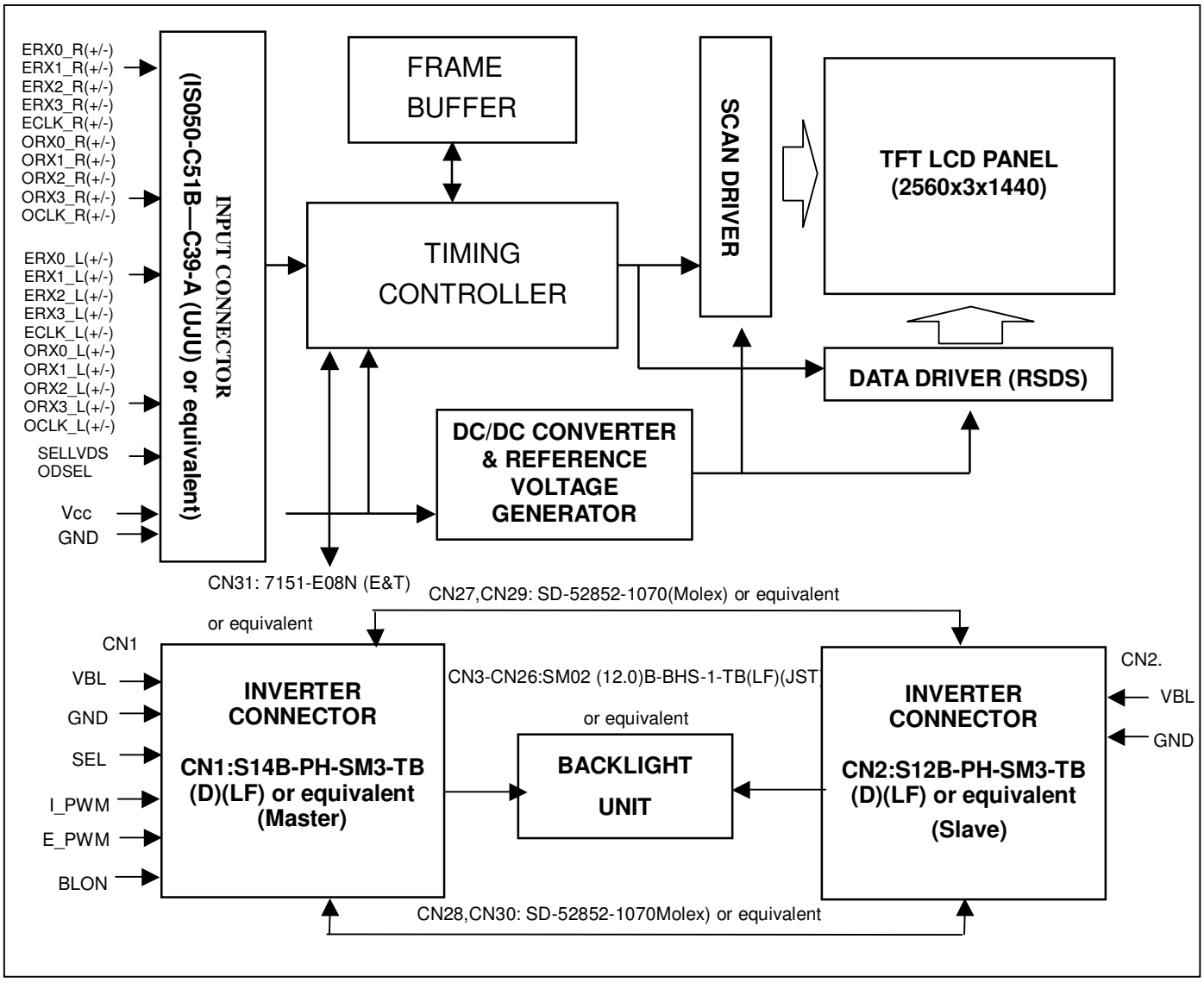
Note (2) The power sequence and control signal timing are shown in the following figure.

Note (3) The power sequence and control signal timing must follow the figure below. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.


Tr1
Tf1
VBL
0
Ton
Toff
VBLON
2.0V
0.8V
0
Backlight on duration
Tr
Tf
VSEL
2.0V
0.8V
0
Int. Dimming Function
Ext. Dimming Function
TPWMR
TPWMF
VEPWM
2.0V
0.8V
0
TPWM
3.0V
VIPWM
0
VW
External PWM Period
External PWM Duty
100%
Minimun Duty

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module

CNF1

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	SELLVDS	LVDS data format Selection	(2)
8	N.C.	No Connection	(1)
9	ODSEL	Overdrive Lookup Table Selection	(3)
10	N.C.	No Connection	(1)
11	GND	Ground	
12	ORX0_L-	Odd pixel Negative LVDS differential data input. Channel 0	(4)
13	ORX0_L+	Odd pixel Positive LVDS differential data input. Channel 0	
14	ORX1_L-	Odd pixel Negative LVDS differential data input. Channel 1	
15	ORX1_L+	Odd pixel Positive LVDS differential data input. Channel 1	
16	ORX2_L-	Odd pixel Negative LVDS differential data input. Channel 2	
17	ORX2_L+	Odd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK_L-	Odd pixel Negative LVDS differential clock input.	(4)
20	OCLK_L+	Odd pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ORX3_L-	Odd pixel Negative LVDS differential data input. Channel 3	(4)
23	ORX3_L+	Odd pixel Positive LVDS differential data input. Channel 3	
24	GND	Ground	
25	N.C.	No Connection	(1)
26	GND	Ground	
27	GND	Ground	
28	ERX0_L-	Even pixel Negative LVDS differential data input. Channel 0	(4)
29	ERX0_L+	Even pixel Positive LVDS differential data input. Channel 0	
30	ERX1_L-	Even pixel Negative LVDS differential data input. Channel 1	
31	ERX1_L+	Even pixel Positive LVDS differential data input. Channel 1	
32	ERX2_L-	Even pixel Negative LVDS differential data input. Channel 2	
33	ERX2_L+	Even pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK_L-	Even pixel Negative LVDS differential clock input.	(4)
36	ECLK_L+	Even pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	ERX3_L-	Even pixel Negative LVDS differential data input. Channel 3	(4)
39	ERX3_L+	Even pixel Positive LVDS differential data input. Channel 3	
40	GND	Ground	
41	N.C.	No Connection	(1)
42	GND	Ground	
43	GND	Ground	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	

47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

CNF2

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	N.C.	No Connection	
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	ORX0_R-	Odd pixel Negative LVDS differential data input. Channel 0	(5)
13	ORX0_R+	Odd pixel Positive LVDS differential data input. Channel 0	
14	ORX1_R-	Odd pixel Negative LVDS differential data input. Channel 1	
15	ORX1_R+	Odd pixel Positive LVDS differential data input. Channel 1	
16	ORX2_R-	Odd pixel Negative LVDS differential data input. Channel 2	
17	ORX2_R+	Odd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK_R-	Odd pixel Negative LVDS differential clock input.	(5)
20	OCLK_R+	Odd pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ORX3_R-	Odd pixel Negative LVDS differential data input. Channel 3	(5)
23	ORX3_R+	Odd pixel Positive LVDS differential data input. Channel 3	
24	GND	Ground	
25	N.C.	No Connection	(1)
26	GND	Ground	
27	GND	Ground	
28	ERX0_R-	Even pixel Negative LVDS differential data input. Channel 0	(5)
29	ERX0_R+	Even pixel Positive LVDS differential data input. Channel 0	
30	ERX1_R-	Even pixel Negative LVDS differential data input. Channel 1	
31	ERX1_R+	Even pixel Positive LVDS differential data input. Channel 1	
32	ERX2_R-	Even pixel Negative LVDS differential data input. Channel 2	
33	ERX2_R+	Even pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK_R-	Even pixel Negative LVDS differential clock input.	(5)
36	ECLK_R+	Even pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	ERX3_R-	Even pixel Negative LVDS differential data input. Channel 3	(5)
39	ERX3_R+	Even pixel Positive LVDS differential data input. Channel 3	
40	GND	Ground	
41	N.C.	No Connection	(1)
42	GND	Ground	
43	GND	Ground	

44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	N.C.	No Connection	
49	N.C.	No Connection	
50	N.C.	No Connection	
51	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) Low : VESA LVDS Format (default), High : JEIDA Format.

Note (3) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

ODSEL	Note
L	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

Note (4) Left side image signal input.

Note (5) Right side image signal input.

Note (6) Connector part no. : IS050-C51B—C39-A (UJU) or equivalent.

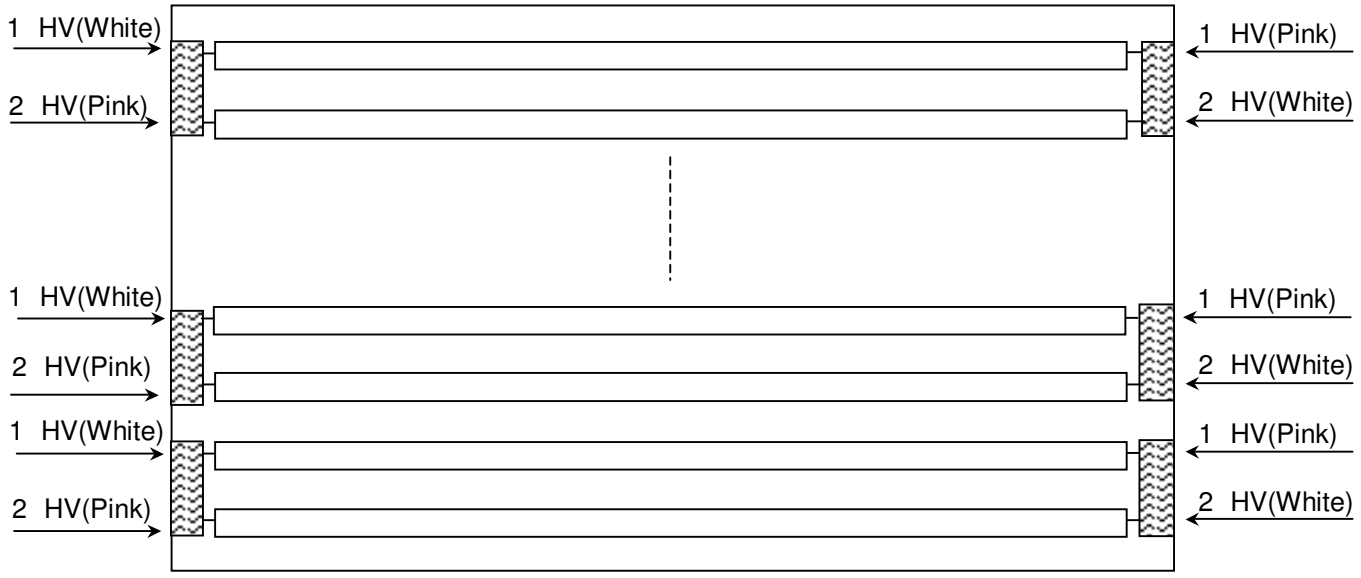
5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN3-CN26: BHR-04VS-1 (JST).

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-04VS-1 or equivalent. The mating header on inverter part number is SM02(12.0)B-BHS-1-TB(LF) or equivalent.



5.3 INVERTER UNIT

CN1 (Header): S14B-PH-SM3-TB (D)(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	VBL	+24V_{DC} power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	SEL	Internal/external PWM selection High : external dimming Low : internal dimming
12	E_PWM	External PWM control signal E_PWM should be connected to ground when internal PWM was selected (SEL = Low).
13	I_PWM	Internal PWM Control Signal I_PWM should be connected to ground when external PWM was selected (SEL = High).
14	BLON	Backlight on/off control

CN2 (Header): S12B-PH-SM3-TB (D)(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	VBL	+24V_{DC} power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC

CN3-CN26 (Header): SM02(12.0)B-BHS-1-TB (LF)(JST) or equivalent

Pin No.	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

CN27-CN30 (Header): LM113P-020-TF1-3(Unicorn) or equivalent

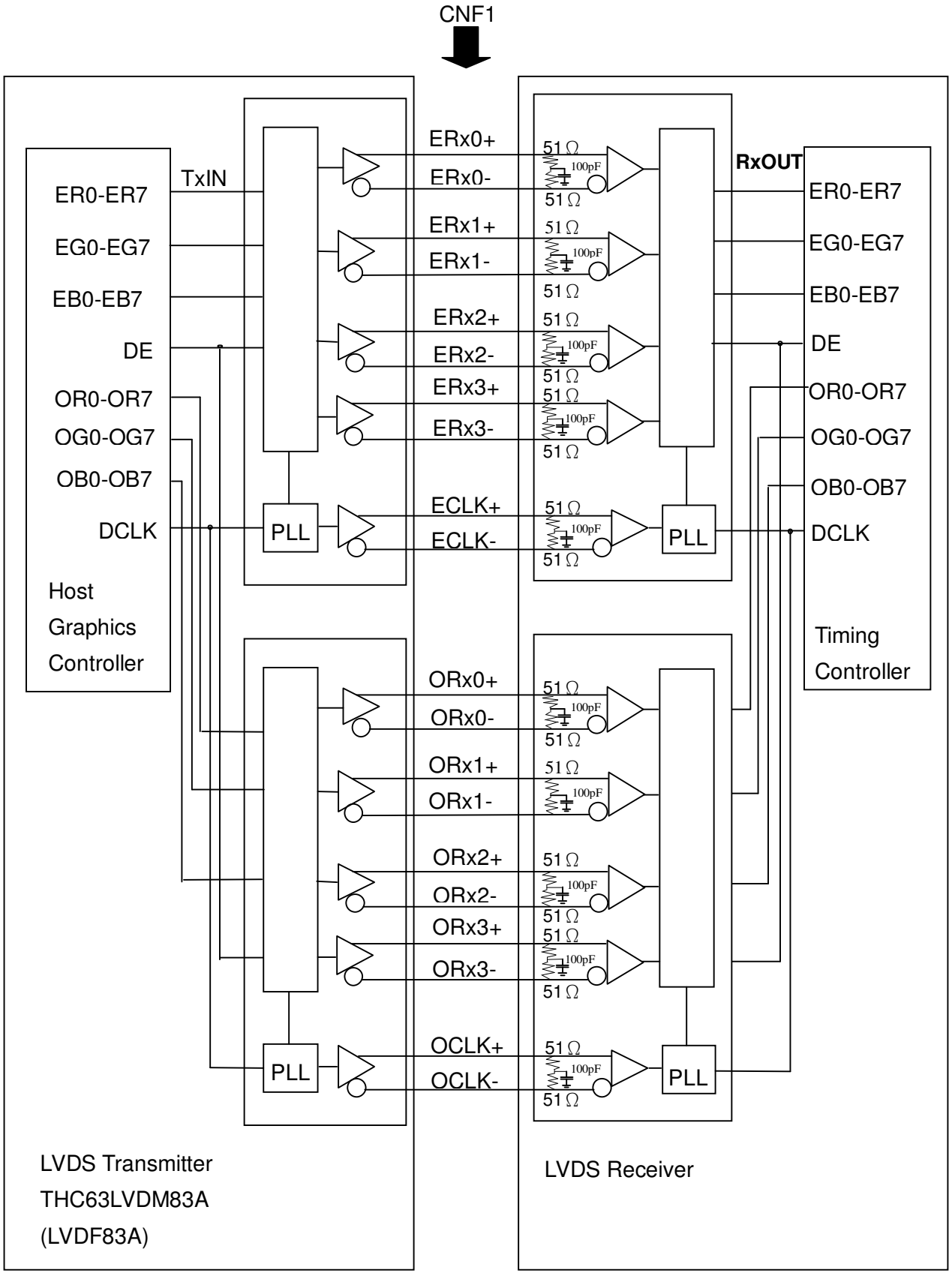
Pin No.	Symbol	Description
1	Control Signal	Board to Board
2		Board to Board
3		Board to Board
4		Board to Board
5		Board to Board
6		Board to Board
7		Board to Board
8		Board to Board
9		Board to Board
10		Board to Board

Note (1) Floating of any control signal is not allowed.

CN31: 7151-E08N (E&T) or equivalent

Pin №	Symbol	Feature	Remark
1	Dim-out	Inverter deliver dimming signal to C/B	Output pin
2	GND	GND	
3	GND	GND	
4	GND	GND	
5	GND	GND	
6	GND	GND	
7	Dim-in	C/B feedback dimming signal	Input pin
8	GND	GND	

5.4 BLOCK DIAGRAM OF INTERFACE



ER0~ER7 : Even pixel R data
EG0~EG7 : Even pixel G data
EB0~EB7 : Even pixel B data
OR0~OR7 : Odd pixel R data
OG0~OG7: Odd pixel G data
OB0~OB7 : Odd pixel B data
DE : Data enable signal
DCLK : Data clock signal

Notes: (1) The system must have the transmitter to drive the module.
(2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.
(3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is even pixel and the second pixel is odd pixel.

5.5 LVDS INTERFACE

	SIGNAL		TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT	
	LVDS_SEL =L or OPEN	LVDS_SEL = H	PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	LVDS_SEL =L or OPEN	LVDS_SEL = H
24 bit	R0	R2	51	TxIN0			27	Rx OUT0	R0	R2
	R1	R3	52	TxIN1			29	Rx OUT1	R1	R3
	R2	R4	54	TxIN2	TA OUT0+	Rx 0+	30	Rx OUT2	R2	R4
	R3	R5	55	TxIN3			32	Rx OUT3	R3	R5
	R4	R6	56	TxIN4			33	Rx OUT4	R4	R6
	R5	R7	3	TxIN6	TA OUT0-	Rx 0-	35	Rx OUT6	R5	R7
	G0	G2	4	TxIN7			37	Rx OUT7	G0	G2
	G1	G3	6	TxIN8			38	Rx OUT8	G1	G3
	G2	G4	7	TxIN9			39	Rx OUT9	G2	G4
	G3	G5	11	TxIN12	TA OUT1+	Rx 1+	43	Rx OUT12	G3	G5
	G4	G6	12	TxIN13			45	Rx OUT13	G4	G6
	G5	G7	14	TxIN14			46	Rx OUT14	G5	G7
	B0	B2	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0	B2
	B1	B3	19	TxIN18			51	Rx OUT18	B1	B3
	B2	B4	20	TxIN19			53	Rx OUT19	B2	B4
	B3	B5	22	TxIN20			54	Rx OUT20	B3	B5
	B4	B6	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4	B6
	B5	B7	24	TxIN22			1	Rx OUT22	B5	B7
	DE	DE	30	TxIN26			6	Rx OUT26	DE	DE
	R6	R0	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6	R0
	R7	R1	2	TxIN5			34	Rx OUT5	R7	R1
	G6	G0	8	TxIN10			41	Rx OUT10	G6	G0
	G7	G1	10	TxIN11			42	Rx OUT11	G7	G1
	B6	B0	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6	B0
	B7	B1	18	TxIN17			50	Rx OUT17	B7	B1
	RSVD 1	RSVD 1	25	TxIN23			2	Rx OUT23	NC	NC
	RSVD 2	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	NC	NC
	RSVD 3	RSVD 3	28	TxIN25			5	Rx OUT25	NC	NC
	DCLK		31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK	

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

5.7 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

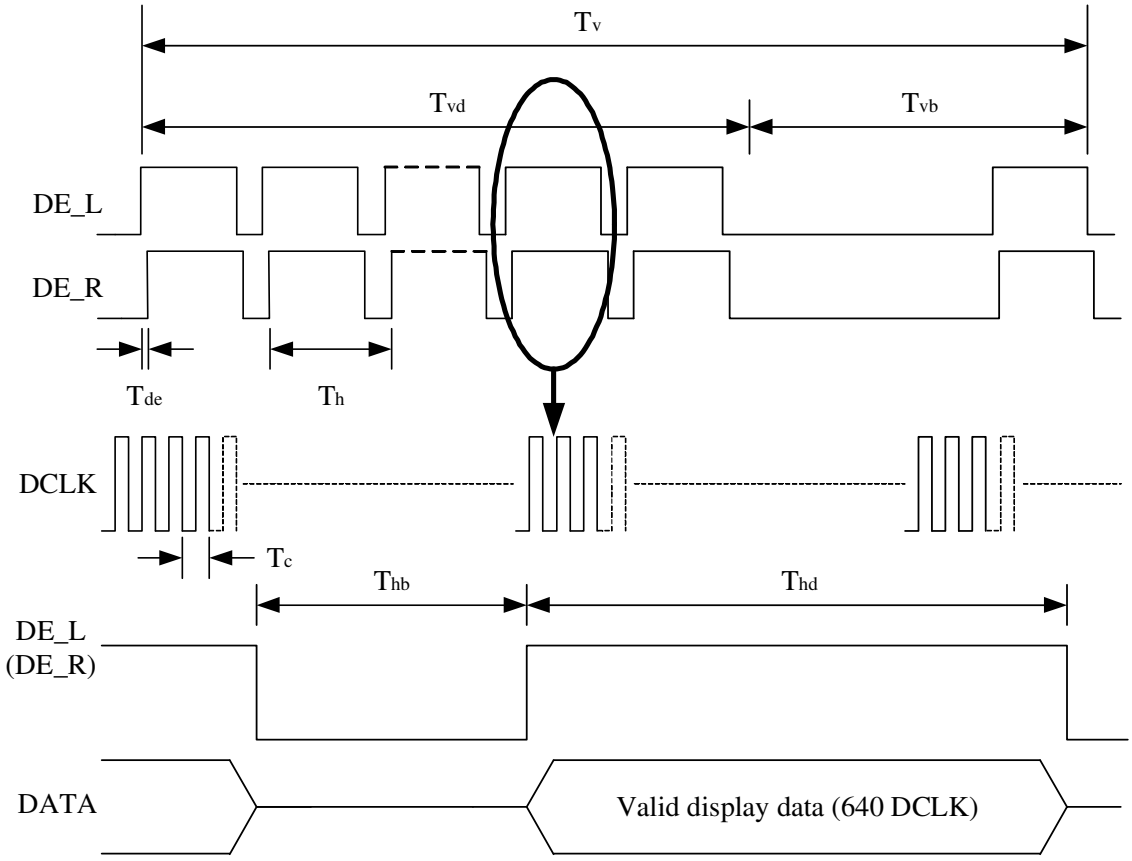
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	(60)	78	(80)	MHz	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	-
	Hold Time	Tlvhd	600	-	-	ps	-
Vertical Active Display Term	Frame Rate	Fr5	47	50	53	Hz	(1)
		Fr6	57	60	63	Hz	(1)
	Total	Tv	(1475)	1490	(1520)	Th	Tv=Tvd+Tvb
	Display	Tvd	1440	1440	1440	Th	-
	Blank	Tvb	(35)	50	(80)	Th	-
Horizontal Active Display Term	Total	Th	(750)	872	(890)	Tc	Th=Thd+Thb
	Display	Thd	640	640	640	Tc	-
	Blank	Thb	(110)	232	(250)	Tc	-
Data Enable Term	Delay Time	Tde		0	(3)	DCLK	(3)

Note (1) (ODSEL) = (H) , (L). Please refer to 5.1 for detail information.

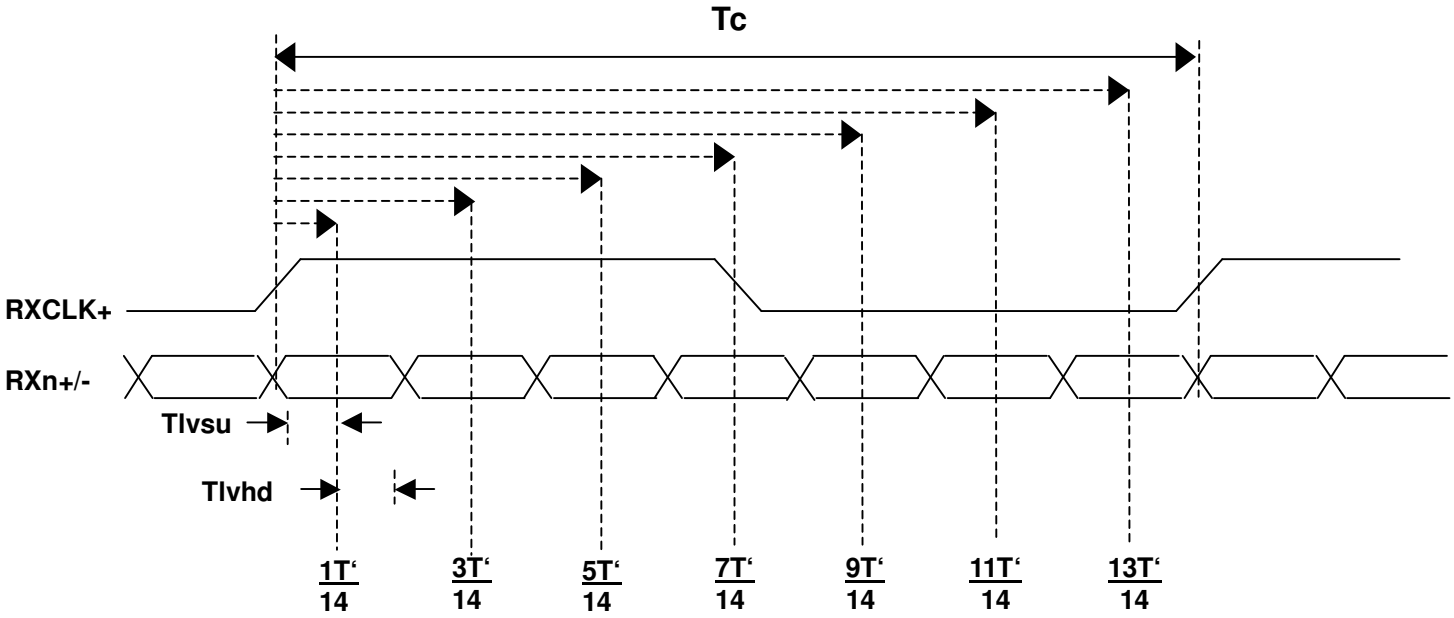
Note (2) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (3) Left side Data Enable signal (DE_L) and Right side Data Enable signal (DE_R) must be synchronized. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM

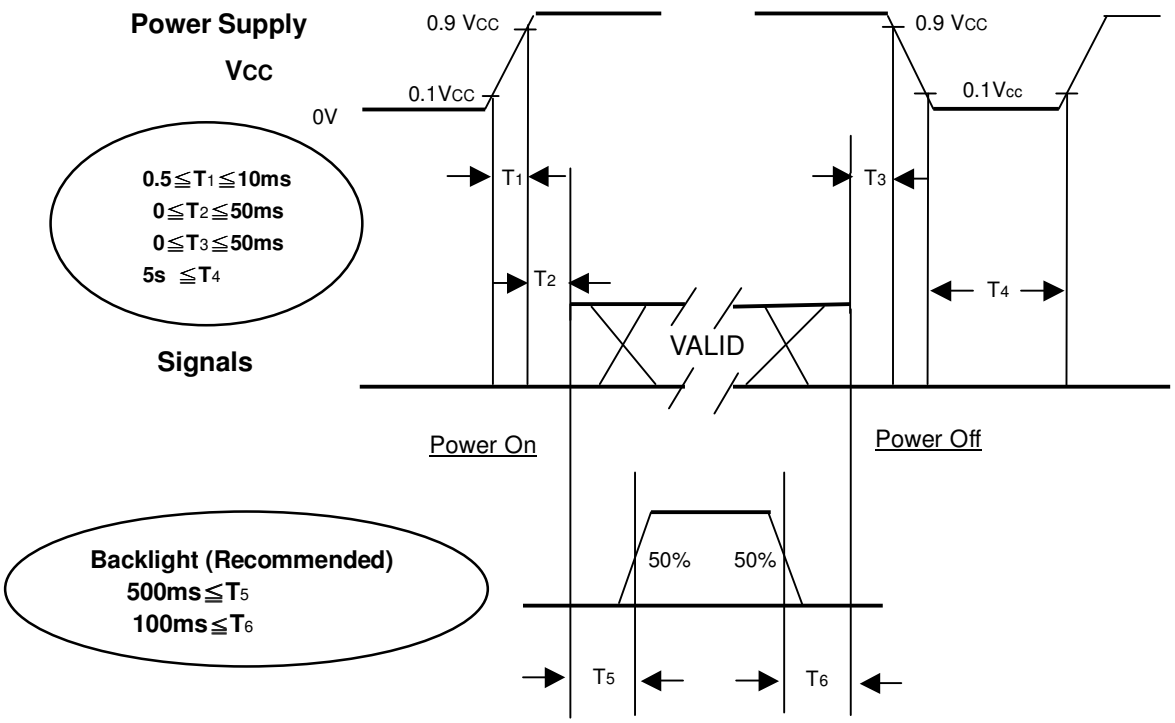


LVDS INPUT INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Power ON/OFF Sequence

Note.

(1) The supply voltage of the external system for the module input should follow the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12/V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	5.8±0.5	mA
Oscillating Frequency (Inverter)	F_W	47±3	KHz
Vertical Frame Rate	Fr	60	Hz

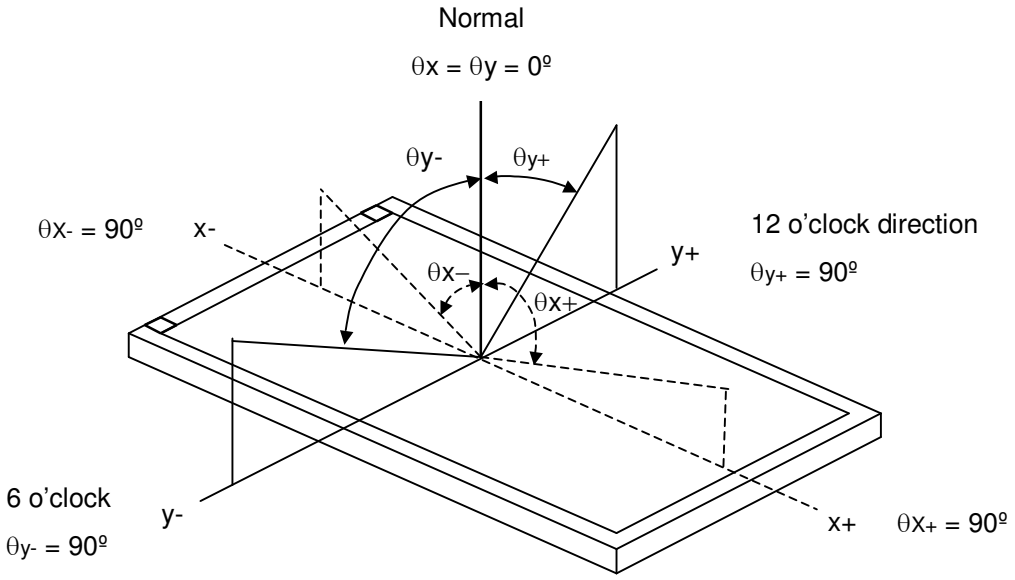
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Angle at Normal Direction	(1200)	(1500)	-	-	Note (2)
Response Time		Gray to gray		-	(6.5)		ms	Note (3)
Center Luminance of White		L_C		(400)	(450)	-	cd/m^2	Note (4)
White Variation		δW		-	-	(1.3)	-	Note (7)
Cross Talk		CT		-	-	4	%	Note (5)
Color Chromaticity	Red	Rx		Typ.– 0.03	(0.652)	Typ.+ 0.03	-	Note (6)
		Ry			(0.322)		-	
	Green	Gx			(0.204)		-	
		Gy			(0.597)		-	
	Blue	Bx			(0.144)		-	
		By			(0.092)		-	
	White	Wx			0.280		-	
		Wy			0.285		-	
	Color Gamut				(85)	-	%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20	80	88	-	Deg.	Note (1)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

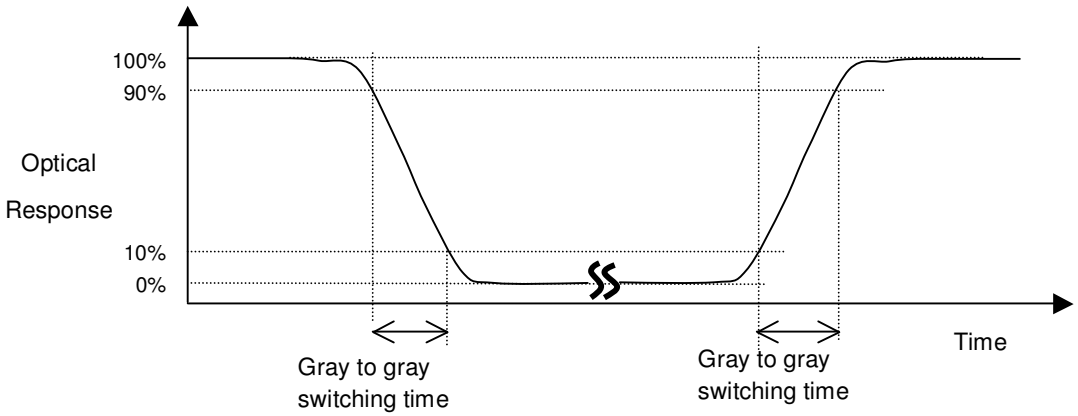
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7)

Note (3) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 63, 127, 191, and 255.

Gray to gray average time means the average switching time of gray level 0 ,63,127,191,255 to each other .

Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point.

L_C = L (5), where L (x) is corresponding to the luminance of the point X at the figure in Note (7).

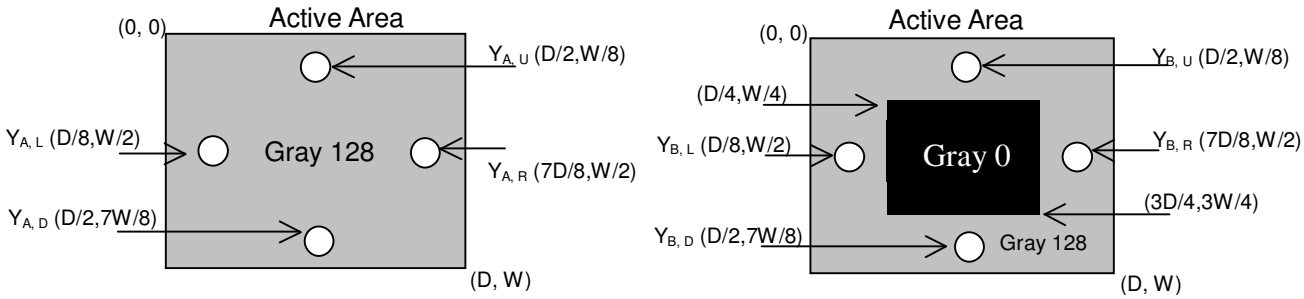
Note (5) Definition of Cross Talk (CT):

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where:

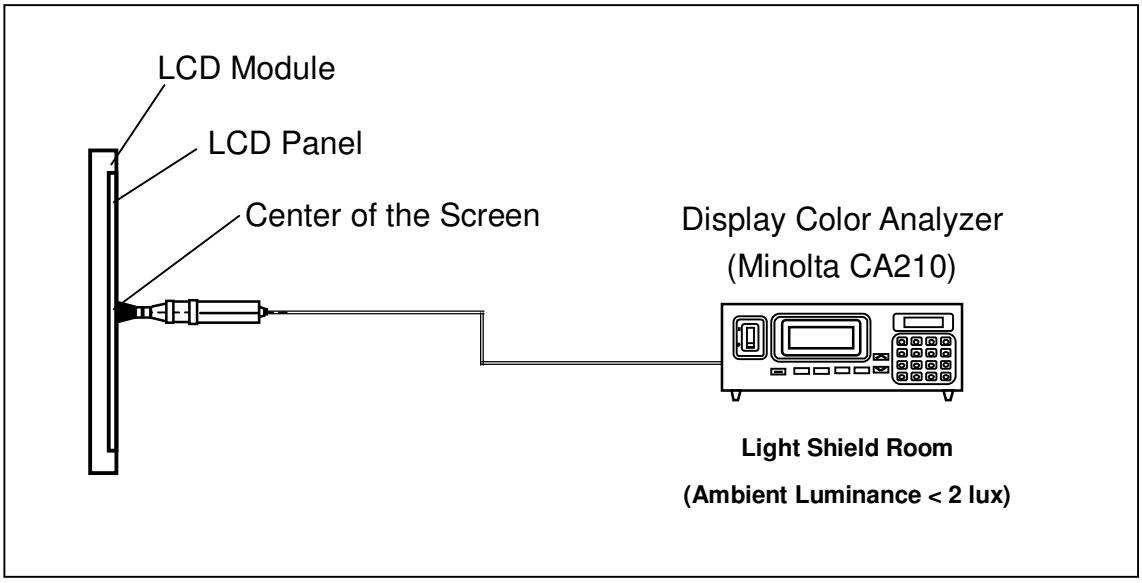
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

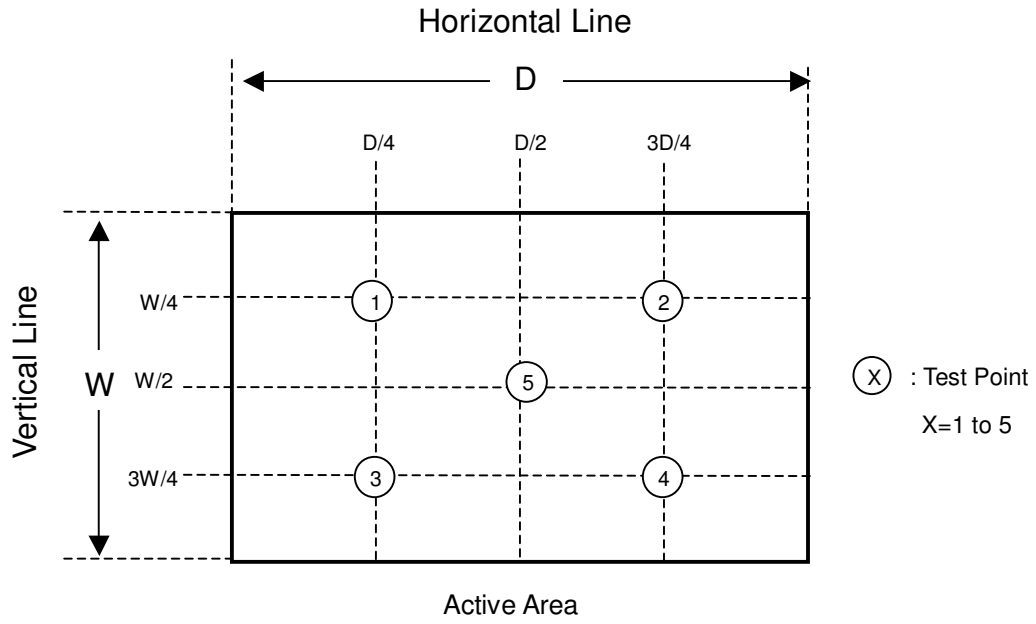
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

(1) The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

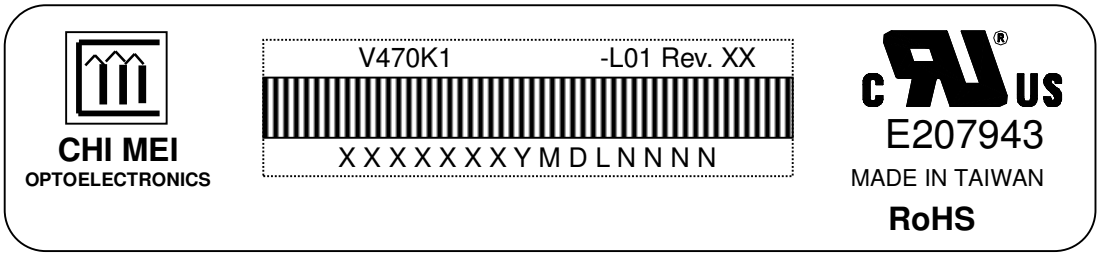
(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

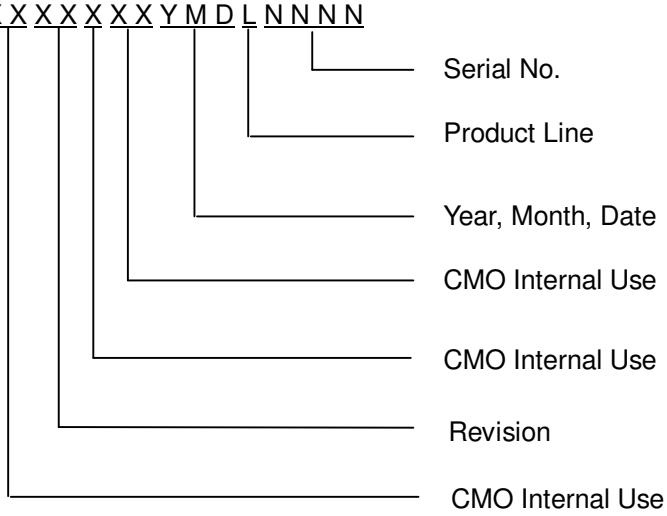
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V470K1-L01

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2000~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

10. PACKAGING

10.1 PACKING SPECIFICATIONS

(1) 2 LCD TV modules / 1 Box

(2) Box dimensions : 1198(L) X 331 (W) X 720 (H)

(3) Weight : approximately 43Kg (2 modules per box)

10.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

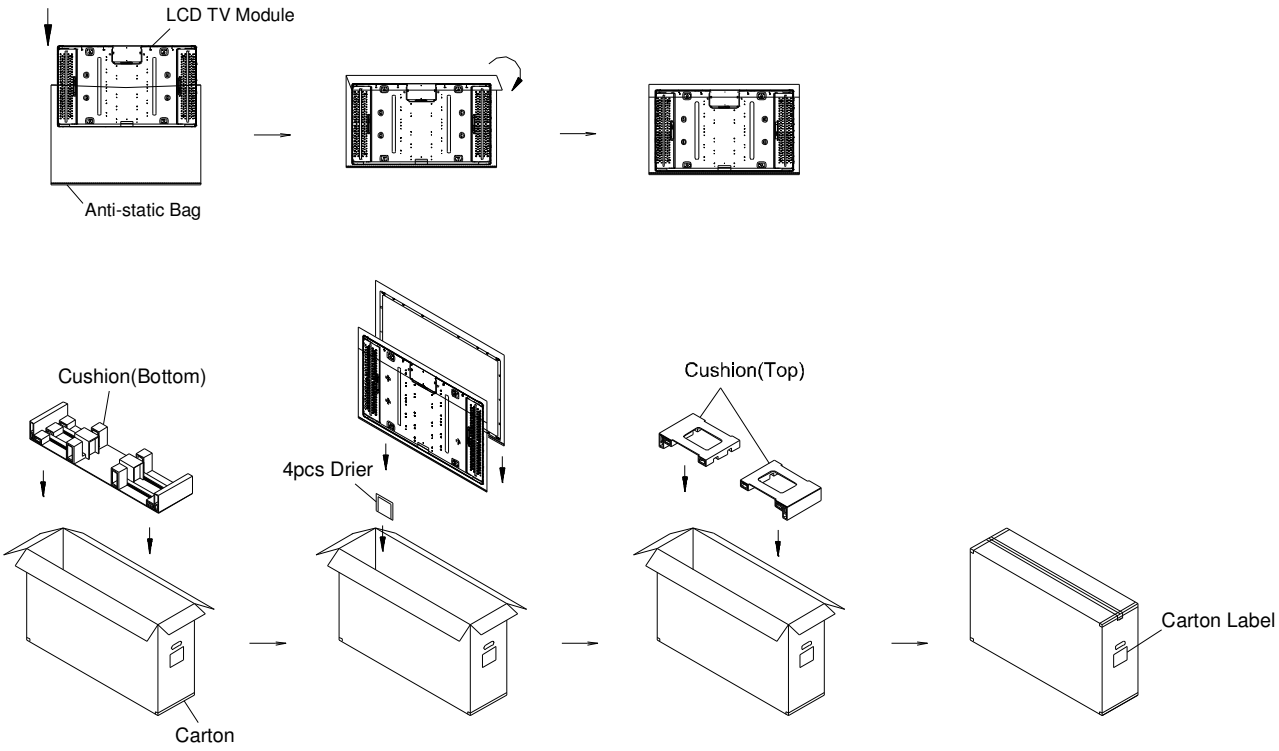


Figure.9-1 packing method

Corner Protector:L1130*50*50mm
L1400*50*50mm
Pallet:L1000*W1200*H140mm
Pallet Stack:L1000*W1200*H1580mm
Gross:276kg

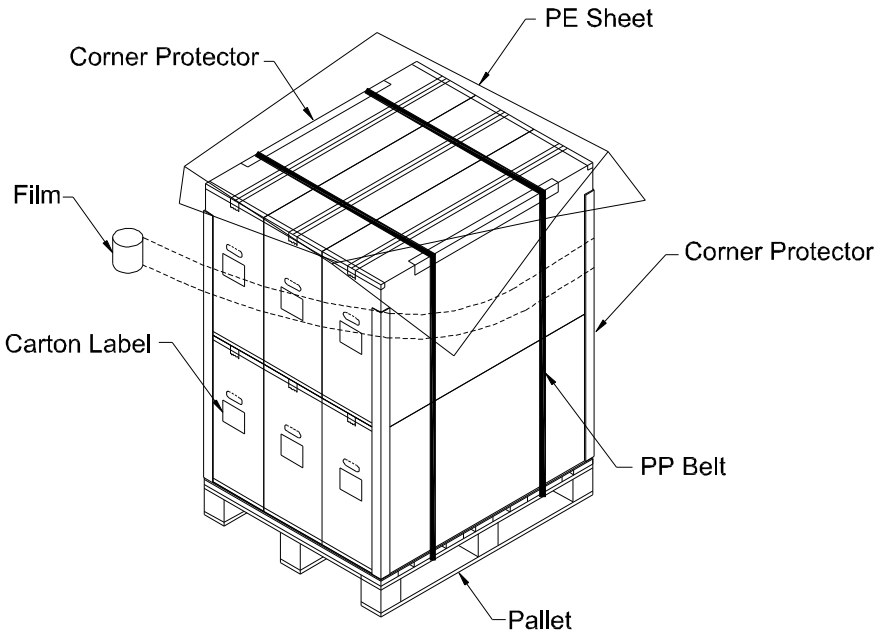
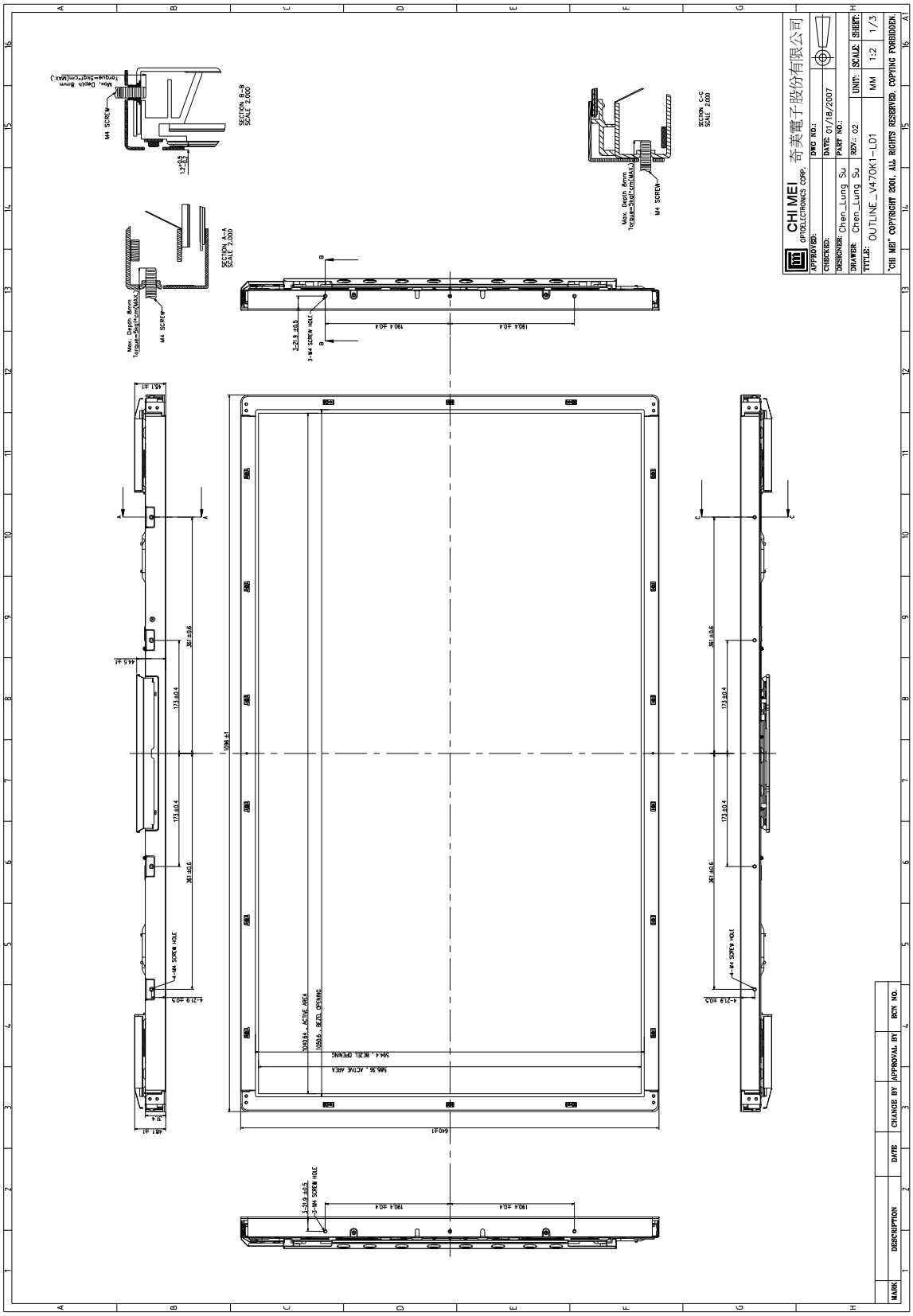
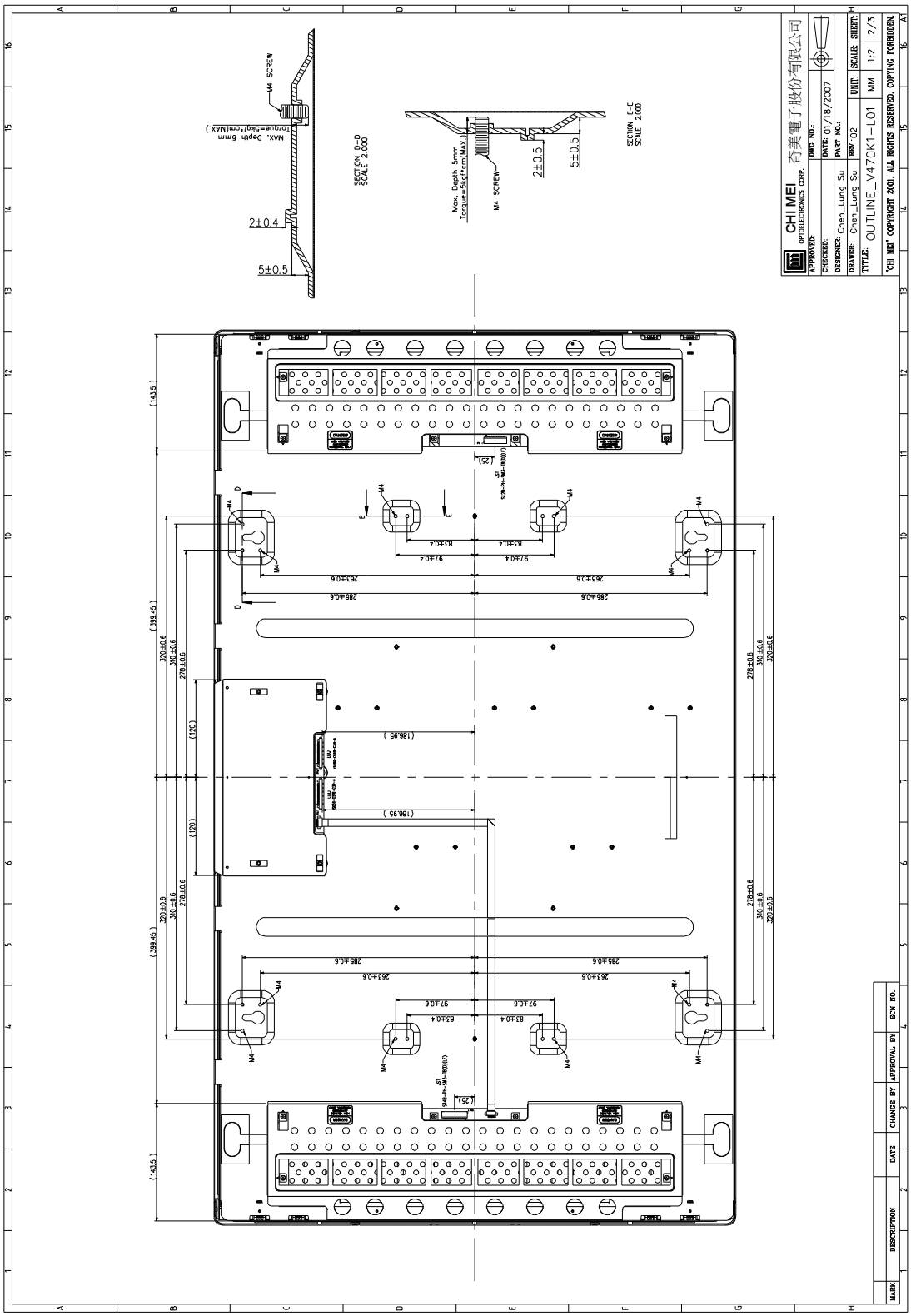
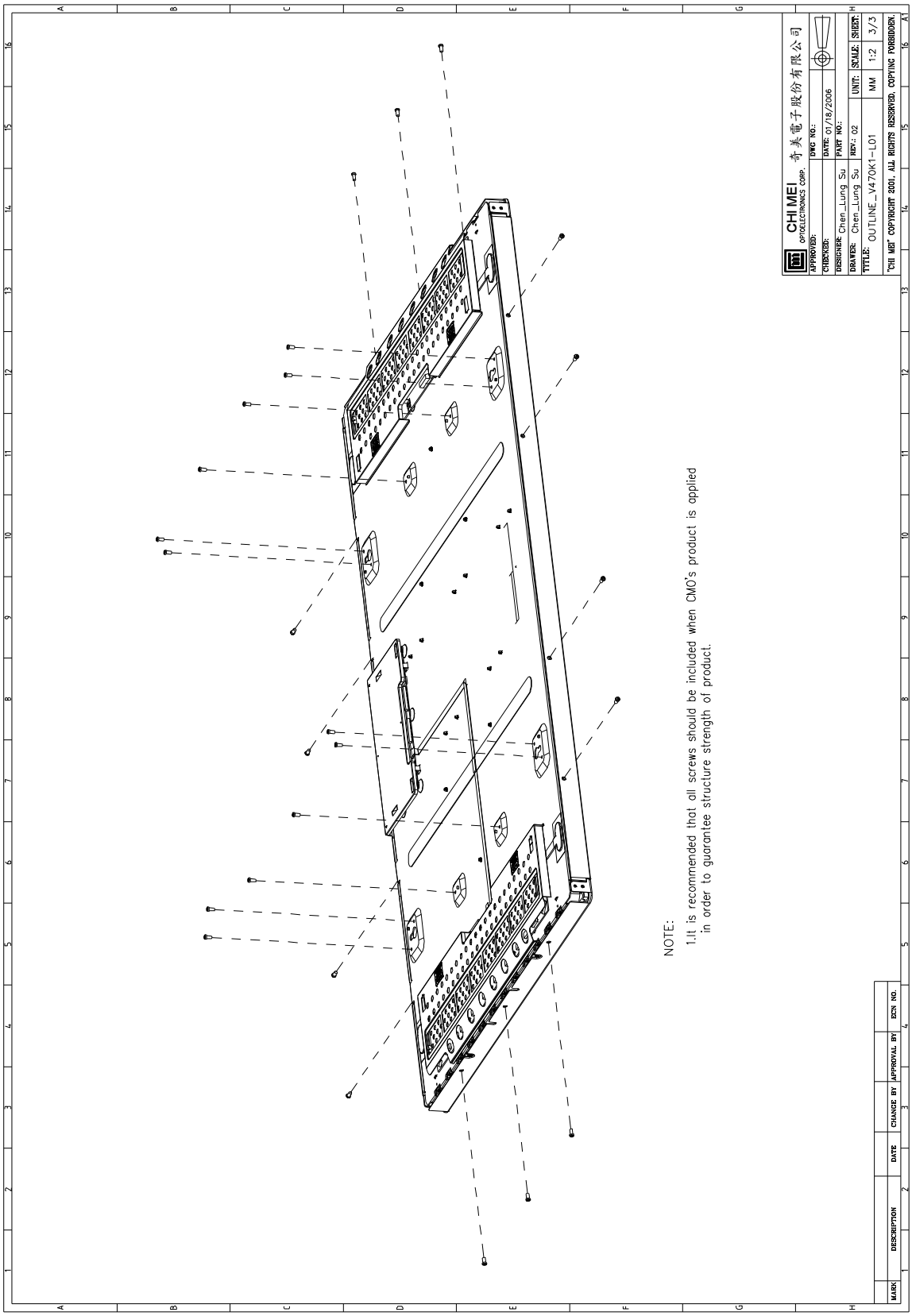


Figure.10-2 packing

11. MECHANICAL CHARACTERISTIC




SECTION D-D
SCALE 2.000
SECTION E-E
SCALE 2.000
M4 SCREW
Max. Depth 5mm
Torque=5kgf*cm(MAX.)
2±0.4
5±0.5
2±0.5
奇美電子股份有限公司
CHI MEI OPTOELECTRONICS CORP.
DWG NO.:
DATE: 01/18/2007
PART NO.:
REV: 02
UNIT: MM
SCALE: 1:2
SHEET: 2/3
DESIGNER: Chen_Lung Su
DRAWER: Chen_Lung Su
TITLE: OUTLINE_V470K1-L01
"CHI MEI" COPYRIGHT 2001, ALL RIGHTS RESERVED, COPYING FORBIDDEN.
APPROVED:
CHECKED:
MARK
DESCRIPTION
DATE
CHANGES BY
APPROVAL BY
ECN NO.


NOTE:
1.It is recommended that all screws should be included when CMO's product is applied
in order to guarantee structure strength of product.
CHI MEI OPTOELECTRONICS CORP.
奇美電子股份有限公司
APPROVED:
CHECKED:
DWG NO.:
DESIGNER: Chen_Lung Su
DATE: 01/18/2006
PART NO.:
DRAWER: Chen_Lung Su
REV: 02
UNIT: MM
SCALE: 1:2
SHEET 3/3
TITLE: OUTLINE_V470K1-L01
"CHI MEI" COPYRIGHT 2001, ALL RIGHTS RESERVED, COPYING FORBIDDEN.
MARK
DESCRIPTION
DATE
CHANGE BY
APPROVAL BY
ECN NO.