National Semiconductor

74BCT543
Octal Registered Transceiver

General Description

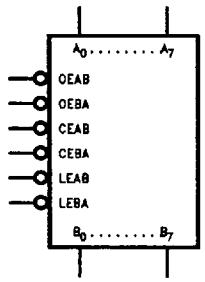
The 'BCT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 24 mA while the B outputs are rated for 64 mA.

Features

- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 24 mA
- B outputs sink 64 mA
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Ordering Code: See Section 11

Logic Symbols



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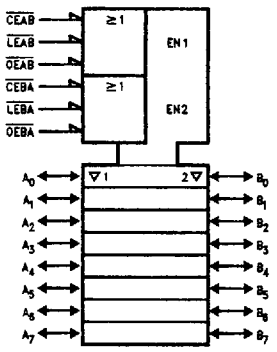
IEEE/IEC



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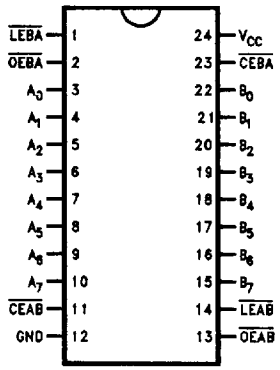
Connection Diagram

Pin Assignment for DIP and SOIC



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Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

Functional Description

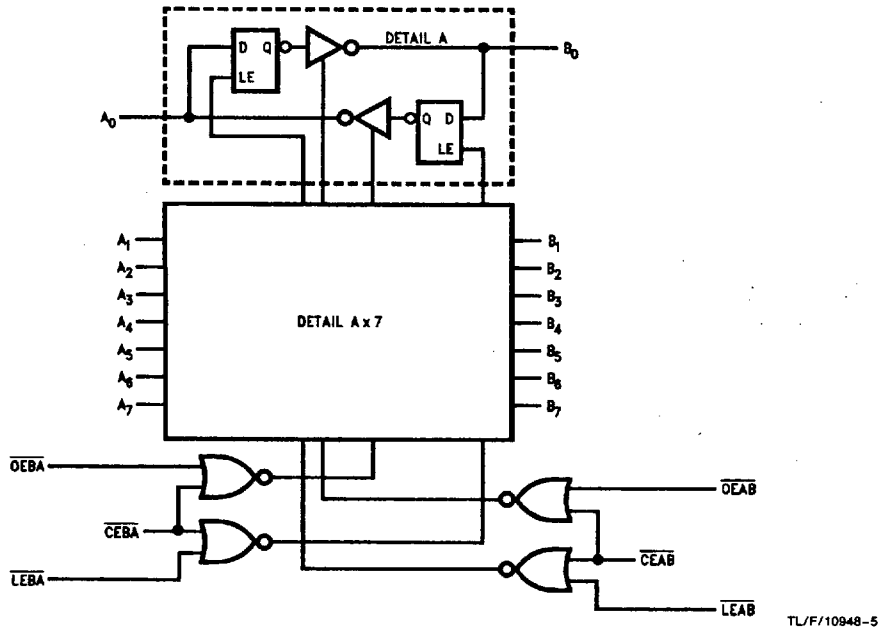
The 'BCT543 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0–A_7 or take data from B_0–B_7, as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in the Disable or Power-Off State	−0.5V to +5.5V
in HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V_{IN} = 7.0V ($\overline{OEAB}$, $\overline{OEBA}$, $\overline{LEAB}$, $\overline{LEBA}$, $\overline{CEAB}$, $\overline{CEBA}$)
I_{BVIT}	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded

DC Electrical Characteristics (Continued)

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
I_{IL}	Input LOW Current			−0.6 −1.2	mA	Max	V_{IN} = 0.5V ($\overline{OEAB}$, $\overline{OEBA}$) V_{IN} = 0.5V ($\overline{CEAB}$, $\overline{CEBA}$)
$I_{IH} + I_{OZH}$	Output Leakage Current			70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
$I_{IL} + I_{OZL}$	Output Leakage Current			−650	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current	−60 −100		−150 −225	mA	Max	V_{OUT} = 0V (A_n) V_{OUT} = 0V (B_n)
I_{ZZ}	Bus Drainage Test			500	μA	0.0V	V_{OUT} = 5.25V (A_n, B_n)
I_{CCH}	Power Supply Current			15	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			71	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			15	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT T_A = +25°C V_{CC} = +5.0V C_L = 50 pF			74BCT T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	2.0 2.0		8.8 9.6	2.0 2.0	8.8 9.6	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ or $\overline{LEAB}$ to A_n or B_n	2.0 2.0		12.9 12.7	2.0 2.0	12.9 12.7	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.0 1.0		12.5 14.5	1.0 1.0	12.5 14.5	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.0 1.0		8.1 7.2	1.0 1.0	8.1 7.2		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			0.8		0.8	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			0.8		0.8	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			3.8		3.8	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			4.0		4.0	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}).

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device.

AC Operating Requirements: See Section 8 for Waveforms

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$		74BCT T_A, V_{CC} = Com		Units	Fig. No.
		Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	4.5 3.0		4.5 3.5		ns	8–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	1.5 3.0		1.5 3.5		ns	8–6
$t_w(L)$	Latch Enable, B to A Pulse Width, LOW	7.0		7.0		ns	8–4

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT T_A = Com V_{CC} = Com C_L = 50 pF 8 Outputs Switching (Note 3)		74BCT T_A = Com V_{CC} = Com C_L = 250 pF (Note 4)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	3.0 3.0	9.8 10.6	3.0 3.0	9.8 10.6	ns	8–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_n	3.0 3.0	13.4 13.2	3.0 3.0	13.9 13.7	ns	8–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAB}$ to B_n	4.5 4.5	13.0 13.0	4.5 4.5	13.5 13.5	ns	8–3

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Control Inputs	6	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	11	pF	V_{CC} = 5.0V