

T-46-07-09



## CD4508B Types

## CMOS Dual 4-Bit Latch

## High-Voltage Types (20-Volt Rating)

■ CD4508B dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET, and OUTPUT DISABLE controls. With the STROBE line in the high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the reset line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line applications by a high level on the DISABLE input.

The CD4508B types are supplied in the 24-lead dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

The CD4508B is similar to industry type MC14508.

## Features:

- Two independent 4-bit latches
- Individual master reset for each 4-bit latch
- 3-state outputs with high-impedance state for bus line applications
- Medium-speed operation:  $t_{PHL} = t_{PLH} = 70$  ns (typ.) at  $V_{DD} = 10$  V and  $C_L = 50$  pF
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

## Applications:

- Buffer storage
- Holding registers
- Data storage and multiplexing

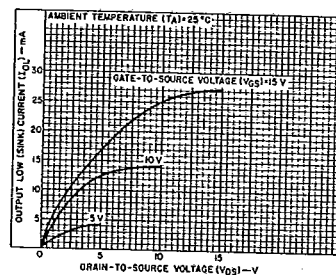
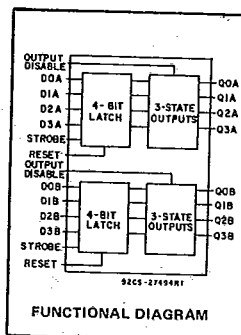


Fig. 2 - Typical output low (sink) current characteristics.

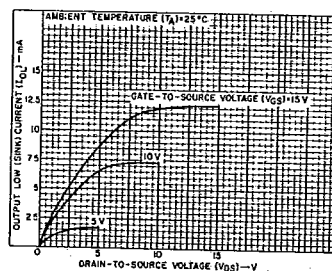


Fig. 3 - Minimum output low (sink) current characteristics.

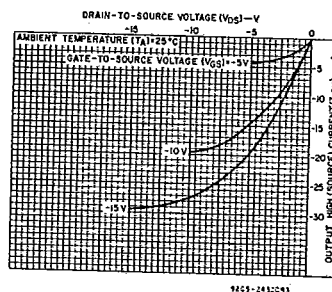


Fig. 4 - Typical output high (source) current characteristics.

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal) ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to  $V_{DD} + 0.5$  V

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm 10$  mA

POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearly at 12mW/ $^\circ\text{C}$  to 200mW

## DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$  ..... 100mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

## LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79mm) from case for 10s max .....  $+265^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS at  $T_A = 25^\circ\text{C}$ , Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC                                                            | $V_{DD}$<br>(V) | LIMITS            |             | UNITS |
|---------------------------------------------------------------------------|-----------------|-------------------|-------------|-------|
|                                                                           |                 | Min.              | Max.        |       |
| Supply-Voltage Range (For $T_A = \text{Full Package-Temperature Range}$ ) |                 | 3                 | 18          | V     |
| Reset Pulse Width, $t_{WR}$                                               | 5<br>10<br>15   | 200<br>140<br>100 | —<br>—<br>— | ns    |
| Strobe Pulse Width, $t_{W(st)}$                                           | 5<br>10<br>15   | 140<br>80<br>70   | —<br>—<br>— |       |
| Setup Time, $t_{SU}$                                                      | 5<br>10<br>15   | 50<br>30<br>20    | —<br>—<br>— |       |
| Hold Time, $t_H$                                                          | 5<br>10<br>15   | 0<br>0<br>0       | —<br>—<br>— |       |

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## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTER-<br>ISTIC                             | CONDITIONS |            |            | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      |    | UNITS |
|-------------------------------------------------|------------|------------|------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|----|-------|
|                                                 | VO<br>(V)  | VIN<br>(V) | VDD<br>(V) | +25                                   |       |       |       |       |                   |      |    |       |
|                                                 |            |            |            | -55                                   | -40   | +85   | +125  | Min.  | Typ.              | Max. |    |       |
| Quiescent Device<br>Current,<br>IDD Max.        | —          | 0.5        | 5          | 5                                     | 5     | 150   | 150   | —     | 0.04              | 5    | μA |       |
|                                                 | —          | 0,10       | 10         | 10                                    | 10    | 300   | 300   | —     | 0.04              | 10   |    |       |
|                                                 | —          | 0,15       | 15         | 20                                    | 20    | 600   | 600   | —     | 0.04              | 20   |    |       |
|                                                 | —          | 0,20       | 20         | 100                                   | 100   | 3000  | 3000  | —     | 0.08              | 100  |    |       |
| Output Low<br>(Sink) Current<br>IOL Min.        | 0.4        | 0.5        | 5          | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | —    | mA |       |
|                                                 | 0.5        | 0,10       | 10         | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | —    |    |       |
|                                                 | 1.5        | 0,15       | 15         | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | —    |    |       |
| Output High<br>(Source)<br>Current,<br>IOH Min. | 4.6        | 0.5        | 5          | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | —    | mA |       |
|                                                 | 2.5        | 0.5        | 5          | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | —    |    |       |
|                                                 | 9.5        | 0,10       | 10         | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | —    |    |       |
|                                                 | 13.5       | 0,15       | 15         | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              | —    |    |       |
| Output Voltage<br>Low-Level,<br>VOL Max.        | —          | 0.5        | 5          | 0.05                                  |       |       |       | —     | 0                 | 0.05 | V  |       |
|                                                 | —          | 0,10       | 10         | 0.05                                  |       |       |       | —     | 0                 | 0.05 |    |       |
|                                                 | —          | 0.15       | 15         | 0.05                                  |       |       |       | —     | 0                 | 0.05 |    |       |
| Output Voltage<br>High-Level,<br>VOH Min.       | —          | 0.5        | 5          | 4.95                                  |       |       |       | 4.95  | 5                 | —    | V  |       |
|                                                 | —          | 0,10       | 10         | 9.95                                  |       |       |       | 9.95  | 10                | —    |    |       |
|                                                 | —          | 0.15       | 15         | 14.95                                 |       |       |       | 14.95 | 15                | —    |    |       |
| Input Low<br>Voltage,<br>VIL Max.               | 0.5, 4.5   | —          | 5          | 1.5                                   |       |       |       | —     | —                 | 1.5  | V  |       |
|                                                 | 1, 9       | —          | 10         | 3                                     |       |       |       | —     | —                 | 3    |    |       |
|                                                 | 1.5, 13.5  | —          | 15         | 4                                     |       |       |       | —     | —                 | 4    |    |       |
| Input High<br>Voltage,<br>VIH Min.              | 0.5, 4.5   | —          | 5          | 3.5                                   |       |       |       | 3.5   | —                 | —    | V  |       |
|                                                 | 1, 9       | —          | 10         | 7                                     |       |       |       | 7     | —                 | —    |    |       |
|                                                 | 1.5, 13.5  | —          | 15         | 11                                    |       |       |       | 11    | —                 | —    |    |       |
| Input Current<br>IIN Max.                       | —          | 0,18       | 18         | ±0.1                                  | ±0.1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0.1 | μA |       |
| 3-State Output<br>Leakage Current<br>IOUT Max.  | 0,18       | 0,18       | 18         | ±0.4                                  | ±0.4  | ±12   | ±12   | —     | ±10 <sup>-4</sup> | ±0.4 | μA |       |

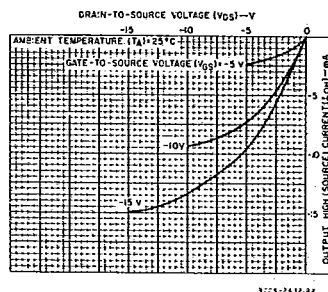
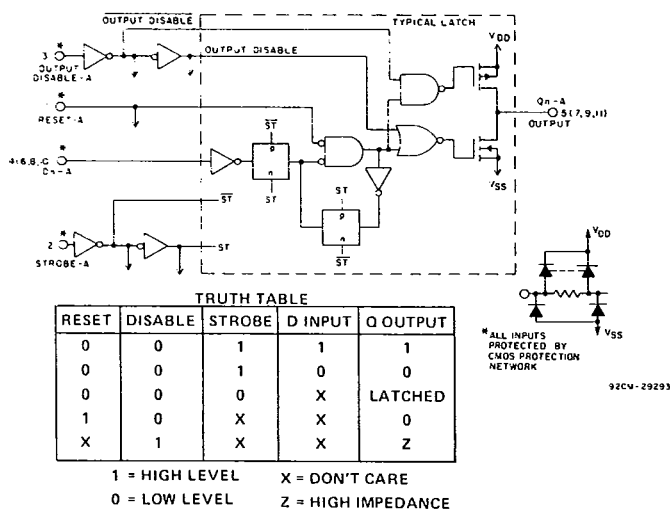


Fig. 4 — Minimum output high (source) current characteristics.

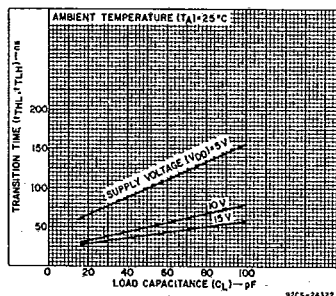


Fig. 5 — Typical transition time as a function of load capacitance.

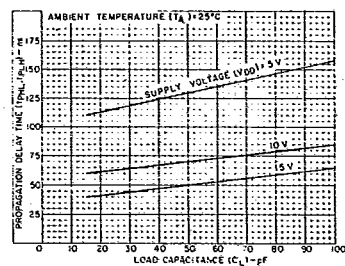


Fig. 6 — Typical propagation delay time as a function of load capacitance (strobe to data out).

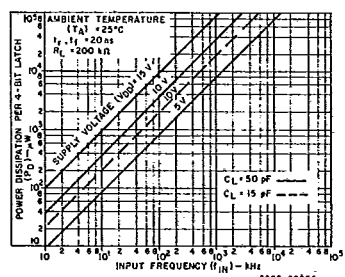


Fig. 8 — Typical power dissipation as a function of frequency.

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DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$ , unless otherwise specified.

| CHARACTERISTIC                                                               | TEST CONDITIONS | LIMITS   |      |      | UNITS |
|------------------------------------------------------------------------------|-----------------|----------|------|------|-------|
|                                                                              |                 | $V_{DD}$ | Typ. | Max. |       |
| Transition Time, $t_{THL}, t_{TLH}$                                          |                 | 5        | 100  | 200  | ns    |
|                                                                              |                 | 10       | 50   | 100  |       |
|                                                                              |                 | 15       | 40   | 80   |       |
| Minimum Reset Pulse Width, $t_{W(R)}$                                        |                 | 5        | 100  | 200  |       |
|                                                                              |                 | 10       | 70   | 140  |       |
|                                                                              |                 | 15       | 50   | 100  |       |
| Minimum Strobe Pulse Width, $t_{W(st)}$                                      |                 | 5        | 70   | 140  |       |
|                                                                              |                 | 10       | 40   | 80   |       |
|                                                                              |                 | 15       | 35   | 70   |       |
| Minimum Setup Time, $t_{SU}$                                                 |                 | 5        | 25   | 50   |       |
|                                                                              |                 | 10       | 15   | 30   |       |
|                                                                              |                 | 15       | 10   | 20   |       |
| Minimum Hold Time, $t_H$                                                     |                 | 5        | 0    | 0    |       |
|                                                                              |                 | 10       | 0    | 0    |       |
|                                                                              |                 | 15       | 0    | 0    |       |
| Propagation Delay Times: $t_{PHL}, t_{PLH}$<br>Strobe to Data Out            |                 | 5        | 130  | 260  |       |
|                                                                              |                 | 10       | 70   | 140  |       |
|                                                                              |                 | 15       | 50   | 100  |       |
| Data In to Data Out                                                          |                 | 5        | 105  | 210  |       |
|                                                                              |                 | 10       | 60   | 120  |       |
|                                                                              |                 | 15       | 45   | 90   |       |
| Reset to Data Out                                                            |                 | 5        | 90   | 180  |       |
|                                                                              |                 | 10       | 50   | 100  |       |
|                                                                              |                 | 15       | 40   | 80   |       |
| 3-State Propagation Delay Times:<br>Output High to High Impedance, $t_{PHZ}$ |                 | 5        | 90   | 180  | ns    |
|                                                                              |                 | 10       | 50   | 100  |       |
|                                                                              |                 | 15       | 35   | 70   |       |
| High Impedance to Output High, $t_{PZH}$                                     |                 | 5        | 90   | 180  |       |
|                                                                              |                 | 10       | 50   | 100  |       |
|                                                                              |                 | 15       | 35   | 70   |       |
| Output Low to High Impedance, $t_{PLZ}$                                      |                 | 5        | 90   | 180  |       |
|                                                                              |                 | 10       | 50   | 100  |       |
|                                                                              |                 | 15       | 35   | 70   |       |
| High Impedance to Output Low, $t_{PZL}$                                      |                 | 5        | 90   | 180  |       |
|                                                                              |                 | 10       | 50   | 100  |       |
|                                                                              |                 | 15       | 35   | 70   |       |
| Input Capacitance, $C_{IN}$                                                  | Any Input       | —        | 5    | 7.5  | pF    |

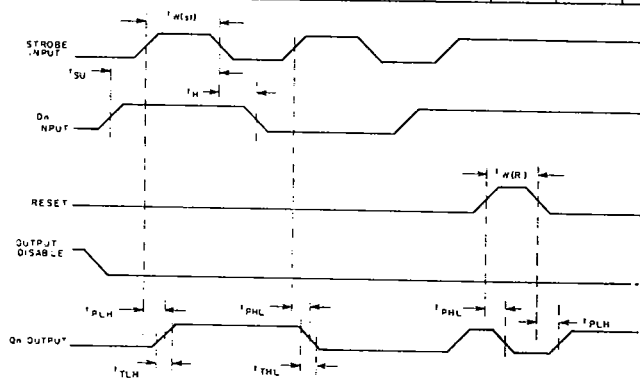


Fig. 12 — Test waveforms.

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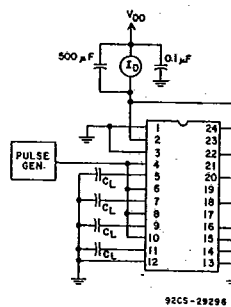


Fig. 9 — Power dissipation test circuit.

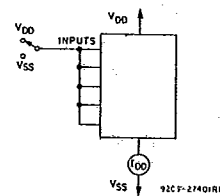


Fig. 10 — Quiescent device current test circuit.

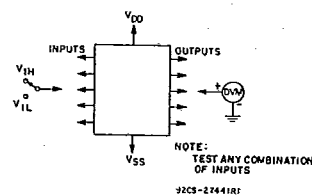


Fig. 11 — Input voltage test circuit.

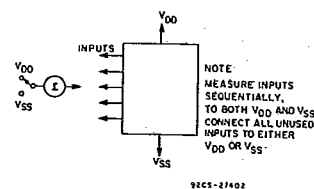
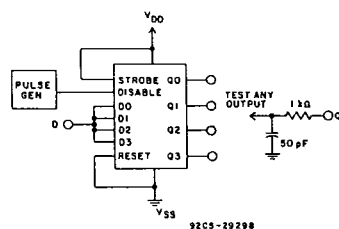


Fig. 13 — Input current test circuit.

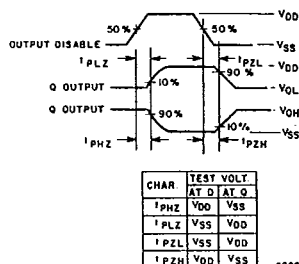
3  
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HIGH VOLTAGE ICs

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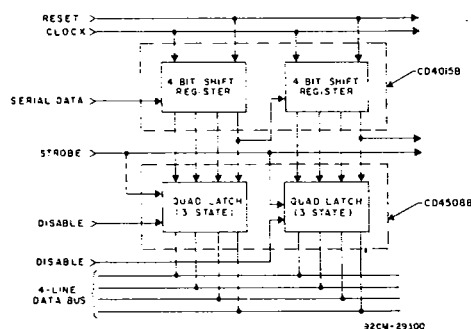


92CS-29298



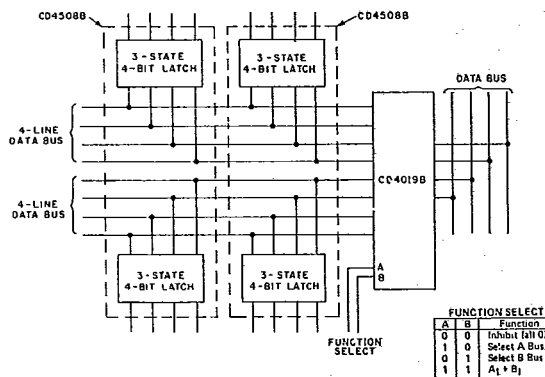
92CS-29299

Fig. 14 - Output disable test circuit and waveforms.



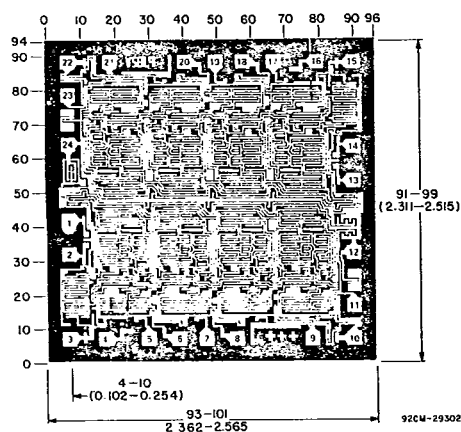
92CM-29300

Fig. 15 - Bus register.



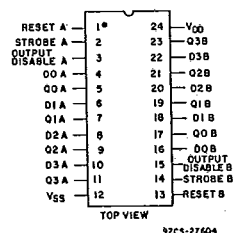
92CM-29301

Fig. 16 - Dual multiplexed bus register with function select.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10<sup>-3</sup> inch).

Chip dimensions and pad layout for CD4508B.



TERMINAL ASSIGNMENT