

2x512Kx8 Static RAM
CMOS, Module

Features

2x512Kx8 bit CMOS Static
Random Access Memory

- Access Times: 70, 85, and 100ns
- Common Address and Data Pins
- Data Retention Function (EDI9F81025LP)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

36 Lead SOIC Module, No. 198

Single +5V ($\pm 10\%$) Supply Operation

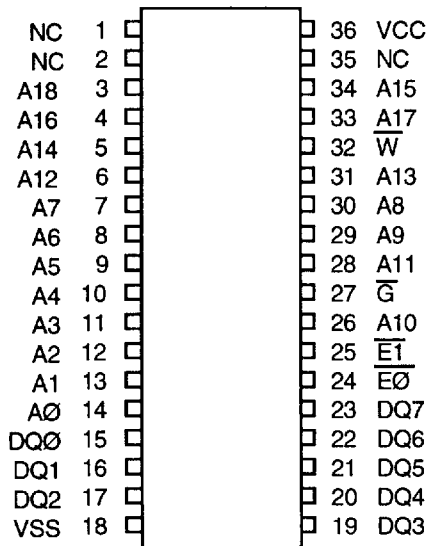
The EDI9F81025C is an 8 megabit CMOS Static RAM based on two 512Kx8 Static RAMs mounted on a multi-layered epoxy laminate (FR4) substrate.

The EDI9F81025C is organized as two separate banks of 512Kx8 Random Access Memory, with common address and data pins to minimize module size. It is offered with access times of 70, 85, and 100ns.

It is also available as EDI9F81025LP, which features Low Power and Battery Back-up Data Retention.

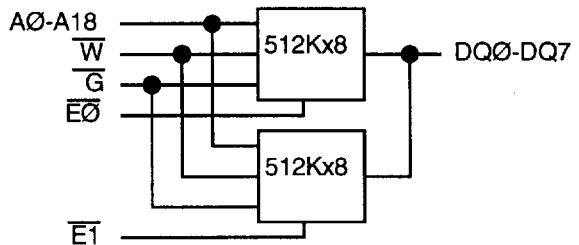
All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI9F81025C requires no clocks or refreshing for operation.

Pin Configurations and Block Diagram



Pin Names

A0-A18	Address Inputs
$\overline{E0-E1}$	Chip Enable
\overline{W}	Write Enable
\overline{G}	Output Enable
DQ0-DQ7	Common Data Input/Output
VCC	Power (+5V $\pm 10\%$)
VSS	Ground
NC	No Connection



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Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Power Dissipation	2 Watts
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 100pF

(note: For TEHOZ, TGHOZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power	ICC1	\bar{W} , I/O = 0mA, $\bar{E}0$ or $\bar{E}1 = VIL$, Min Cycle	--	60	85	mA
Supply Current		(Operating Current per Bank of 512K bits)				
Standby (TTL) Power	ICC2	$\bar{E} \geq VIH$, $VIN \leq VIL$	--	1	2	mA
Supply Current		$VIN \geq VIH$				
Full Standby Power	ICC3	$\bar{E} \geq VCC - 0.2V$			1	mA
Supply Current (CMOS)		$VIN \geq VCC - 0.2V$ or $VIN \leq 0.2V$		10	100	μA
Input Leakage Current	ILI	$VIN = 0V$ to VCC	-10		10	μA
Output Leakage Current	ILO	$V I/O = 0V$ to VCC	-10		10	μA
Output High Voltage	VOH	$IOH = -1.0mA$	2.4	--	--	V
Output Low Voltage	VOL	$IOL = 2.1mA$	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

\bar{G}	$\bar{E}0$	$\bar{E}1$	\bar{W}	Mode	Output	Power
X	H	H	X	Standby	High Z	ICC2 ICC3
H	H	L	H	Output Deselect	High Z	ICC1
H	L	H	H	Output Deselect	High Z	ICC1
H	L	L	H	Output Deselect	High Z	ICC1 ICC2
L	L	H	H	Read	DOUT (1st 512K)	ICC1
L	H	L	H	Read	DOUT (2nd 512K)	ICC1
L	L	L	X	Not Allowed	--	--
X	L	H	L	Write	DIN (1st 512K)	ICC1
X	H	L	L	Write	DIN (2nd 512K)	ICC1
X	L	L	L	Write	DIN (1st & 2nd 512K)	ICC1 ICC2

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	30	pF
Data Lines	CD/Q	30	pF
Chip Enable Line	CC	20	pF
Write and Output Enable Lines	CW	30	pF

These parameters are sampled, not 100% tested.

EDI9F81025C

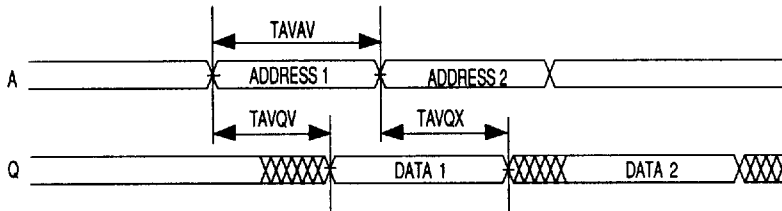
2x512x8 SRAM Module

AC Characteristics Read Cycle

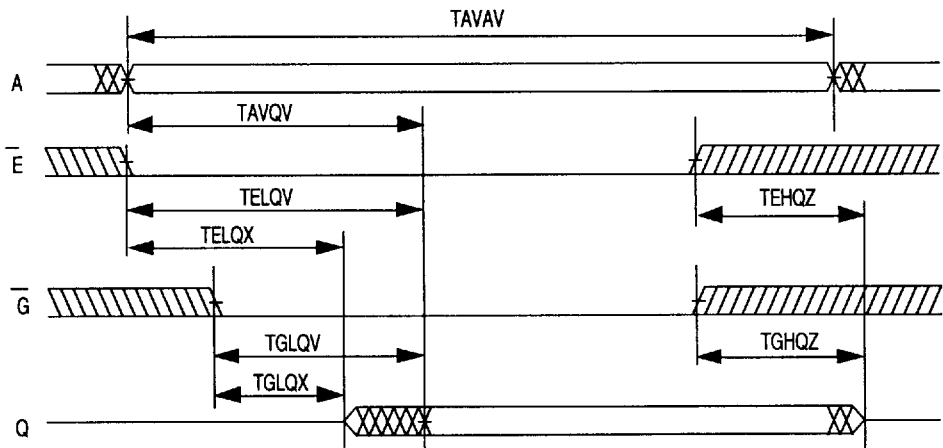
Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	70		85		100		ns
Address Access Time	TAVQV	TAA		70		85		100	ns
Chip Enable Access Time	TELQV	TACS		70		85		100	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		30		35		40	ns
Output Hold from Address Change	TAVQX	TOH	5		5		5		ns
Output Enable to Output Valid	TGLQV	TOE		40		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	5		5		5		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		30		35		40	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - W High, G, E Low



Read Cycle 2 - W High



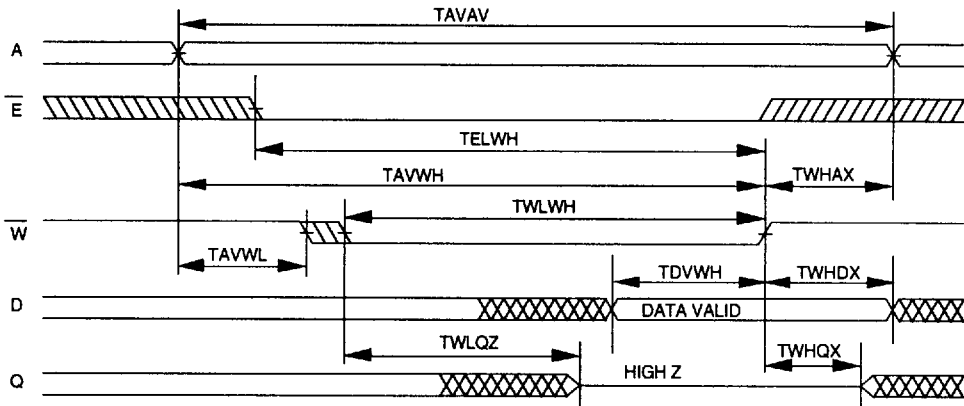
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AC Characteristics Write Cycle

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	70		85		100		ns
Chip Enable to End of Write	TELWH	TCW	65		70		80		ns
Address Setup Time	TELEH	TCW	65		70		80		ns
	TAVWL	TAS	0		0		0		ns
Address Valid to End of Write	TAVEL	TAS	0		0		0		ns
	TAVWH	TAW	65		70		80		ns
Write Pulse Width	TAVEH	TAW	65		70		80		ns
	TWLWH	TWP	65		70		80		ns
Write Recovery Time	TWLEH	TWP	65		70		80		ns
	TWHAX	TWR	5		5		5		ns
Data Hold Time	TEHAX	TWR	5		5		5		ns
	TWHDX	TDH	0		0		0		ns
Data to Write Time	TEHDX	TDH	0		0		0		ns
	TWLOZ	TWHZ	0	30	0	35	0	40	ns
Output Active from End of Write (1)	TDVWH	TDW	30		35		40		ns
	TDVEH	TDW	30		35		40		ns
Output Active from End of Write (1)	TWHQX	TWLZ							

Note 1: Parameter guaranteed, but not tested.

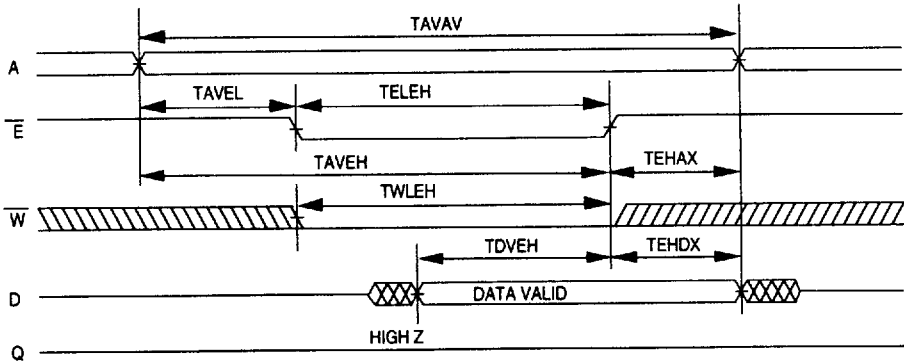
Write Cycle 1 - W Controlled



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2x512x8 SRAM Module

Write Cycle 2 - E Controlled



Data Retention Characteristics

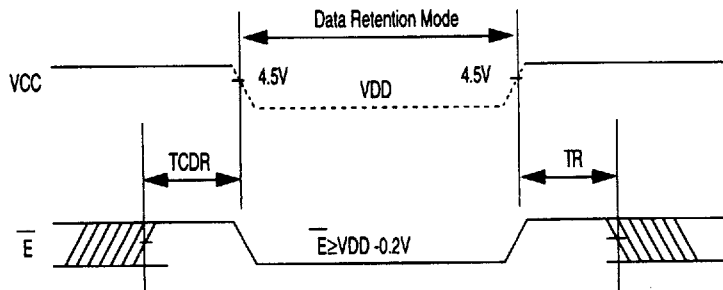
LP Version Only

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max		Unit
						70°C	85°C	
Data Retention Voltage	VDD	VDD= 0.2V		2	--	--	--	V
Data Retention Quiescent Current	ICCDR	$\bar{E} \geq VDD - 0.2V$	2V	--	10	60	100	μA
		$V_{IN} \geq VDD - 0.2V$	3V	--	20	90	150	μA
Chip Disable to Data Retention Time(1)	TCDR	or $V_{IN} \leq 0.2V$		0		--	--	ns
Operation Recovery Time (1)	TR			TAVAV*		--	--	ns

*Read Cycle Time

Note 1: Parameter guaranteed, but not tested.

Data Retention - E Controlled



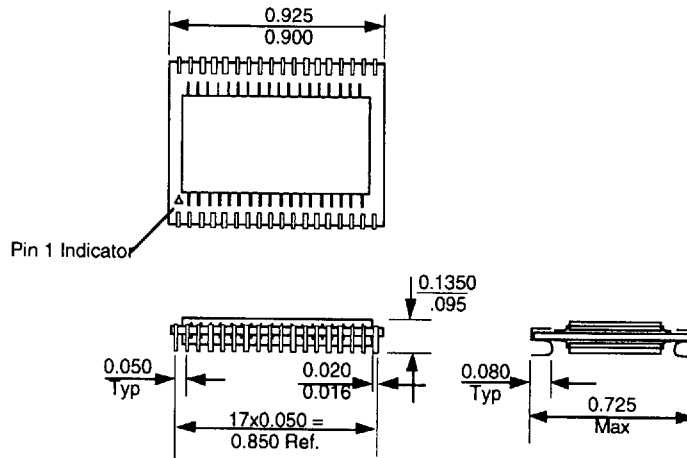
Ordering Information

Standard Power	Low Power with Data Retention	Speed (ns)	Package No.
EDI9F81025C70BPC	EDI9F81025LP70BPC	70	198
EDI9F81025C85BPC	EDI9F81025LP85BPC	85	198
EDI9F81025C100BPC	EDI9F81025LP100BPC	100	198

Note: To order an Industrial grade product substitute the letter C in the Suffix with the letter I, eg. EDI8F9F81025C70BPC becomes EDI9F81025C70BPI.

Package Description

Package No. 198 36 Lead SOIC Package



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