SFF-1063/1250N-SW PTH Serial Optical Transceiver Design & Layout Guide

Introduction

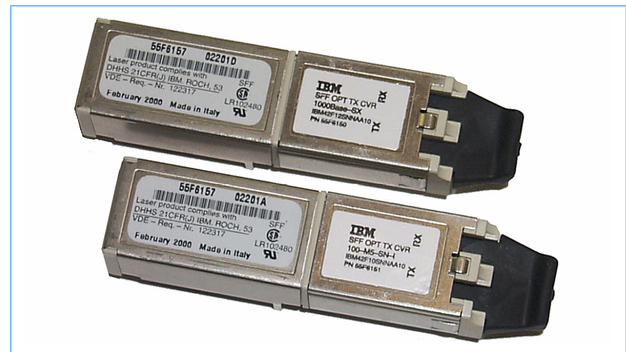
The SFF-1063/1250N-SW is a small form factor (SFF), plated through hole-type (PTH) serial optical transceiver for use at distances up to 1804.6ft/550m in high data rate applications including Fibre Channel Arbitrated Loop (FC-AL) and Gigabit Ethernet. The transceiver receives serial optical signals and converts them into serial electrical signals. Conversely, it also receives serial electrical signals and retransmits them as optical signals.

The transceiver uses 850nm short-wavelength light emitted by a vertical cavity surface emitter laser (VCSEL) and operates at 1.063Gbps (IBM42F10SNNAA20) in Fibre Channel applications and at 1.250Gbps (IBM42F12SNNAA20) in Gigabit Ethernet applications. The transceiver conforms to ANSI Fibre Channel specification FC-0 for short-wavelength operation (100-M5-SN-I) and conforms to draft 2 of the IEEE 802.3z 1000 Base-SX standard. The transceiver works with industry-standard "8b/10b" serializer/deserializer modules and incorporates circuits optimized for the 8b/10b protocol.

The transceiver uses outgoing and incoming fiber channel paths. The preferred fiber optic medium is 50/125mm multimode, duplex (dual) optical fiber cable. A 62.5/125mm multimode fiber can be substituted for shorter linking distances. Single-mode 10/125mm single-mode fiber should not be used. A duplex LC-style miniature connector is used for the fiber optic input, a direct follow-on to the duplex SC-style connector that has long been used with IBM GBIC products. However, the LC connector has been in service long enough to prove its reliability. The transceiver is a Class 1 laser-safe product. Under normal operation, optical power is at eyesafe levels. Cables can be connected and disconnected while the transceiver is in operation.

This application note should be used in conjunction with IBM engineering specification *1063/1250 MBd Small Form Factor Transceiver with Signal Detect,* available from the IBM Microelectronics web site at:

www.chips.ibm.com/techlib/products/fiberoptic/datasheets.html



Special Design Considerations

As noted in the following paragraphs, the transceiver requires design considerations different from that of previous industry transceiver devices, namely the GBIC and the 1x9.

Vcc Supply

In contrast to the IBM GBIC, which requires 5Vdc and has internally connected receiver and transmitter power pins, the transceiver requires 3.3Vdc for receive and transmit power, which is applied at pins 2 and 6 (Rx Power and Tx Power) of the transceiver, respectively (Figure 1). Pins 2 and 6 may be tied together or fed separately, however better isolation between transmit and receive signals can be obtained with separate power feeds.

Logic Levels

The transceiver is compatible with 3-volt PECL logic technology for high speed transmit and receive interfaces, and is compatible with 3-volt open-collector TTL technology for low speed logic lines.

AC Coupling

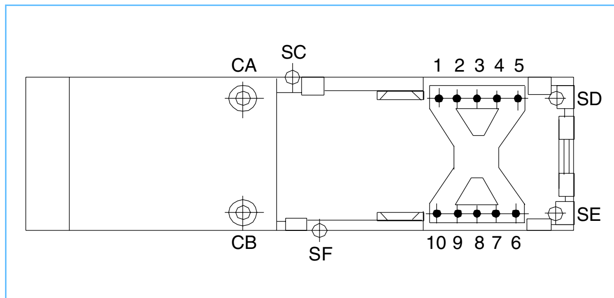
To ensure AC coupling between the transceiver and the host logic or SERDES module, a DC blocking capacitor is required in series with each of the two high speed input lines and each of the two high speed output lines.

Split-Chassis Grounds

The transceiver chassis is divided into two electrically isolated halves:

1. The half near the optical fiber is electrically floating and must be connected to chassis ground (pins CA and CB) for best electrical shielding.
2. The half near the signal pins is electrically connected to logic ground inside the transceiver. Pins SC through SF are electrically connected to pins 1 and 7 inside the SFF transceiver and should be connected to the host logic ground. See *Grounding Considerations* on page 3 for more information.

Figure 1: Pinout (Bottom View)



Pin Description

Pin	Name	Type
1	Rx Ground	Logic Ground
2	Rx Power	Power
3	Rx_SD+	Status Output
4	Rx_DAT-	Signal Output
5	Rx_DAT+	Signal Output
6	Tx Power	Power
7	Tx Ground	Logic Ground
8	Tx_Disable+	Control Input
9	Tx_DAT+	Signal Input
10	Tx_DAT-	Signal Input
CA	Chassis Ground	Chassis Ground
CB	Chassis Ground	Chassis Ground
SC	Logic Ground	Logic Ground
SD	Logic Ground	Logic Ground
SE	Logic Ground	Logic Ground
SF	Logic Ground	Logic Ground

Transmit/Receive Interface Impedance

Unlike the IBM GBIC, the SFF transceiver's high speed transmit (Tx_DAT) and receive (Rx_DAT) data lines have a characteristic line-to-line impedance of 100 ohms and a line-to-ground impedance of 50 ohms (GBIC and 1x9 transceiver devices have line-to-line and line-to-ground impedances of 150 and 75 ohms, respectively).

Physical Size

The transceiver occupies approximately half the volume of GBIC devices, making it possible to space optical fiber cable connections at about half the horizontal distance required for GBIC devices.

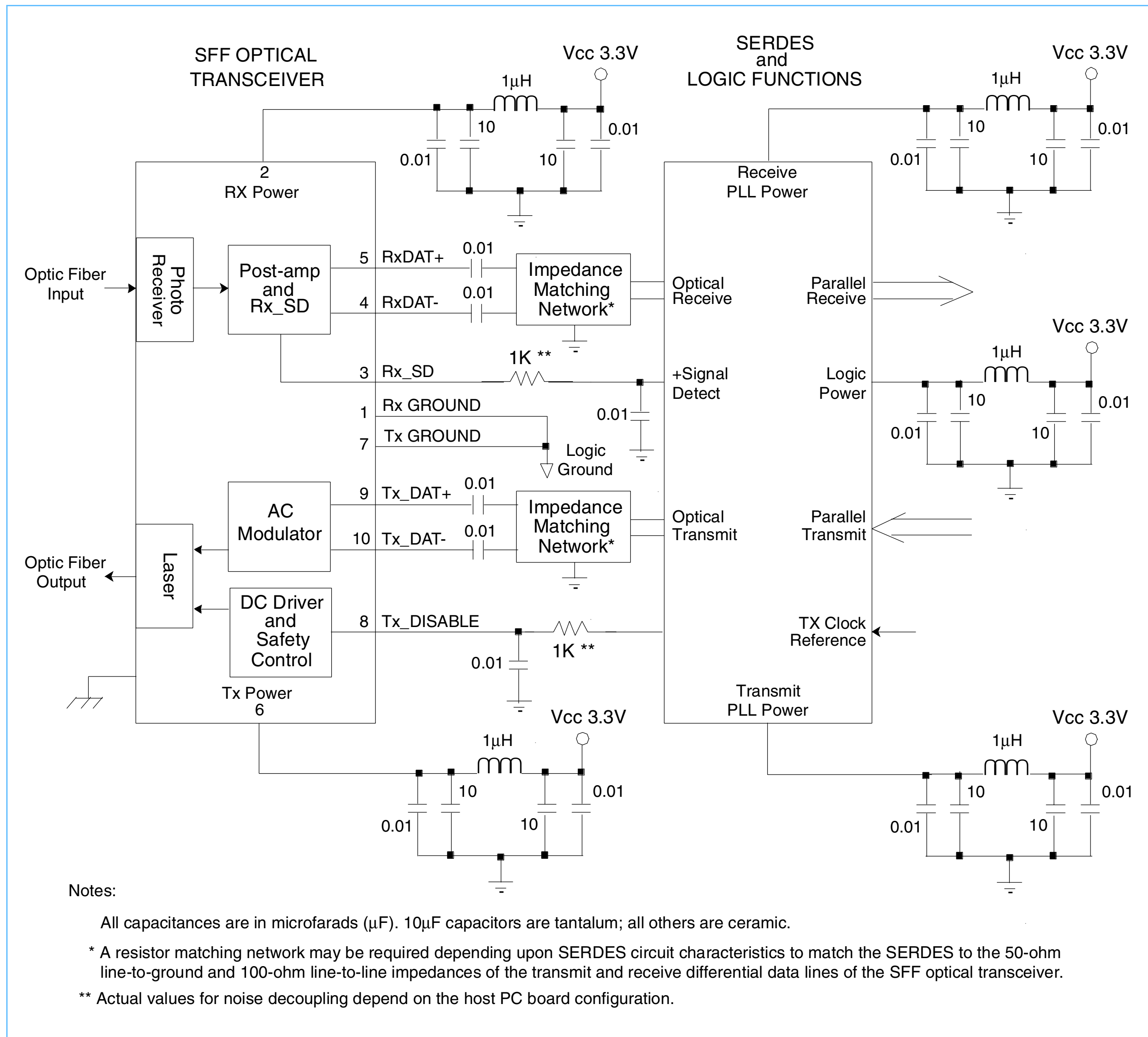
EMI/EMC/ESD

Data Paths

Because data rates on the lines to and from the SERDES module are near 1 GHz, the "fundamental" is approximately 0.5 GHz and includes both higher order harmonics and lower frequency "data noise." For best eye diagram characteristics, the transmit and receive data lines must make fast 1-0 and 0-1 transitions. Therefore, a somewhat rich array of frequencies is present in these lines. To reduce crosstalk, susceptibility, and radiation in high speed data lines, consider the following design approaches:

1. Keep data lines as short as possible. When lines approach 0.05 wavelength at 0.5 GHz (approximately 0.79in/2cm), serious consideration should be given to matching impedances with PC board stripline or microstrip transmission lines at 100 ohms line-to-line or 50 ohms line-to-ground plane (See *Appendix A: Stripline Transmission Lines* on page 6).
2. When transmission lines are not used, it is still important to terminate at the SERDES end with 100-ohm and 50-ohm equivalent impedances. Transmit and receive impedances of internal SERDES circuits must be considered when determining termination resistance.
3. Keep differential pairs parallel, closely spaced, and the same length. Avoid sharp corners in the path.Separate the input data line pairs from the output data line pairs as much as possible and route them above signal ground planes.
4. Particular care must be taken to space other wiring as far as practicable from data lines. Wiring traversing these lines should cross at right angles on the opposite side of the ground plane.
5. To reduce reflections and radiation, maintain uniform data line land widths. For example, avoid abrupt width discontinuities when connecting data lines to I/O connectors. Use gradual line width increases and decreases whenever possible.

Figure 2: Simplified Schematic



PC Boards

Because the transceiver employs isolated power islands, multilayer PC boards must be used in the host board design. Also, some designs require both chassis and logic grounds on the same board. Finally, high speed data line routing would be very difficult without a ground plane under the differential data pairs.

Grounding Considerations

Ground Tabs

The section of the transceiver chassis nearest the optical fiber connector has grounding tabs that must mesh firmly with the rectangular bezel cutout into which the transceiver is inserted. The bezel must be part of the main host chassis sheet metal or be well connected to the main chassis box through multi-point contacts. Grounding techniques must follow good UHF/microwave shielding practices. Excessive

EMI will be radiated through the bezel and bezel opening if the SFF transceiver does not make good multipoint contact to a well-grounded host bezel.

Pin Convention

At this time there is not complete agreement among optical transceiver manufacturers on the use of ground pins SC through SF. Some manufacturers do not offer split-chassis grounding, thus SC through SF are connected to a one-piece chassis. In this case, all ground pins CA through SF (although some pins might be omitted in some industry SFF products) are connected to box chassis ground. Some manufacturers omit SC through SF from the transceiver chassis, while others float CA and CB and retain SC through SF. IBM and several other manufacturers offer the split-chassis grounding scheme whereby the pins are internally connected to logic ground (See *Split-Chassis Grounds* on page 1.

Host PC board designers must consider these differences when choosing SFF transceiver suppliers. To maintain compatibility among the various manufacturers, pins SC through SF should be floated to separate the chassis and logic grounds. For designs using the IBM transceiver or an IBM-like transceiver exclusively, SC through SF along with pins 1 and 7 should be connected to chassis ground to provide maximum shielding and a ground connection for the high speed logic circuits.

Isolation

Good design practice normally suggests that chassis and logic grounds be tied together at only one point or in close proximity in an electrical system. Historically, this tiepoint has been at the power supply. However, when designing high speed digital transceiver circuits, one must also consider the effects EMI, EMC, and ESD in addition to traditional ground loop problems. To minimize the effects of crosstalk, radiation, etc., it is sometimes necessary to connect the grounds at an alternate point in the system. The proper design of system grounding is complex and therefore must be carefully considered during the early stages of system design, whether it be a small box or many interconnected units. A big advantage of optical fiber coupling is that from a complex system standpoint, grounding can be broken into electrically isolated boxes.

Because the logic and chassis grounds are normally tied together in the power supply, they should be isolated at the transceiver whenever possible to avoid ground loops. If this is not feasible, a 10-15 ohm resistor can be substituted for the direct connection at the power supply, with direct connection being made elsewhere in the chassis box. This grounding technique is currently being used by some computer manufacturers in their enclosure designs.

If the logic and chassis grounds are not tied together in the power supply, they can be joined at the communication ports to minimize ground loops. This approach requires the logic and chassis grounds to be tied together at the transceiver in split-chassis designs. Connecting the logic and chassis grounds at the communication ports has also proven effective in some designs to minimize EMI radiation and EMC/ESD susceptibility from the ports.

Enclosure

Because the host enclosure box uses copper interface cables and contains an exposed transceiver chassis, it poses the greatest risk for EMI/EMC/ESD problems. To minimize these effects, the enclosure must make good electrical contact with the conductive leaf springs around the opening for the transceiver chassis.

The opening must be in conductive material and be sized to match the dimensions shown in the 1063/1250 MBd Small Form Factor Transceiver with Signal Detect engineering specification. Enclosure ventilation holes must not exceed 0.157in/4mm in diameter, and internal wiring should be kept away from the holes.

Cables and Connectors

All metallic interface cables should be shielded or use in-line filters to prevent EMI and to provide good EMC/ESD compatibility. To support the use of unshielded cables outside the enclosure box, UTP or similar connectors must be used. When using unshielded cables, wiring inside the enclosure must be shielded and kept away from the transceiver to prevent EMI from radiating from the external interface cables.

Power Isolation

Transceiver Power Island

To reduce jitter and crosstalk through the power supply, a separate power island should be used to supply the transceiver. To create the island, power from Vcc should be fed through a pi-network LC filter consisting of a 1µH series inductor and a capacitor network on either side of the inductor connected to the PC board ground plane. The capacitor network consists of a parallel combination of one 0.01µF ceramic and one 10µF tantalum capacitor. Capacitors should be surface-mount, however components with extremely short leads may be used.

SERDES Power Islands

Some SERDES modules provide separate power pins for the transmit and receive phase locked loop circuits and the remainder of the module electronics. Each of these power domains should be isolated from the Vcc supply using the pi-network isolation method described in the previous paragraph. Depending on the host PC board layout and power supply characteristics, more high frequency (ceramic) and/or mid frequency (tantalum) bypass capacitors may be required. To increase capacitance, several capacitors should be paralleled rather than using a single large-value component to minimize inductance and ESR.

Logic Connections

The low speed Tx_Disable input and Rx_LOS output lines to and from the transceiver are open collector and TTL-compatible. RC deglitching should be used on the Tx_Disable line to desensitize it from electrical noise. Each connection of the high speed Tx_DAT+/Tx_DAT- and Rx_DAT+/Rx_DAT- differential line pairs between the transceiver and the SERDES module should be decoupled with a 0.01µF capacitor. These lines have no series DC decoupling capacitors inside the transceiver module.

Mechanical

Some mechanical force is required to connect and disconnect optical fiber cables from the enclosure box. Because this can exert mechanical forces on the host PC board, the transceiver-to-PC board and PC board-to-chassis mountings must be designed to handle the additional stress.

Cooling

The transceiver's power dissipation is quite low, but it is not zero. Because the transceiver package is small, some air flow around the device is required to maintain acceptable operating temperatures. Convection cooling may be used only when enough space exists around the transceiver to permit sufficient air flow.

Manufacturing Process

Because the transceiver is a non-wettable component, it must be soldered to the host PC board using a washless flux for both wave solder and hand solder processes. The protective cover shipped with the transceiver should not be removed during manufacturing assembly processes, otherwise dust and evaporative matter could contaminate the optical assemblies.

Reasonable care should taken to not expose the transceiver to ESD conditions during handling and particularly when inserting the device into the host PC board. The transceiver should be left in its conductive plastic packing until insertion, which should be done only under ESD-controlled conditions. Particular care must be taken in low-humidity environments.

Because of the very close tolerances required to mesh with the front bezel, it will probably be necessary to fixture all SFF transceiver modules during the host PC board soldering process.

Laser Safety

The optical laser used in the transceiver is a Class 1 laser-safe product. Monitoring and control circuits inside the transceiver help to ensure safe laser operation. However, the Class 1 safety rating is valid only when the host power supply Vcc remains below 4Vdc. Therefore, to ensure Class 1 safety operation of the laser, the Tx Power voltage must not exceed 4Vdc. The host power electronics must provide overvoltage protection to prevent Tx Power from exceeding 4Vdc.

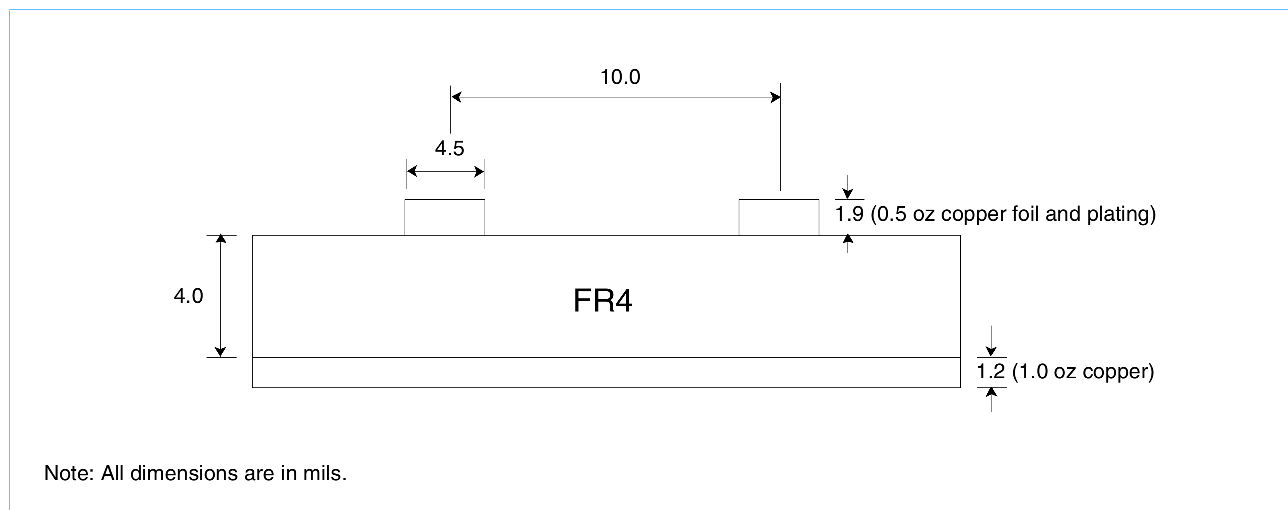
Appendix A: Stripline Transmission Lines

An example stripline transmission line configuration is shown in Figure 3. A similar layout can be used on host PC board designs for long high speed data lines. The example transmission line is built on a glass-epoxy (FR4) PC board. The dimensions shown are taken from a stripline incorporated into an IBM test card and are for reference only.

Mathematical modeling of stripline transmission characteristics is complex due to the interaction of multiple PC board properties and parameters. The example stripline has a line-to-line impedance of just over 100 ohms and a line-to-ground impedance considerably higher than 50 ohms. Although the IBM engineering specification *1063/1250 MBd Small Form Factor Transceiver with Signal Detect* and this application note state that high speed data lines must have an impedance of 100 ohms line-to-line and 50 ohms line-to-ground, it is not possible to build a practical stripline to meet these requirements.

In applications where high-speed data lines remain entirely on the host PC board, the more critical of the two impedances is 100 ohms line-to-line for the differential pair. To achieve this impedance for a practical stripline, the line-to-ground impedance of the differential pair must be considerably higher than 50 ohms.

Figure 3: Stripline Transmission Line Example



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