



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS 9-BIT REGISTER

ADVANCE INFORMATION
IDT54/74FBT823A
IDT54/74FBT823B
IDT54/74FBT823C

FEATURES:

- IDT54/74FBT823A equivalent to 54/74BCT823A
- IDT54/74FBT823B 25% faster than the 823A
- IDT54/74FBT823C 10% faster than the 823B
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- $\pm 10\%$ power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

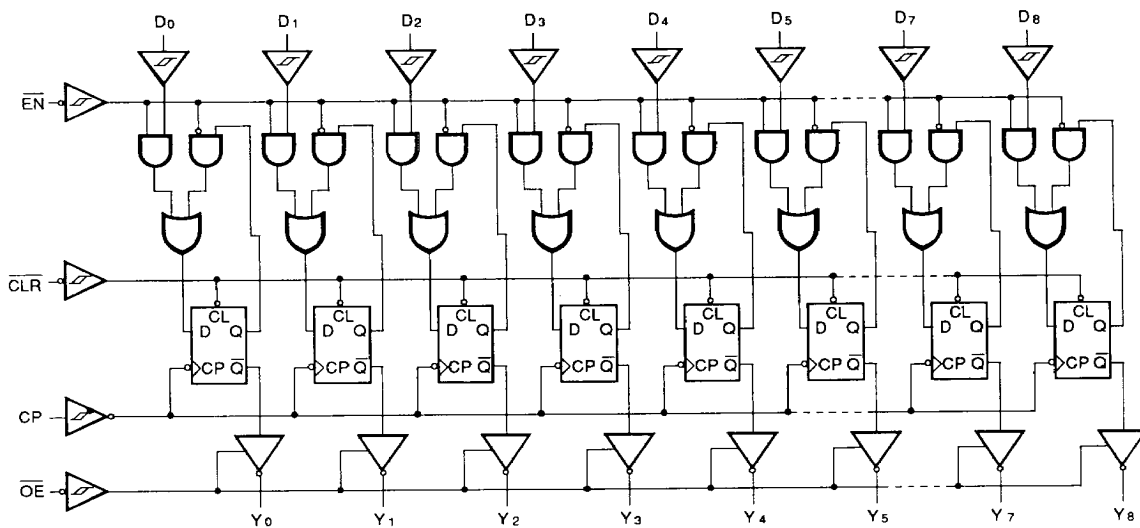
DESCRIPTION:

The FBT series of BiCMOS buffers and bus drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT823 is a 9-bit wide buffered register with Clock Enable (EN) and Clear (CLR). The '823 is ideal for parity bus interfacing in high-performance microprogrammed systems.

The FBT series of buffers are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM



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MILITARY AND COMMERCIAL TEMPERATURE RANGES

JUNE 1990

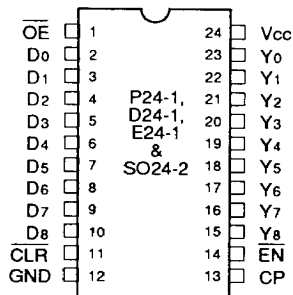
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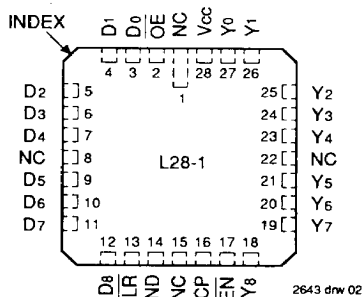
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PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Name	I/O	Description
D0-8	I	The D flip-flop data inputs.
CLR	I	For both inverting and non-inverting registers, when the clear input is LOW, the Qi outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y0- Y8	O	The register three-state outputs.
EN	I	Clock Enable. When the Clock Enable is LOW, data on the Di input is transferred to the Qi output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Qi outputs do not change state, regardless of the data or clock input transitions.
OE	I	Output Control. When the OE input is HIGH, the Yi outputs are in the high impedance state. When the OE input is LOW, the TRUE register data is present at the Yi outputs.

2643 tbl 05

FUNCTION TABLE⁽¹⁾

Inputs					Internal Outputs		Function
OE	CLR	EN	Di	CP	Qi	Yi	
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:

1. H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

2643 tbl 06

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTE: 2643 tbl 01

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2643 tbl 02

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C, Vcc = 5.0V ± 10%; Military: TA = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I _{IH}	Input HIGH Current	Vcc = Max., V _I = 2.7V	—	—	10	μA
I _{IL}	Input LOW Current	Vcc = Max., V _I = .5V	—	—	-10	μA
I _{OZH}	High Impedance	Vcc = Max. Vo = 2.7V	—	—	50	μA
I _{OZL}	Output Current	Vo = .5V	—	—	-50	μA
I _I	Input HIGH Current	Vcc = Max., V _I = 5.5V	—	—	100	μA
V _{IK}	Clamp Diode Voltage	Vcc = Min., I _N = -18mA	—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	Vcc = Max., V _O = GND ⁽³⁾	-75	—	-225	mA
V _{OH}	Output HIGH Voltage	Vcc = Min. VIN = VIH or VIL I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.4	3.3	—	V
		I _{OH} = -18mA MIL. I _{OH} = -24mA COM'L.	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 32mA MIL. I _{OL} = 48mA COM'L.	—	0.3	0.5	V
V _H	Input Hysteresis	Vcc = 5V	—	200	—	mV
I _{OFF}	Bus Leakage Current	Vcc = 0V, V _O = 4.5V	—	—	100	μA
I _{CC}	Quiescent Power Supply Current	Vcc = Max. VIN = GND or Vcc	—	0.2	1.5	mA

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

2643 tbl 05

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	$V_{CC} = \text{Max.}, \text{Outputs Open}$ $V_{IN} = 3.4V^{(3)}$		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}, \text{Outputs Open}$ $\overline{OE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_i = 10\text{MHz}, 50\% \text{ Duty Cycle}$ $\overline{OE} = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	—	4.0	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	—	5.0	
		$V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_i = 2.5\text{MHz}, 50\% \text{ Duty Cycle}$ $\overline{OE} = \text{GND}$ Eight Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	—	7.2 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	—	16.2 ⁽⁵⁾	

2643 b1 04

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient, and maximum loading.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	IDT54/74FBT823A				IDT54/74FBT823B				IDT54/74FBT823C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Clock to Y _i (OE = LOW)	CL = 50pF RL = 500Ω	—	10	—	—	—	7.5	—	—	—	6.0	—	—	ns
tsu	Data to CP Set-up Time		7	—	—	—	3	—	—	—	3	—	—	—	ns
tH	Data CP Hold Time		1.5	—	—	—	1.5	—	—	—	1.5	—	—	—	ns
tsu	Enable (EN) to CP Set-up Time		6	—	—	—	3	—	—	—	3	—	—	—	ns
tH	Enable (EN) to CP Hold Time		0	—	—	—	0	—	—	—	0	—	—	—	ns
tPHL	Propagation Delay, Clear to Y _i		—	12	—	—	—	9	—	—	—	8.0	—	—	ns
tREM	Clear Recovery (CLR)Time		6	—	—	—	6	—	—	—	6	—	—	—	ns
tw	Clock Pulse Width		7	—	—	—	6	—	—	—	6	—	—	—	ns
tw	Clear (CLR=LOW) Pulse Width		6	—	—	—	6	—	—	—	6	—	—	—	ns
tPZH tPZL	Output EnableTime OE to Y _i		—	12	—	—	—	8	—	—	—	7.0	—	—	ns
tPHZ tPLZ	Output Disable Time OE to Y _i		—	8	—	—	—	7.5	—	—	—	6.5	—	—	ns

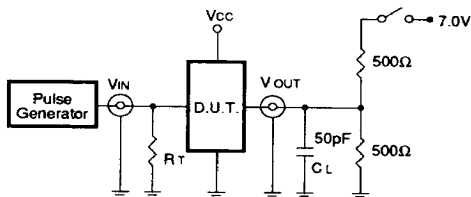
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2643 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

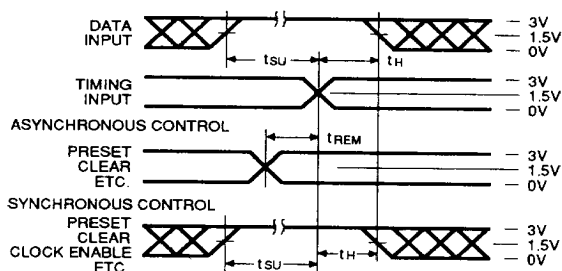
DEFINITIONS:

C_L = Load capacitance; includes jig and probe capacitance.

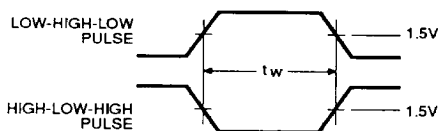
R_T = Termination resistance; should be equal to Z_{out} of the Pulse Generator.

2643 btl 08

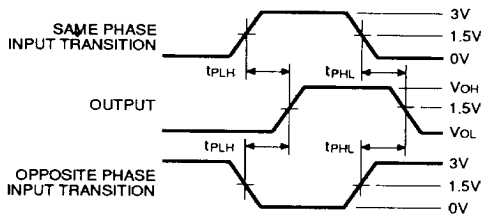
SET-UP, HOLD AND RELEASE TIMES



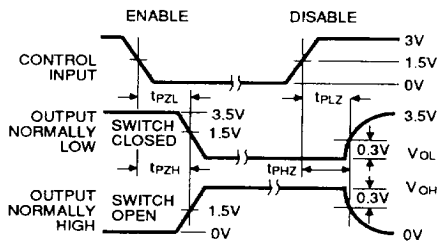
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

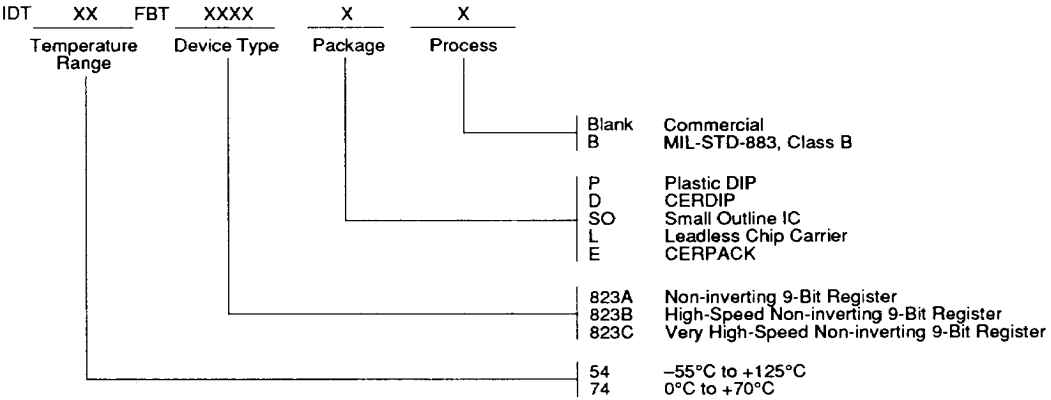


NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_o \leq 50\Omega$; $t_r \leq 2.5$ ns; $t_r \leq 2.5$ ns.

2643 drw 04

ORDERING INFORMATION



2643 d/w 03