

DATA SHEET

OQ2545HP; OQ2545BHP **SDH/SONET STM16/OC48** **laser drivers**

Product specification
Supersedes data of 1997 Nov 27
File under Integrated Circuits, IC19

1999 Aug 24

SDH/SONET STM16/OC48 laser drivers

OQ2545HP; OQ2545BHP

FEATURES

- Differential 50 Ω inputs for direct connection to Current-Mode Logic (CML) outputs
- Internal retiming to minimize jitter (OQ2545HP only)
- Input clock phase margin of 320° at 2.5 Gbits/s (OQ2545HP only)
- RF output current sinking capability of 60 mA
- Bias output current sinking capability of 100 mA
- TTL compatible control inputs
- Loop mode for system testing
- Continuous output monitoring
- Power dissipation <1500 mW (for typical application)
- Low cost LQFP48 plastic package.

APPLICATIONS

- Digital fibre optical modulation driver in STM16/OC48 short, medium and long haul optical transmission systems
- Optical modulation driver in high-speed data networks
- High current driver for electro-optical converters
- High current electrical line driver.

GENERAL DESCRIPTION

The OQ2545 is a driver IC intended to be used with a directly modulated laser diode or with an Electro Absorption Modulator (EAM) in SDH/SONET 2.5 Gbits/s optical transmission systems.

The IC features differential data inputs. Loop mode inputs are provided for system testing, along with an output for continuous monitoring. In addition, the OQ2545HP features differential clock inputs for internal retiming resulting in a better jitter performance.

The IC has bias and modulating current outputs, the levels of which can be set separately. As an additional safety measure, the active HIGH-level input for automatic laser shutdown (pin ALS) can be used to switch off the laser modulation and bias currents.

Although the IC is intended for 2.5 Gbits/s optical transmission systems, it can be used in any application requiring high current drive at high frequencies.

The IC is transparent from input to output.

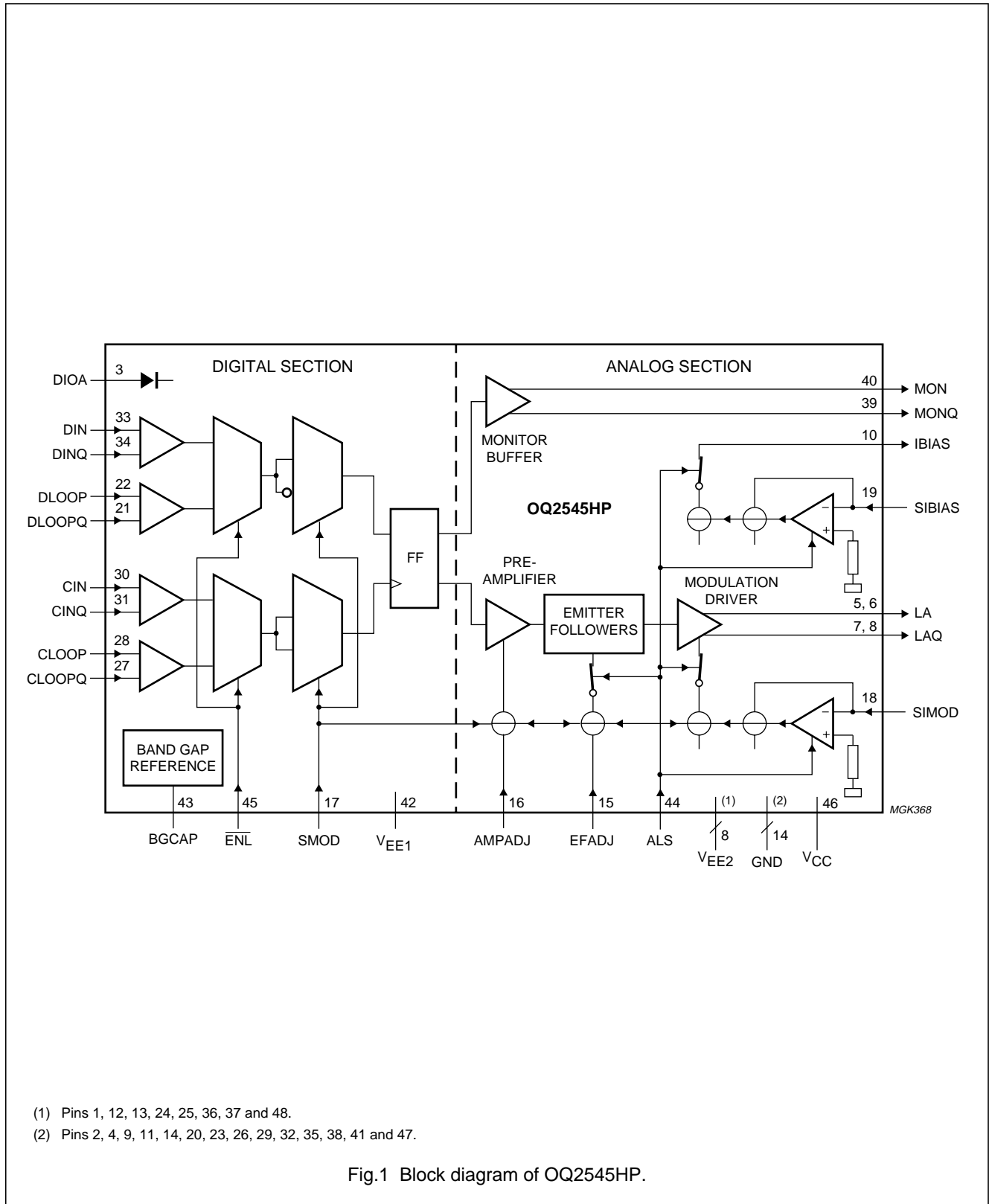
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ2545HP	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
OQ2545BHP			

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BLOCK DIAGRAMS



SDH/SONET STM16/OC48 laser drivers

OQ2545HP; OQ2545BHP

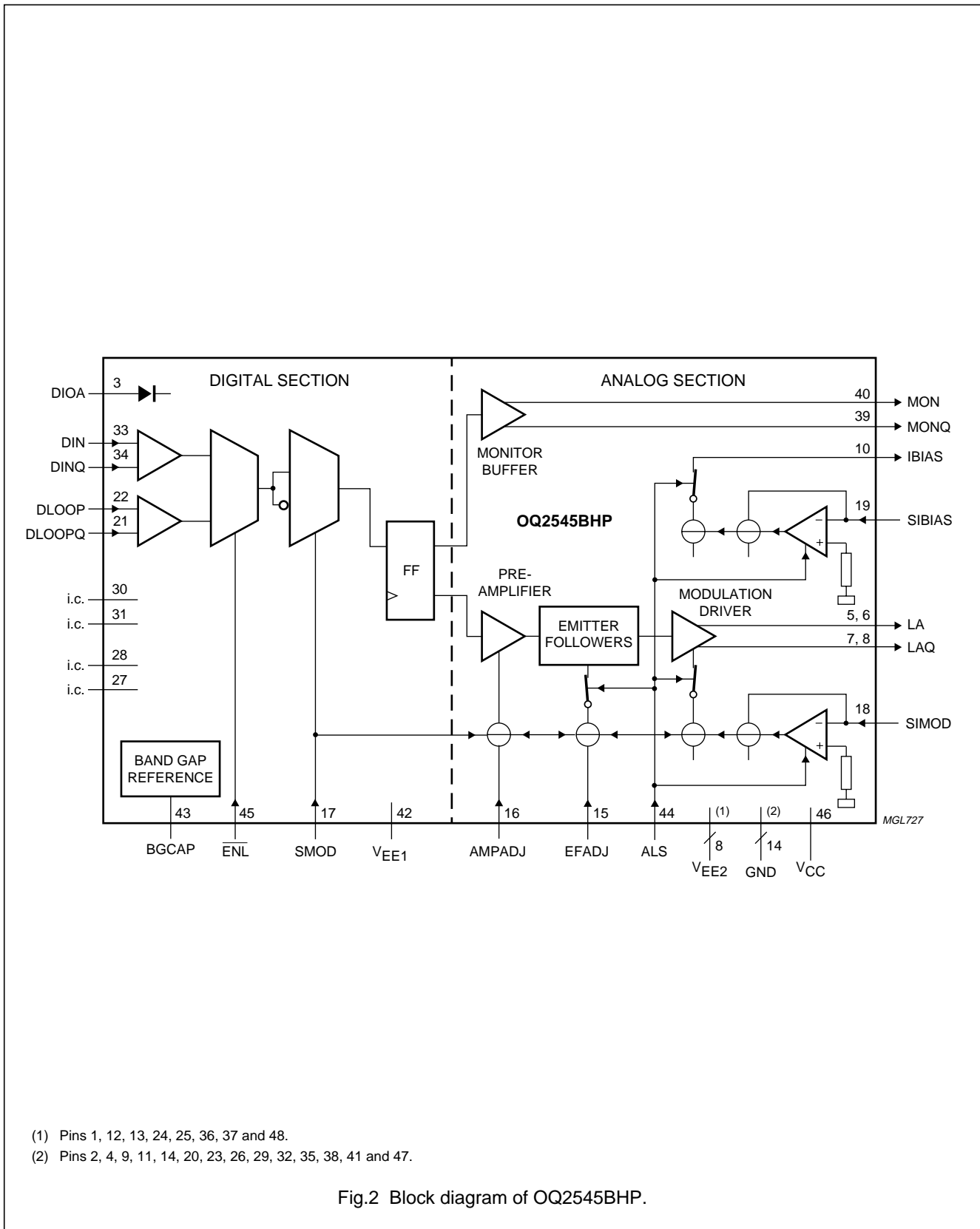


Fig.2 Block diagram of OQ2545BHP.

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OQ2545HP; OQ2545BHP

PINNING

SYMBOL	PIN		TYPE ⁽¹⁾	DESCRIPTION
	OQ2545HP	OQ2545BHP		
V _{EE2}	1	1	S	supply voltage for analog section (–6.5 V)
GND	2	2	S	ground supply
DIOA	3	3	A	temperature sensing diode array connection
GND	4	4	S	ground supply
LA	5	5	O	laser modulation current output
LA	6	6	O	laser modulation current output
LAQ	7	7	O	inverted laser modulation current output
LAQ	8	8	O	inverted laser modulation current output
GND	9	9	S	ground supply
IBIAS	10	10	O	laser bias current control output
GND	11	11	S	ground supply
V _{EE2}	12	12	S	supply voltage for analog section (–6.5 V)
V _{EE2}	13	13	S	supply voltage for analog section (–6.5 V)
GND	14	14	S	ground supply
EFADJ	15	15	AI	input for emitter follower current adjustment
AMPADJ	16	16	AI	input for preamplifier current adjustment
SMOD	17	17	I	input for data polarity switch
SIMOD	18	18	I	input for RF modulated output current control
SIBIAS	19	19	I	input for DC output current control
GND	20	20	S	ground supply
DLOOPQ	21	21	I	inverted loop mode data input
DLOOP	22	22	I	loop mode data input
GND	23	23	S	ground supply
V _{EE2}	24	24	S	supply voltage for analog section (–6.5 V)
V _{EE2}	25	25	S	supply voltage for analog section (–6.5 V)
GND	26	26	S	ground supply
CLOOPQ	27	–	I	inverted loop mode clock input
i.c.	–	27	–	internally connected; internal resistance of 50 Ω to GND
CLOOP	28	–	I	loop mode clock input
i.c.	–	28	–	internally connected; internal resistance of 50 Ω to GND
GND	29	29	S	ground supply
CIN	30	–	I	clock input
i.c.	–	30	–	internally connected; internal resistance of 50 Ω to GND
CINQ	31	–	I	inverted clock input
i.c.	–	31	–	internally connected; internal resistance of 50 Ω to GND
GND	32	32	S	ground supply
DIN	33	33	I	data input
DINQ	34	34	I	inverted data input

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SYMBOL	PIN		TYPE ⁽¹⁾	DESCRIPTION
	OQ2545HP	OQ2545BHP		
GND	35	35	S	ground supply
V _{EE2}	36	36	S	supply voltage for analog section (-6.5 V)
V _{EE2}	37	37	S	supply voltage for analog section (-6.5 V)
GND	38	38	S	ground supply
MONQ	39	39	O	inverted monitor data output
MON	40	40	O	monitor data output
GND	41	41	S	ground supply
V _{EE1}	42	42	S	supply voltage for digital section (-4.5 V)
BGCAP	43	43	A	connection for band gap reference decoupling capacitor
ALS	44	44	I	automatic laser shutdown control input
ENL	45	45	I	loop mode enable input (active LOW)
V _{CC}	46	46	S	positive supply voltage for TTL interface (+5 V)
GND	47	47	S	ground supply
V _{EE2}	48	48	S	supply voltage for analog section (-6.5 V)

Note

1. Pin type abbreviations: O = output, I = input, S = power supply and A = analog function.

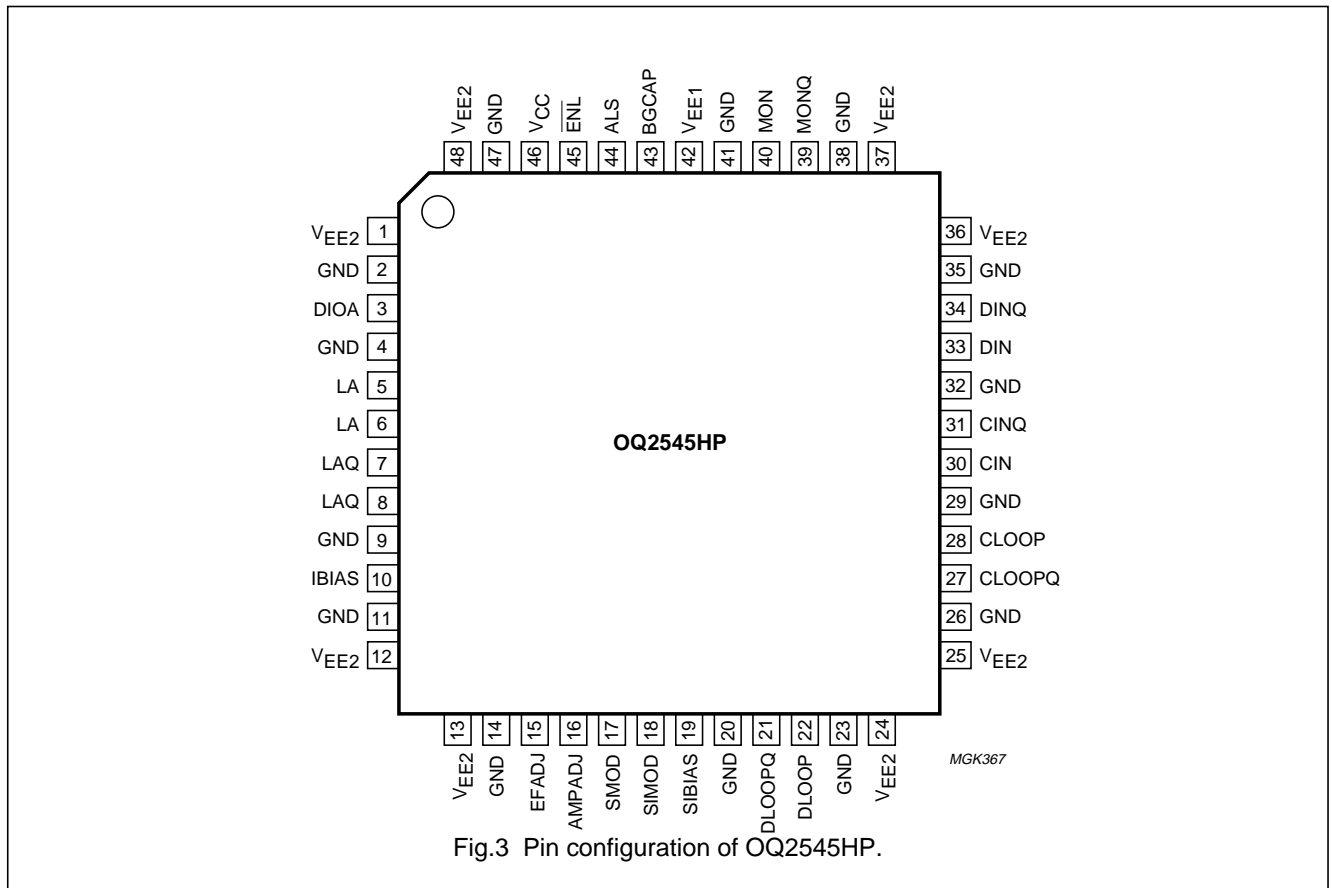


Fig.3 Pin configuration of OQ2545HP.

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OQ2545HP; OQ2545BHP

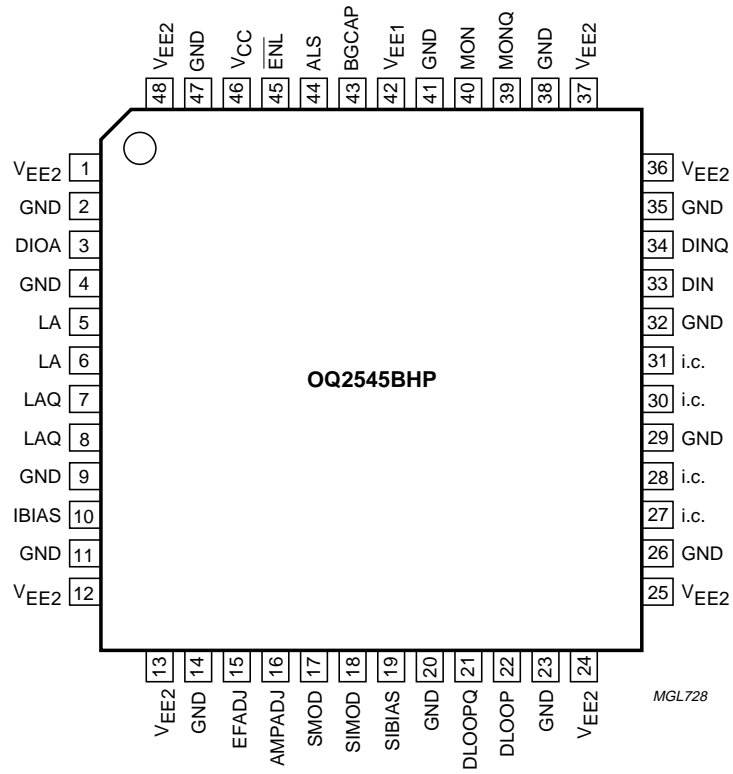


Fig.4 Pin configuration of OQ2545BHP.

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OQ2545HP; OQ2545BHP

FUNCTIONAL DESCRIPTION

The OQ2545(B)HP can be divided into two functional blocks (see Fig.1):

- A digital section on the input side
- An analog section on the output side.

The data input buffers present an impedance of 50 Ω to the data stream on the differential data inputs (see Fig.5). The input data is then fed to a multiplexer where normal mode (pin ENL = HIGH-level) or loop mode (pin ENL = LOW-level) inputs are selected. For driving an EAM, a second multiplexer inverts the input signals when pin SMOD is connected to VEE1.

An external clock (OQ2545HP only) connected to a master-slave flip-flop is then used to retiming the data. This reduces jitter on the data signal to a minimum.

The preamplifier boosts the signal to a suitable level for the modulation driver. Two emitter followers provide the necessary signal isolation between the preamplifier and the high current modulation driver. The bias currents for the preamplifier and the emitter followers contain an output level dependent component, along with an independent component. The output level dependent component is controlled via the signal on pin SIMOD and the operational amplifier, which also sets the modulation driver level. The independent component is adjusted by means of the signal on pin AMPADJ (preamplifier) and pin EFADJ (emitter followers).

The signal on pin AMPADJ also controls the shape of the output signal on pins LA and LAQ.

An independent adjustable on-chip bias current source is provided to drive directly a modulated laser diode. Pin SIBIAS is used to set the bias current level. The output current at pin IBIAS will be approximately 106 times the input current at pin SIBIAS. A similar arrangement is used to control the modulation current at pins LA and LAQ. The output current at pins LA and LAQ is proportional to the input current at pin SIMOD. The coefficient depends on the load impedance on pins LA and LAQ and on the voltage setting of pin SMOD (see section 'Modulation current setting').

Pin ALS is a TTL compatible input and at HIGH-level it can be used to switch off all current sources. This function makes it possible to implement safety measures that will switch off the circuit in the event of an optical system malfunction.

The buffered differential 50 Ω outputs (pins MON and MONQ) can be used to monitor the optically modulated data.

Loop mode

The loop mode is provided for system testing. A LOW-level on pin ENL selects the loop mode. When pin ENL is left open-circuit, it is pulled to a HIGH-level (TTL) by an internal pull-up resistor.

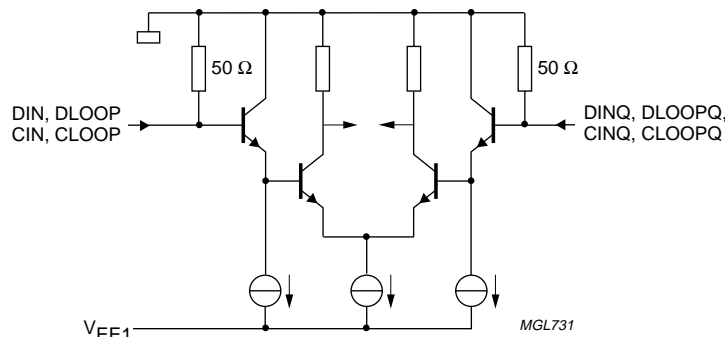


Fig.5 Schematic for CML differential inputs.

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Automatic laser shutdown

A HIGH-level (TTL) on pin ALS switches off the laser modulation and bias currents. This function allows the circuit to be switched off in the event of an optical system malfunction or for system maintenance. When not connected, pin ALS is pulled to a LOW-level (TTL) by an internal pull-down resistor.

Data monitoring

Pins MON and MONQ can be used as data monitor outputs. They need to be AC-coupled, e.g. to a 50 Ω matched RF amplifier with sufficient bandwidth.

Output polarity selection

Pin SMOD is used to set the correct logic assignment between the data input on pins DIN and DINQ (or pins DLOOP and DLOOPQ) and the data output on pins LA, LAQ, MON and MONQ. This is necessary because a directly modulated laser diode and an EAM have different output voltage requirements.

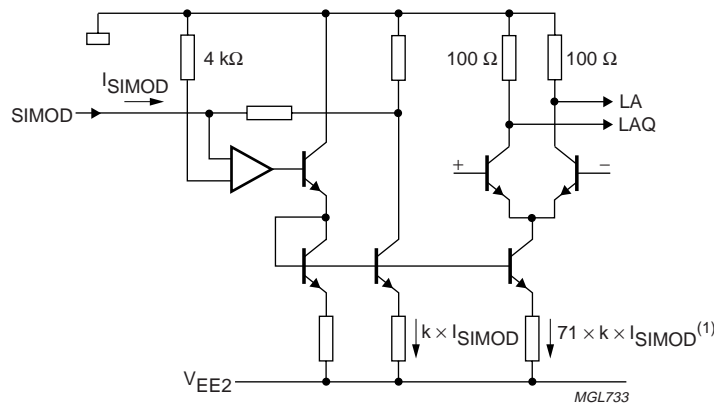
If a laser diode is used and connected between pin LA and ground, a high current through pin LA corresponds to a logic HIGH, while a low current through pin LA corresponds to a logic LOW.

The opposite is the case with an EAM, where a high current (i.e. a large voltage across the load) activates the EAM, thereby causing a logic LOW. Therefore, an inversion is needed between input and output. This happens in the second multiplexer when pin SMOD is connected to V_{EE1} . When left open-circuit, pin SMOD is pulled-up to ground, which is the laser diode setting.

Modulation current setting

Pin SIMOD is used to adjust the modulation current on pins LA and LAQ (see Fig.6). This is achieved by regulating the internal current mirror, which serves as a reference current for the modulation driver. The reference port of the control operational amplifier is connected to ground through an internal 4 kΩ resistor, thus establishing a ‘virtual earth’ on pin SIMOD (DC level is 0 V). An external (approximately) 4 kΩ resistor connected to an adjustable voltage source is needed to regulate the internal current mirror. This adjustable voltage source can be a part of the laser current control box (see Fig.15).

The ratio between the current into pin SIMOD and the total modulation current depends on the polarity setting via pin SMOD. When pin SMOD = 0 V the value of $I_{mod} = 92 \times I_{SIMOD}$ (approximately) and whereas pin SMOD = V_{EE1} the value of $I_{mod} = 107 \times I_{SIMOD}$ (approximately).



(1) $k = 1.3$ when pin SMOD = 0 V.
 $k = 1.5$ when pin SMOD = V_{EE1} .

Fig.6 Schematic of laser modulation outputs.

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Due to the internal resistors of 100 Ω between pins LA and LAQ to GND, a part of the total modulation current I_{mod} flows internally (see Fig.7). Therefore the modulation current can be written as: $I_{mod} = I_{LA(int)} + I_{LA(ext)}$.

The ratio is: $\frac{I_{LA(int)}}{I_{LA(ext)}} = \frac{R_{LA}}{100}$ where R_{LA} is the external impedance between pins LA and GND.

A similar argument holds for pin LAQ, with an external impedance of R_{LAQ} .

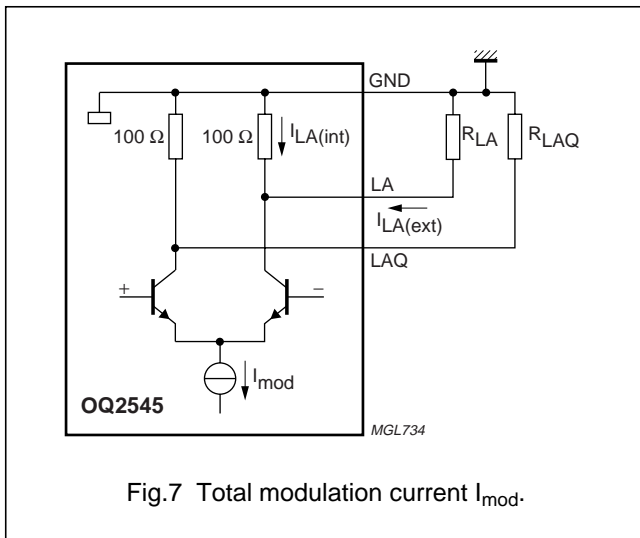


Fig.7 Total modulation current I_{mod} .

Bias current setting

An independent adjustable on-chip bias current source is provided for when the IC is driving directly a modulated laser diode. Pin SIBIAS is used to adjust the bias current at pin IBIAS, in a similar arrangement to that used for adjusting the modulation current. The reference port of the control operational amplifier is connected to ground through an internal 4 kΩ resistor, thus establishing a 'virtual earth' on pin SIBIAS (DC-level of 0 V). An adjustable voltage source connected to pin SIBIAS through an (approximately) 4 kΩ resistor is used to regulate the internal current mirror. The maximum output current of 100 mA is achieved with an input voltage of 4 V. In this case, the input current at pin SIBIAS is approximately 1 mA.

Band gap decoupling capacitor

The band gap voltage on pin BGCAP should be decoupled to V_{EE1} with an external 10 nF capacitor to minimize noise. It cannot be used as an external reference voltage for other circuits.

Preamplifier bias current adjustment

The bias current for the preamplifier contains a modulation dependent component and a modulation independent component. The modulation dependent current is adjusted via pin SIMOD. The modulation independent current will be adequate under normal circumstances. However, in some applications it may be necessary to customize the shape of the modulation current. This can be done by adjusting the preamplifier bias current via pin AMPADJ. When this pin is left open-circuit, the bias current is 0.5 mA and when this pin is connected to ground, the maximum bias current will be approximately 2.5 mA. A resistor can be connected between pin AMPADJ and ground to adjust the current level within this range. The bias current can be decreased by connecting a resistor between pins AMPADJ and V_{EE2} . However, care should be taken as the preamplifier will not be able to drive the modulation driver when the bias current is too low.

Emitter follower bias current adjustment

The bias currents for the emitter followers contain two components: a modulation independent component and a modulation dependent component to be controlled via pin SIMOD. The modulation independent currents (8.2 and 16.4 mA, respectively) are sufficient to ensure the emitter followers operate correctly under normal circumstances. In some applications, however, the eye pattern needs to be optimized. This is achieved by connecting an external resistor between pin EFADJ and ground. When pin EFADJ is connected directly to ground, the maximum currents for the two emitter followers will be approximately 25 and 50 mA, respectively. Because the emitter followers buffer the signal from the preamplifier, the current range to be adjusted via pin EFADJ depends on the setting via pin AMPADJ.

Grounding and power supply decoupling

The ground connection on the PCB needs to be a large copper area fill connected to a common ground plane with as low inductance as possible. The large area fill will improve the heat transfer to the PCB and so aiding cooling of the IC.

The power supply pins need to be decoupled using chip capacitors mounted as close as possible to the IC. To avoid high frequency resonance, multiple bypass capacitors should not be mounted at the same location. To minimise low frequency switching noise in the vicinity of the IC, the power supply line should ideally be filtered once using an LC circuit with a low cut-off frequency.

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RF connections

A coupled stripline or microstrip with an odd mode characteristic impedance of 50 Ω (nominal value) should be used for the differential RF connections on the PCB. This applies to the CML differential line pairs on pins CIN and CINQ, DIN and DINQ, CLOOP and CLOOPQ, DLOOP and DLOOPQ, and MON and MONQ.

In addition, the following lines should not differ in length by more than 10 mm:

- Lines to pins DIN, DINQ, CIN and CINQ
- Lines to pins CLOOP, CLOOPQ, DLOOP and DLOOPQ.

ESD protection

In order to achieve high frequency performance, it has been necessary to make adjustments to the standard ESD protection scheme. Inputs on pins DIN, DINQ, CIN, CINQ, DLOOP, DLOOPQ, CLOOP and CLOOPQ and outputs on pins MON and MONQ are protected by a reduced ESD structure. The outputs on pins LA and LAQ have **no protection** against ESD, so extra care should be taken with these pins.

Power consumption

The total power consumption of the OQ2545(B)HP depends strongly on the application. A rough guideline is given to estimate the power consumption for a specific application.

The total power dissipation (P_{tot}) consists of the following terms:

$$P_{tot} = P_{VEE1} + P_{VCC} + P_{VEE2} - (P_{LA} + P_{LAQ} + P_{IBIAS})$$

where

1. P_{VEE1} and P_{VCC} represent the power consumption terms corresponding with the supplies V_{EE1} and V_{CC} , required for the digital section and the TTL interfaces. These 2 terms are application independent and only depend on the process spread and supply voltages. Values can be found in Chapter "Characteristics".
2. $P_{VEE2} = I_{EE2} \times |V_{EE2}|$ represents the power consumption of the analog section, including the modulation current and bias current. It is mainly determined by the magnitude of the modulation current and bias current and the additional biasing currents of the preamplifier and emitter followers. The supply current is the summation:

$$I_{EE2} = 55 \text{ mA} + 1.5 \times I_{mod} + I_{IBIAS} + 3 \times I_{AMPADJ} + 55 \times I_{EFADJ}$$

where I_{AMPADJ} and I_{EFADJ} are the currents through pins AMPADJ and EFADJ, respectively.

These figures are valid for nominal supply voltage and temperature and are given for rough indication only.

3. P_{LA} , P_{LAQ} and P_{IBIAS} represent the dissipation in the external load (laser or EAM), caused by the modulation and bias current. The expressions are:

$$P_{LA} = 0.5 \times I_{LA(ext)} \times |V_{LA}|,$$

$$P_{LAQ} = 0.5 \times I_{LAQ(ext)} \times |V_{LAQ}| \text{ and}$$

$$P_{IBIAS} = I_{IBIAS} \times |V_{IBIAS}|.$$

The factor 0.5 represents the fact that, for a (scrambled) random data pattern, the modulation switch will be switched to either side 50% of the time integrated over many cycles.

V_{LA} and V_{LAQ} are the voltages on pins LA and LAQ when the modulation current flows through pins LA and LAQ, respectively and the values depend on the external laser or EAM supply voltage, the forward diode voltage drop and additional loads.

To increase the dissipation in the external load and thereby decreasing the dissipation in the IC, the values of $|V_{LA}|$ or $|V_{LAQ}|$ can be increased by adding additional external resistors. A minimum value of V_{LA} and V_{LAQ} is required for proper operation of the IC.

A similar argument is valid for power consumption due to the bias current. It should be noted that this is important, because it provides an easy way to lower the power dissipation of the IC.

Example

Consider the following example to illustrate the calculation of P_{tot} . A laser diode operates at 0.3 mW (optical low) and 3 mW (optical high), i.e. an extinction ratio of 10 dB.

For this laser type this requires $I_{IBIAS} = 20 \text{ mA}$ and $I_{LA(ext)} = 40 \text{ mA}$ (see Fig.8).

The series resistance of the laser is 30 Ω . Therefore the

$$\text{ratio is: } \frac{I_{LA(int)}}{I_{LA(ext)}} = \frac{30}{100}$$

Consequently, a total $I_{mod} = (130/100) \times 40 = 52 \text{ mA}$ will be generated by the IC.

The impedance connected to pin LAQ is 30 Ω as well. As a result also $I_{LAQ(ext)} = 40 \text{ mA}$ and $I_{LAQ(int)} = 12 \text{ mA}$ (see Fig.9).

In first instance the eye pattern is of adequate quality and the preamplifier and emitter follower do not need additional bias current, i.e. pins AMPADJ and EFADJ can be left open-circuit.

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The current I_{BIAS} is supplied through an RF choke with a high RF resistance and a low DC resistance (e.g. 5 Ω). When the laser is in the high (emitting) state, the voltage drop across the diode and the modulation current of 40 mA in combination with the bias current of 20 mA through the 30 Ω laser resistance results in:

$$V_{LA} = -1.2 - 30 \times (0.040 + 0.020) = -3.0 \text{ V}$$

No current through the 30 Ω resistor gives $V_{LAQ} = 0 \text{ V}$.

When the laser is in the low (dark) state, the bias current of 20 mA results in $V_{LA} = -1.2 - 30 \times 0.020 = -1.8 \text{ V}$

The modulation current of 40 mA through the 30 Ω resistor sets the value $V_{LAQ} = 30 \times 0.040 = -1.2 \text{ V}$

The RF choke causes V_{IBIAS} to be stationary and equal to the average value of V_{LA} minus the small voltage drop across the choke (bias current of 20 mA through 5 Ω):
 $V_{IBIAS} = 0.5 \times (-3.0 - 1.8) - 0.020 \times 5 = -2.5 \text{ V}$

Table 1 Estimate total power consumption

$P_{V_{EE1}}$	$70 \text{ mA} \times 4.5 \text{ V}$	315 mW
$P_{V_{CC}}$	$2 \text{ mA} \times 5 \text{ V}$	10 mW
$P_{V_{EE2}}$	$153 \text{ mA}^{(1)} \times 6.5 \text{ V}$	995 mW
P_{LA}	$0.5 \times 40 \text{ mA} \times 3.0 \text{ V}$	60 mW
P_{LAQ}	$0.5 \times 40 \text{ mA} \times 1.2 \text{ V}$	24 mW
P_{IBIAS}	$20 \text{ mA} \times 2.5 \text{ V}$	50 mW
P_{tot}	$P_{V_{EE1}} + P_{V_{CC}} + P_{V_{EE2}} - (P_{LA} + P_{LAQ} + P_{IBIAS})$	1186 mW

Note

- $153 \text{ mA} = I_{EE2} (55 + 1.5 \times 52 + 20 + 3 \times 0 + 55 \times 0)$.

Thermal requirements and cooling

The maximum allowed junction temperature for normal operation is 125 $^{\circ}\text{C}$. With an application specific estimated power dissipation and the maximum ambient temperature, the required thermal resistance from junction to ambient $R_{th(j-a)}$ can be derived. This value strongly depends on the PCB layout for the IC. It is highly recommended to use copper area fills around the 8 corner leads (pins V_{EE2}) of the IC. If a single copper layer PCB with a copper thickness of 0.034 mm is used, square copper area fills of $10 \times 10 \text{ mm}$ around the corner leads will result in an approximate value for $R_{th(j-a)} = 35 \text{ K/W}$. This value originates from model calculations and is for indication only. Lower values for $R_{th(j-a)}$ can be obtained with multilayer PCBs.

If the required power dissipation is not known, but the maximum ambient temperature is fixed, the maximum allowed dissipation as a function of $R_{th(j-a)}$ can be derived,

namely:
$$P_{tot} = \frac{125 - T_{amb(max)}}{R_{th(j-a)}}$$

The maximum allowed dissipation to prevent overheating as a function of the thermal resistance that is achieved in the application is shown in Fig.12.

The maximum ambient temperature in this application is 85 $^{\circ}\text{C}$ (i.e. $125 - 85 = 40 \text{ }^{\circ}\text{C}$ temperature head room). A low $R_{th(j-a)}$ is recommended.

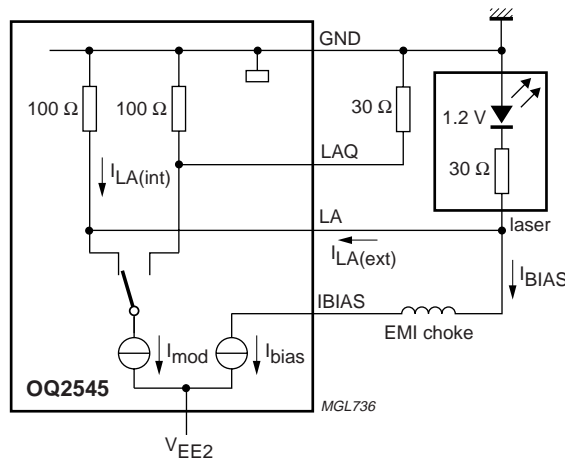


Fig.8 Laser high 'light emitting'.

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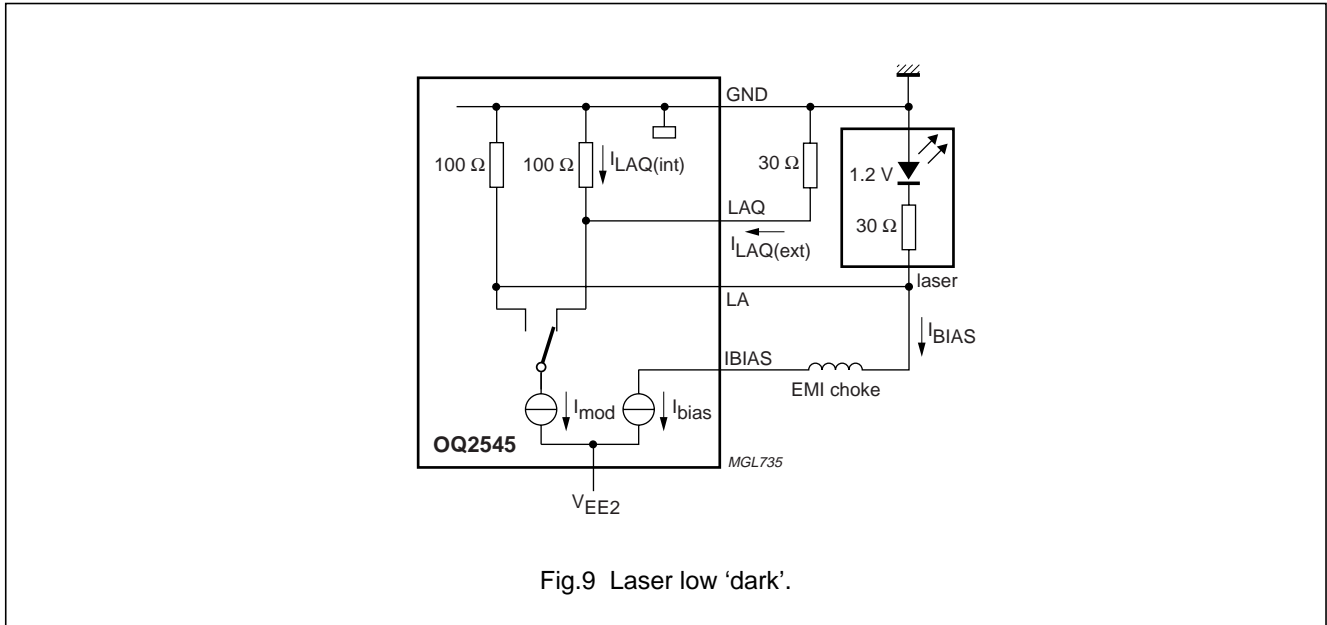


Fig.9 Laser low 'dark'.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V _{CC}	supply voltage for TTL interface	-0.5	+6.0	V
V _{EE1}	supply voltage for digital section	-6.0	+0.5	V
V _{EE2}	supply voltage for analog section	-7.5	+0.5	V
V _n	DC voltage on pins DIN, DINQ, DLOOP, DLOOPQ, CIN, CINQ, CLOOP and CLOOP pins MON and MONQ pins ALS and ENL pins EFADJ, APADJ, SIMOD and SIBIAS pins SMOD and BGCAP	-1.0 -2.0 -0.5 V _{EE2} - 0.5 V _{EE1} - 0.5	+0.5 +0.5 V _{CC} + 0.5 0.5 0.5	V V V V V
I _n	DC current on pins LA and LAQ pin IBIAS pins MON and MONQ pin DIOA	- - - -	80 110 20 10	mA mA mA mA
T _j	junction temperature	-	150	°C
T _{stg}	storage temperature	-65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th(j-s)}	thermal resistance from junction to solder point	27	K/W

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CHARACTERISTICSMeasured at typical supply voltages; all outputs with 50 Ω load; $T_{amb} = -40$ to $+85$ °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	supply voltage for TTL interface		4.75	5.0	5.25	V
V_{EE1}	supply voltage for digital section		-4.75	-4.5	-4.25	V
V_{EE2}	supply voltage for analog section		-6.85	-6.5	-6.15	V
I_{CC}	supply current for TTL interface		-	2	3	mA
I_{EE1}	supply current for digital section	OQ2545HP	-	70	90	mA
		OQ2545BHP	-	50	70	mA
I_{EE2}	supply current for analog section	normal operation; note 1	-	275	-	mA
		laser shutdown	-	5	8	mA
P	power dissipation	maximum bias and modulation current; note 2	-	1984	-	mW
		laser shutdown	-	350	-	mW
T_{amb}	ambient temperature		-40	-	+85	°C
T_j	junction temperature		-	-	125	°C
CML data and clock inputs: pins DIN, DINQ, DLOOP, DLOOPQ, CIN, CINQ, CLOOP and CLOOPQ; note 3						
$V_{i(p-p)}$	input voltage (peak-to-peak value)		100	250	500	mV
V_{IO}	input offset voltage		-25	0	+25	mV
V_I	DC input voltage		-600	-200	+250	mV
Z_i	input impedance	single-ended	40	50	60	Ω
TTL input: pin ENL; note 4						
V_{IL}	LOW-level input voltage		-	0.4	0.8	V
V_{IH}	HIGH-level input voltage		2.4	4.0	-	V
I_{IL}	LOW-level input current		-500	-	0	μ A
I_{IH}	HIGH-level input current		0	-	250	μ A
TTL input: pin ALS; note 4						
V_{IL}	LOW-level input voltage		-	0.4	0.8	V
V_{IH}	HIGH-level input voltage		2.4	4.0	-	V
I_{IL}	LOW-level input current		-90	-	0	μ A
I_{IH}	HIGH-level input current		0	-	600	μ A
t_{res}	response time	note 5	-	-	1.5	ms
Current source control inputs: pins SIMOD and SIBIAS; note 6						
K_{bias}	bias current converter coefficient	note 7	-	120	-	-
K_{mod}	modulation current converter coefficient	diode (SMOD = 0 V)	-	92	-	-
		EAM (SMOD = V_{EE1})	-	106	-	-
B	bandwidth of unity gain amplifier	note 9	-	10	-	MHz
ΔG	gain peaking	note 10	-	1	6	dB
SR	slew rate		-	4	-	V/ μ s

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Preamplifier adjustment: pin AMPADJ						
I_I	input control current		–	–	3	mA
Emitter follower adjustment: pin EFADJ						
I_I	input control current		–	–	3	mA
Band gap decoupling connection: pin BGCAP						
V_{BGCAP}	band gap decoupling voltage	note 11	–2.05	–1.6	–1.25	V
Temperature diodes: pin DIOA						
V_{DIOA}	temperature diode voltage	note 12	1.6	2.0	2.5	V
Laser modulation outputs: pins LA and LAQ; note 13						
I_{OL}	LOW-level output current	note 14	5	–	60	mA
I_{OH}	HIGH-level output current		–	–	2	mA
$I_{O(off)}$	output current during laser shutdown		–	–	200	μ A
V_O	output voltage		–3.5	–	0	V
δ	duty factor	note 15	43	50	57	%
t_r	rise time	note 16	–	155	200	ps
t_f	fall time	note 16	–	160	200	ps
$J_{o(p-p)}$	output jitter (peak-to-peak value)		–	15	40	ps
Z_o	output impedance	single-ended	80	100	120	Ω
BR	bit rate	note 17	–	2.48832	–	Gbits/s
Bias current output: pin IBIAS						
I_O	output current	note 18	1	–	100	mA
$I_{O(off)}$	output current during laser shutdown		–	–	200	μ A
V_O	output voltage	note 19	–5.5	–	0	V
Monitor outputs: pins MON and MONQ						
$V_{o(p-p)}$	output voltage (peak-to-peak value)		70	115	160	mV
V_O	DC output voltage		–	–1.4	–	V
Z_o	output impedance	single-ended	40	50	60	Ω
Clock phase margin: pins CIN and CINQ (OQ2545HP only); see Fig.13						
$T_{cy(CIN)}$	CIN cycle time		–	402	–	ps
t_{su}	set-up time		100	20	–	ps
t_h	hold time		100	20	–	ps
φ_m	clock phase margin		180	320	–	deg

Notes

1. Value is based on:

- External modulation current of 60 mA through an external load of 33 Ω and an internal modulation current of 20 mA giving a total modulation current of 80 mA.
- Bias current is 100 mA.
- Pins AMPADJ and EFADJ are left open-circuit.

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2. Value based on:
 - a) External modulation current of 60 mA and internal modulation current of 20 mA giving a total modulation current of 80 mA.
 - b) Bias current is 100 mA; see Section "Power consumption" for details on application specific power dissipation.
 - c) Pins AMPADJ and EFADJ are left open-circuit.
 - d) Pins LA and LAQ both terminated with 33 Ω .
3. See Fig.10 for CML symbol definitions. All CML inputs are terminated internally using 50 Ω on-chip resistors to ground.
4. Since the TTL inputs are static, no timing specifications are given in this data sheet.
5. The response time is the time it takes the laser currents (I_{LA} and I_{BIAS}) to fall below 1 mA after pin ALS = HIGH-level.
6. The values are valid for capacitive loads of up to 50 pF connected to these input pins; voltage controlled with 3.9 k Ω source resistance.
7.
$$\kappa_{bias} = \frac{I_{IBIAS}}{I_{SIBIAS}}$$
8.
$$\kappa_{mod} = \frac{I_{mod}}{I_{SIMOD}}$$
 where I_{mod} is the total (internal + external) modulation current.
9. The current converters consist of operational amplifiers used as unity gain amplifiers and current mirrors. The specified characteristics apply for the transfer function from pin SIMOD to pins LA and LAQ or from pin SIBIAS to pin IBIAS.
10. Although the operational amplifiers are configured as unity gain amplifiers, the response tends to peak close to the roll-off area.
11. To suppress supply noise in the band gap, an external capacitor of 10 nF can be connected between this pin and V_{EE1} .
12. Three series connected diodes have been integrated for measuring the junction temperature. The anode of this diode array is connected to pin DIOA. The cathode is connected internally to V_{EE2} . With a current of 1 mA, the anode voltage (measured with reference to V_{EE2}) will be somewhere within the specified range, depending on temperature. This voltage will show a -6 mV/ $^{\circ}$ C gradient over temperature.
13. Values are measured electrically and unfiltered (see Fig.11):
 - a) Pins AMPADJ and EFADJ are left open-circuit for all measurements.
 - b) The external load is 33 Ω on pins LA and LAQ.
 - c) The external modulation current is 60 mA.
 - d) Optical rise and fall times, duty factor and jitter depend on the applied filtering and the matching network between pins LA and LAQ and the optical device used.
14. The currents flowing into pins LA and LAQ are not equal to the internal RF modulation current because of an additional current in the internal termination resistance.
15. Duty factor is defined as $\frac{t_{WH}}{T_{cy}} \times 100\%$ The data stream should be '010101010101...'
16. Rise and fall times are between 10% and 90% of the peak values.
17. All RF tests are done at 2.48832 Gbits/s (STM16/OC48 rate).
18. The DC current into pin IBIAS is not equal to the internal DC current because of an additional current from the internal termination resistors.
19. To avoid saturation of the current source on pin IBIAS, the voltage level on pin IBIAS should never be allowed to fall below the specified minimum.

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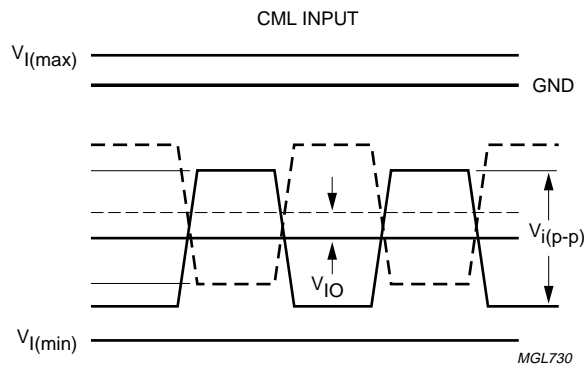


Fig.10 Logic level symbol definitions for CML inputs.

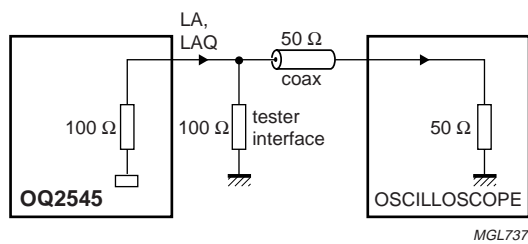
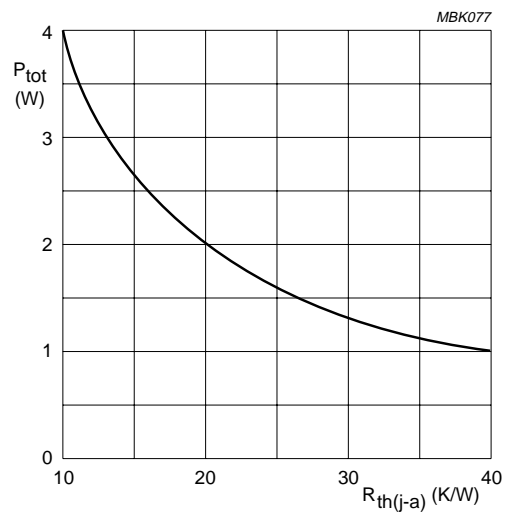


Fig.11 Set-up for electrical measurement of RF parameters.



Measured at $T_{amb} = 85^\circ\text{C}$.

Fig.12 Maximum power dissipation as a function of the thermal resistance.

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TIMING CHARACTERISTICS

Input timing (OQ2545HP only)

Set-up and hold time definitions are illustrated in Fig.13. The timing characteristics are applicable in both normal and loop modes.

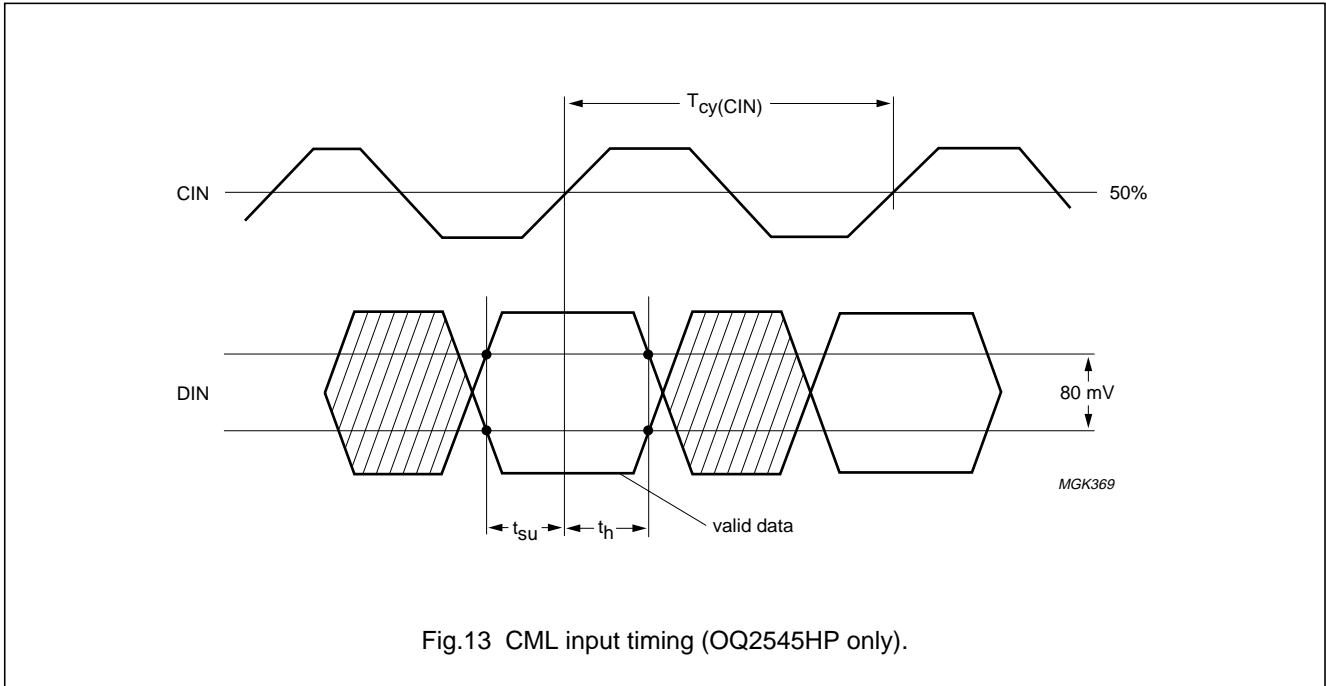


Fig.13 CML input timing (OQ2545HP only).

Output timing

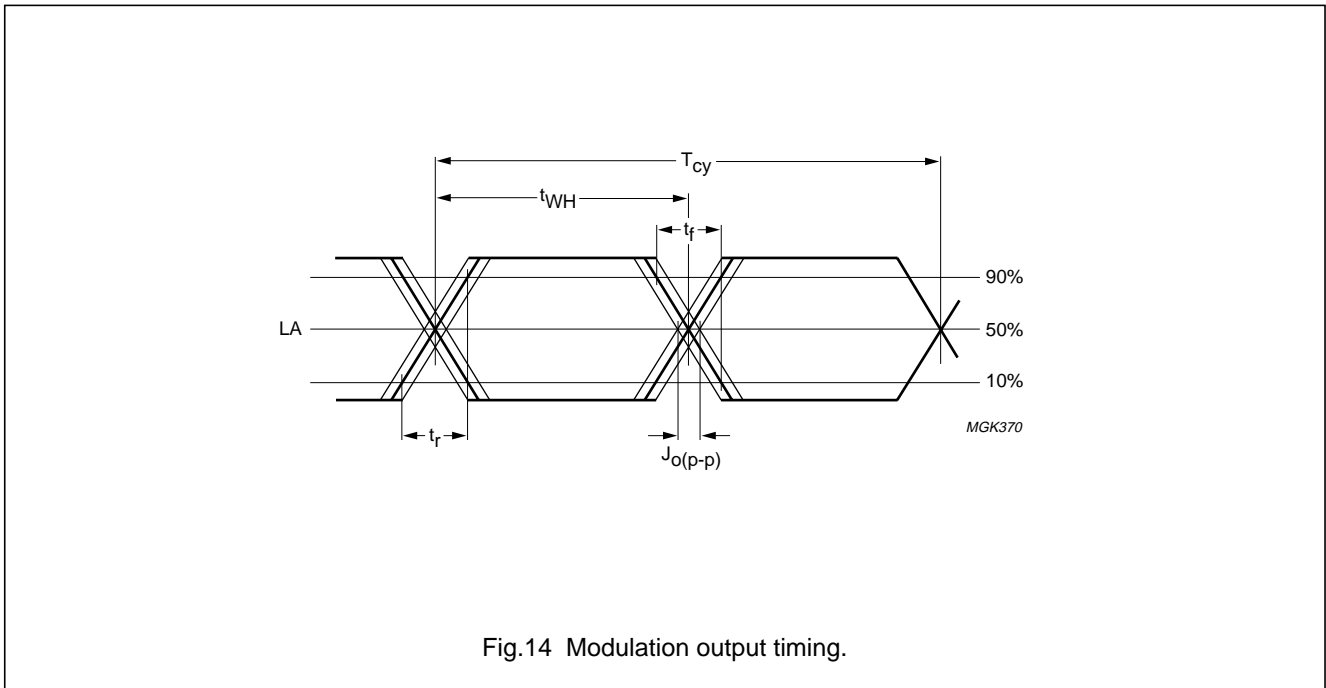
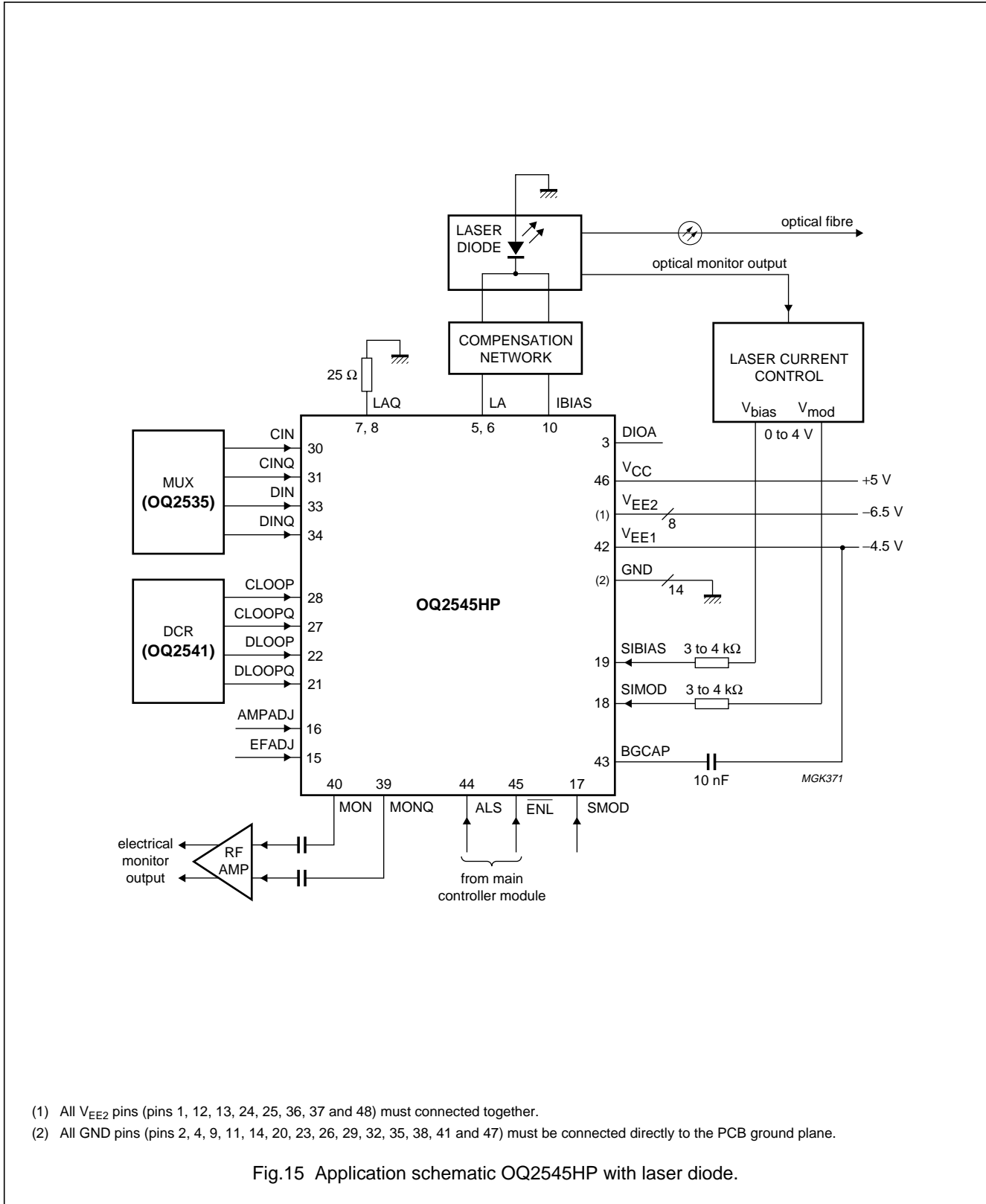


Fig.14 Modulation output timing.

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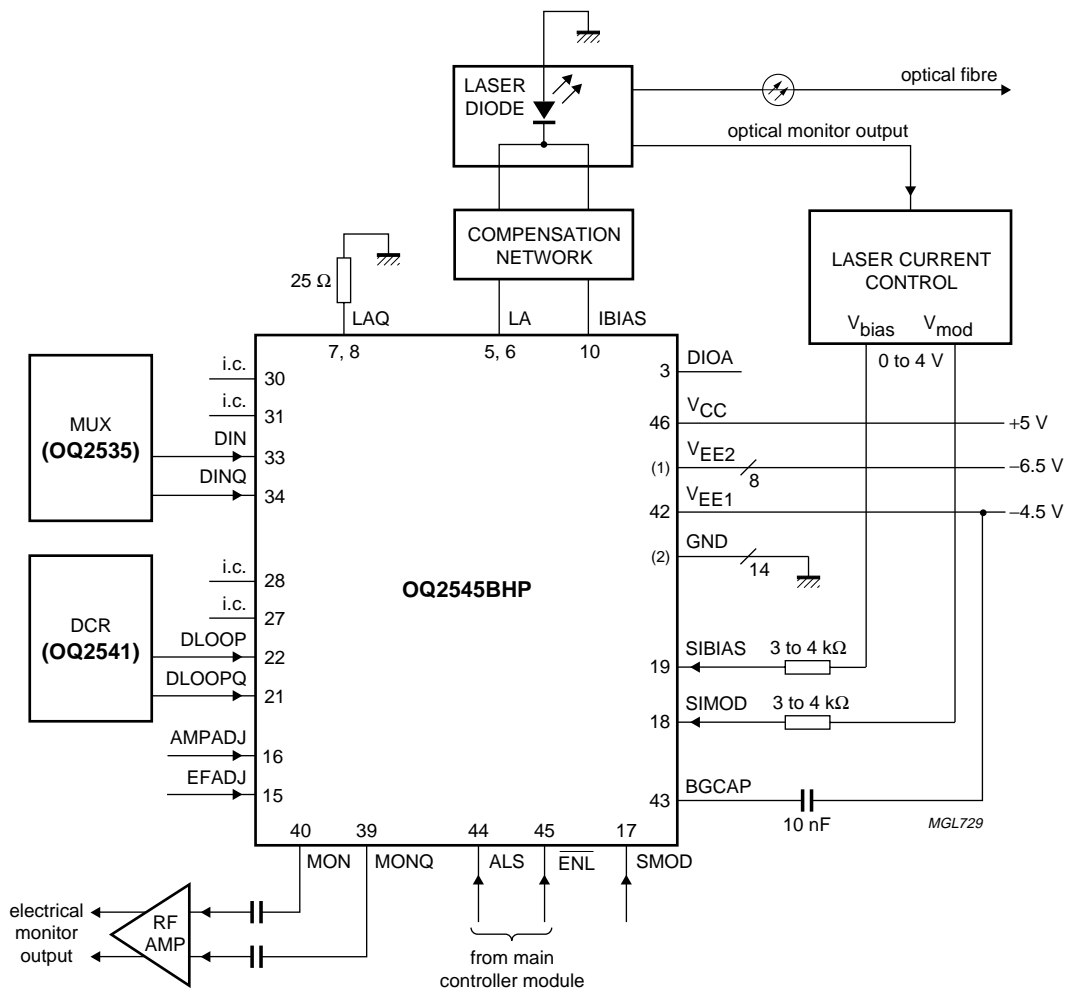
OQ2545HP; OQ2545BHP

APPLICATION INFORMATION



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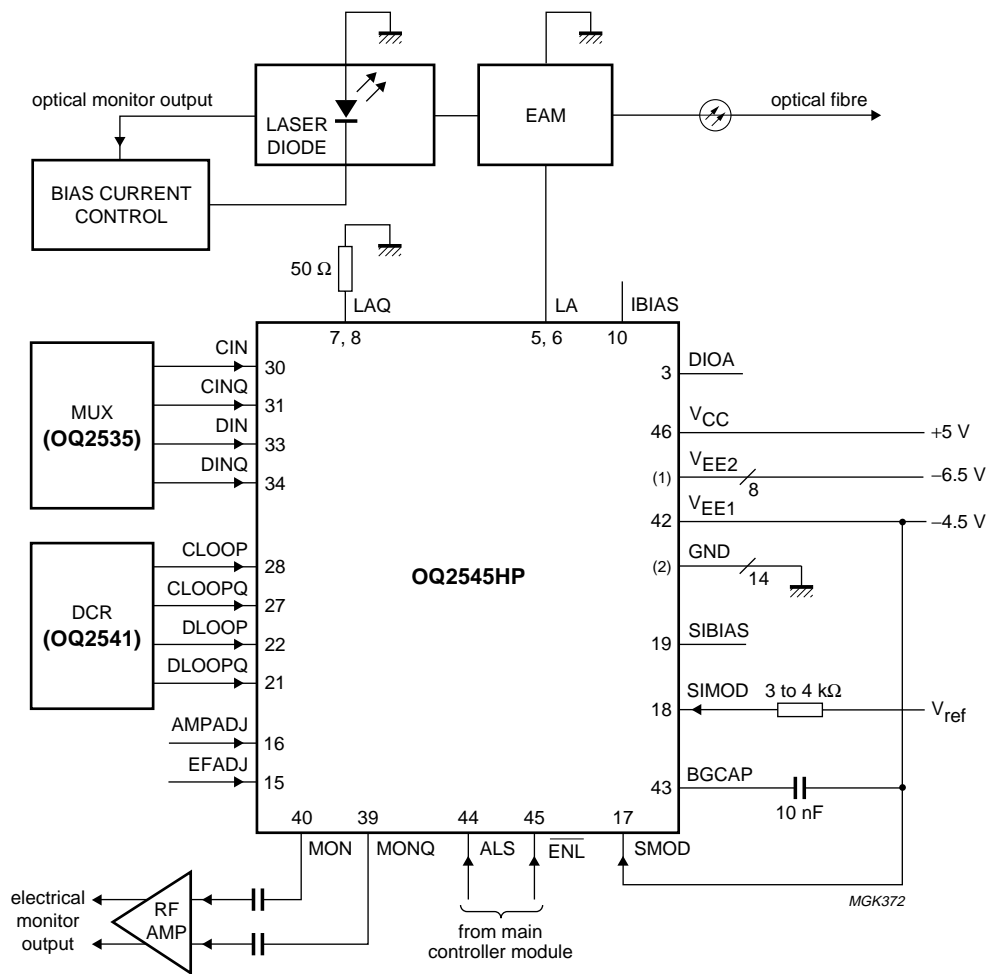


- (1) All V_{EE2} pins (pins 1, 12, 13, 24, 25, 36, 37 and 48) must connected together.
- (2) All GND pins (pins 2, 4, 9, 11, 14, 20, 23, 26, 29, 32, 35, 38, 41 and 47) must be connected directly to the PCB ground plane.

Fig.16 Application schematic OQ2545BHP with laser diode.

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- (1) All VEE2 pins (pins 1, 12, 13, 24, 25, 36, 37 and 48) must be connected together.
- (2) All GND pins (pins 2, 4, 9, 11, 14, 20, 23, 26, 29, 32, 35, 38, 41 and 47) must be connected directly to the PCB ground plane.

Fig.17 Application schematic OQ2545HP with Electro Absorption Modulator (EAM).

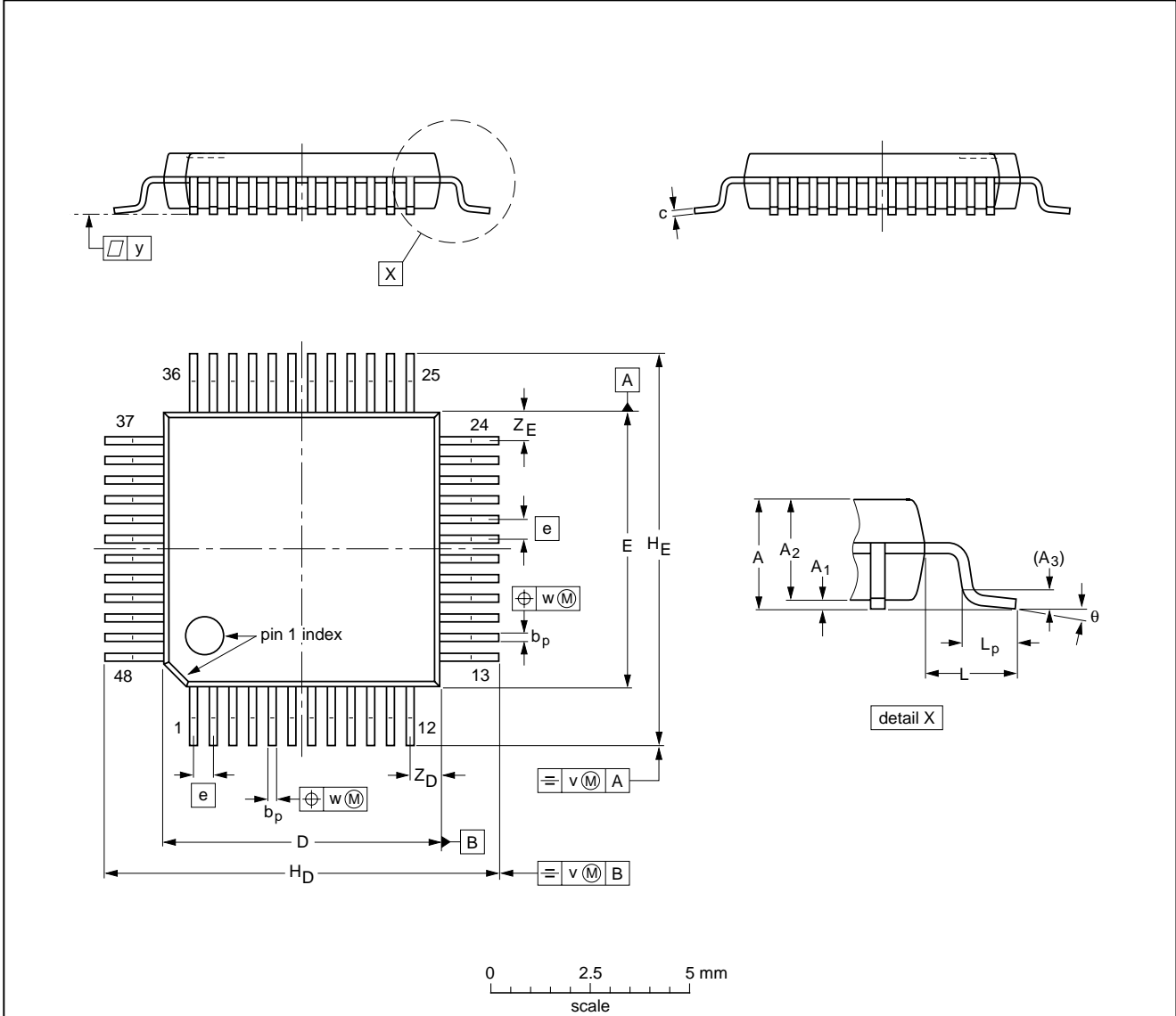
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PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A1	A2	A3	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						94-12-19 97-08-01

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SOLDERING**Introduction to soldering surface mount packages**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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NOTES

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NOTES

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