

QL8x12BL pASIC[®] 1 Family Low Power 3.3 Volt Operation FPGA

pASIC HIGHLIGHTS

*...1,000
usable ASIC gates,
64 I/O pins*

QL8x12BL Block Diagram

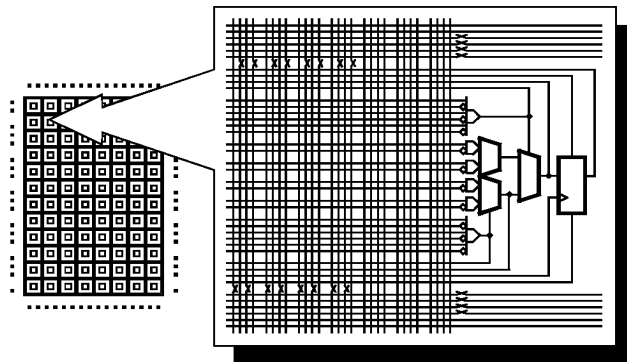
96 Logic Cells



- ✕ **High Speed** – ViaLink[®] metal-to-metal programmable-via antifuse technology, allows counter speeds over 80 MHz at 3.3 Volt operation.
- ✕ **5V Tolerant I/Os** – Support interface to 5 Volt CMOS, NMOS and bipolar devices by sinking up to 12 mA (see IHH specification).
- ✕ **High Usable Density** – An 8-by-12 array of 96 logic cells provides 1,000 usable ASIC gates (2,000 PLD gates) in 44-pin and 68-pin PLCC and 100-pin TQFP packages.
- ✕ **Compatible with Standard 5.0V product** – The "-L" series is fully pin-out and function compatible with the High Speed 5.0V product. See QL8x12B for pin-out and AC Characteristics.
- ✕ **Low-Cost, Easy-to-Use Design Tools** – Designs entered and simulated using QuickLogic's new QuickWorks[®] development environment, or with third-party CAE tools including Viewlogic, Synopsys, Mentor, Cadence and Veribest. Fast, fully automatic place and route on PC and workstation platforms using QuickLogic software.

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pASIC 1



▪ = Up to 56 prog. I/O cells, 6 Input high-drive cells, 2 Input/Clk (high-drive) cells

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage -0.5 to 7.0V
Input Voltage -0.5 to VCC +0.7V
ESD Pad Protection $\pm 2000V$
DC Input Current ± 20 mA
Latch-up Immunity ± 200 mA

Storage Temperature -65°C to + 150°C
Lead Temperature 300°C

OPERATING RANGE

Symbol	Parameter	Commercial		Unit
		Min	Max	
VCC	Supply Voltage	3.0	3.6	V
TA	Ambient Temperature	0	70	°C
TC	Case Temperature			°C
K	Delay Factor	-0 Speed Grade	0.46	2.61
		-1 Speed Grade	0.46	2.23

DC CHARACTERISTICS over operating range

Symbol	Parameter	Conditions	Min	Max	Unit
VIH	Input HIGH Voltage		2.0		V
VIL	Input LOW Voltage			0.8	V
VOH	Output HIGH Voltage	IOH = -2.4 mA	2.4		V
		IOH = -10 mA	VCC-0.1		V
VOL	Output LOW Voltage	IOL = 4 mA		0.4	V
		IOL = 10 μA		0.1	V
IIH	Input HIGH Current Sink (for tolerance to 5V devices)	VCC+0.6V > VI > VCC		12	mA
II	Input Leakage Current	VI = VCC or GND	-10	10	μA
IOZ	3-State Output Leakage Current	VI = VCC or GND	-10	10	μA
CI	Input Capacitance [1]			10	pF
IOS	Output Short Circuit Current [2]	VO = GND	-5	-50	mA
		VO = VCC	15	100	mA
ICC	Supply Current [3]	VI, VIO = VCC or GND		650	μA

Notes:

- [1] Capacitance is sample tested only. CI = 20 pF max on I/(SI) and I/(P).
[2] Only one output at a time. Duration should not exceed 30 seconds.
[3] For AC conditions use the formula described in the Data Book, Section 9 — Power vs Operating Frequency.

ORDERING INFORMATION