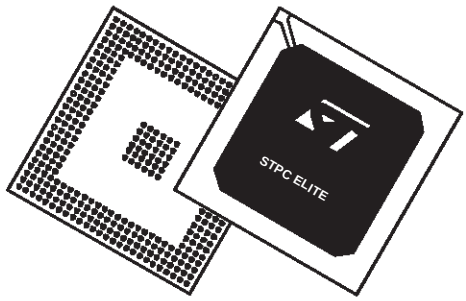
STPC® ELITE

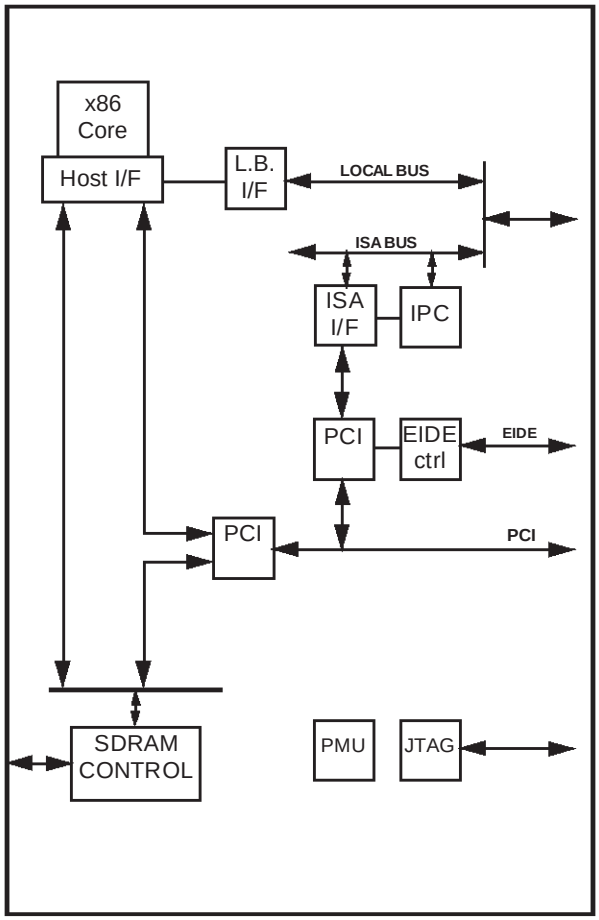
X86 Core General Purpose PC Compatible System - on - Chip

- POWERFUL X86 PROCESSOR
- 64-BIT SDRAM CONTROLLER
- PCI MASTER / SLAVE CONTROLLER
- ISA MASTER/SLAVE
- 16-BIT LOCAL BUS INTERFACE
- EIDE CONTROLLER
- INTEGRATED PERIPHERAL CONTROLLER
  - DMA CONTROLLER
  - INTERRUPT CONTROLLER
  - TIMER / COUNTERS
- POWER MANAGEMENT UNIT
- I C INTERFACE
- 16 GENERAL PURPOSE I/O.
- JTAG IEEE1149.1
- PROGRAMMABLE OUTPUT CLOCK



PBGA388

Logic Diagram



DESCRIPTION

The STPC Elite integrates a fully static x86 processor, fully compatible with standard x86 processors, and combines it with powerful chipset to provide a general purpose PC compatible subsystem on a single device. The device is packaged in a 388 Ball Grid Array (PBGA).

- **X86 Processor core**
- Fully static 32-bit 5-stage pipeline, x86 processor fully PC compatible.
- Can access up to 4GB of external memory.
- 8KByte unified instruction and data cache with write back and write through capability.
- Parallel processing integral floating point unit, with automatic power down.
- Clock core speeds up to of 100 MHz in x1 clock mode and 133MHz in x2 mode.
- Fully static design for dynamic clock control.
- Low power and system management modes.

- **SDRAM Controller**
- 64-bit data bus.
- Up to 100MHz SDRAM clock speed.
- Supports 8MB up to 128 MB system memory.
- Supports 16-, 64- and 128-Mbit memories.
- Supports up to 4 memory banks.
- Supports buffered, non buffered, registered DIMMs
- 4-line write buffers for CPU to DRAM and PCI to DRAM cycles.
- 4-line read prefetch buffers for PCI masters.
- Programmable latency
- Programmable timing for DRAM parameters.
- Supports -8, -10, -12, -13, -15 memory parts
- Supports memory hole between 1MB and 8MB for PCI/ISA busses.

- **PCI Controller**
- Compliant with PCI 2.1 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. External logic allows for greater than 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- 0.25X, 0.33X and 0.5X Host clock PCI clock.

- **ISA master/slave**
- Generates the ISA clock from either 14.318MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus. NSP compliant.
- 16-bit I/O decoding.

- **Local Bus interface**
- Multiplexed with ISA/DMA/Timer functions.
- High speed, low latency bus.
- Supports 32-bit Flash burst.
- 16-bit data bus with word steering capability.
- Separate memory and I/O address spaces.
- Programmable timing (Host clock granularity)
- Supports 2 cashable banks of 16MB flash devices with boot block shadowed to 0x000F0000.
- 2 Programmable Flash/EPROM Chip Select.
- 4 Programmable I/O Chip Select.
- 2-level hardware key protection for Flash boot block protection.
- 22 bit address bus.

- **EIDE Controller**
- Compatible with EIDE (ATA-2).
- Backward compatibility with IDE (ATA-1).
- Supports up to 4 IDE devices
- Supports PIO and Bus Master IDE
- Concurrent channel operation (PIO & DMA modes) - 4 x 32-Bit Buffer FIFO per channel
- Support for 11.1/16.6 MB/s, I/O Channel Ready PIO data transfers.
- Bus Master with scatter/gather capability.
- Multi-word DMA support for fast IDE drives.
- Individual drive timing for all four IDE devices.
- Supports both legacy & native IDE modes.
- Supports hard drives larger than 528MB.
- Support for CD-ROM and tape peripherals.

- **Integrated Peripheral Controller**
- 2X8237/AT compatible 7-channel DMA controller.
- 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Co-processor error support logic.
- Supports external RTC.

- **Power Management**
- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports SMM.
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel ports.
- Supports RTC, interrupts and DMAs wake-up

- **GPIOs**
- 16 General Purpose IO.

- **JTAG Function**

- **Programmable GP-Clock**
- This clock is programmable to frequencies up to 135 MHz.

1 GENERAL DESCRIPTION

At the heart of the STPC Elite is an advanced processor block that includes a powerful x86 processor core along with a 64-bit SDRAM controller, a high speed PCI local-bus controller and Industry standard PC chip set functions (Interrupt controller, DMA Controller, Interval timer and ISA bus) and EIDE controller.

The processor bus runs at the speed of the processor (x1 mode) or half the speed (x2 mode).

The STMicroelectronics x86 processor core is embedded with standard and application specific peripheral modules on the same silicon die. The core has all the functionality of the ST standard x86 processor products, including the low power System Management Mode (SMM).

System Management Mode (SMM) provides an additional interrupt and address space that can be used for system power management or software transparent emulation of peripherals. While running in isolated SMM address space, the SMM interrupt routine can execute without interfering with the operating system or application programs.

Further power management facilities include a suspend mode that can be initiated from either hardware or software. Because of the static nature of the core, no internal data is lost.

The 'standard' PC chipset functions (DMA, interrupt controller, timers, power management logic) are integrated with the x86 processor core.

The PCI bus is the main data communication link to the STPC Elite chip. The STPC Elite translates appropriate host bus I/O and Memory cycles onto the PCI bus. It also supports generation of Configuration cycles on the PCI bus. The STPC Elite, as a PCI bus agent (host bridge class), fully complies with PCI specification 2.1. The chip-set also implements the PCI mandatory header registers in Type 0 PCI configuration space for easy porting of PCI aware system BIOS. The device contains a PCI arbitration function for three external PCI devices.

The STPC Elite integrates an ISA bus controller. Peripheral modules such as parallel and serial communications ports, keyboard controllers and additional ISA devices can be accessed by the STPC Elite chip set through this bus.

An industry standard EIDE (ATA 2) controller is built in to the STPC Elite and connected internally via the PCI bus.

The STPC Elite core is compliant with the Advanced Power Management (APM) specification to provide a standard method by which the BIOS can control the power used by personal computers. The Power Management Unit module (PMU) controls the power consumption providing a comprehensive set of features that control the power usage and supports compliance with the United States Environmental Protection Agency's Energy Star Computer Program. The PMU provides following hardware structures to assist the software in managing the power consumption by the system.

- System Activity Detection.

- 3 power-down timers detecting system inactivity:
  - Doze timer (short durations).
  - Stand-by timer (medium durations).
  - Suspend timer (long durations).

- House-keeping activity detection.

- House-keeping timer to cope with short bursts of house-keeping activity while dozing or in stand-by state.

- Peripheral activity detection.

- Peripheral timer detecting peripheral inactivity

- SUSP# modulation to adjust the system performance in various power down states of the system including full power on state.

- Power control outputs to disable power from different planes of the board.

Lack of system activity for progressively longer period of times is detected by the three power down timers. These timers can generate SMI interrupts to CPU so that the SMM software can put the system in decreasing states of power consumption. Alternatively, system activity in a power down state can generate SMI interrupt to allow the software to bring the system back up to full power on state. The chip-set supports up to three power down states: Doze state, Stand-by state and Suspend mode. These correspond to decreasing levels of power savings.

Power down puts the STPC Elite into suspend mode. The processor completes execution of the current instruction, any pending decoded instructions and associated bus cycles. During the suspend mode, internal clocks are stopped. removing power down, the processor resumes instruction fetching and begins execution in the instruction stream at the point it had stopped.

MEMORY CONTROLLER

The STPC handles the memory data (DATA) bus directly, controlling from 2 to 128 MBytes. The SDRAM controller supports accesses to the Memory Banks to/from the CPU (via the host) from the VMI, to/from the CRTC, to the VIDEO & to/from the GE. (Banks 0 to 3) which can be populated with either single or double sided 72-bit (4 bit parity) DIMMs. Parity is not supported.

The SDRAM controller only supports 64 bit wide Memory Banks.

Four Memory Banks (if DIMMS are used; Single sided or two double-sided DIMMs) are supported in the following configurations (seeTable 1-1)

Table 1-1. Memory configurations

Memory Bank size	Number	Organisation	Device Size
1Mx64	4	1Mx16	16Mbits
2Mx64	8	2Mx8	
4Mx64	16	4Mx4	
4Mx64	4	2Mx16x2	64Mbits
8Mx64	8	4Mx8x2	
16Mx64	16	8Mx4x2	
4Mx64	4	1Mx16x4	
8Mx64	8	2Mx8x4	
32Mx64	16	4Mx4x4	
16Mx64	8	2Mx16x2	128Mbits
32Mx64	16	4Mx8x4	

Figure 1-1. Functional description.

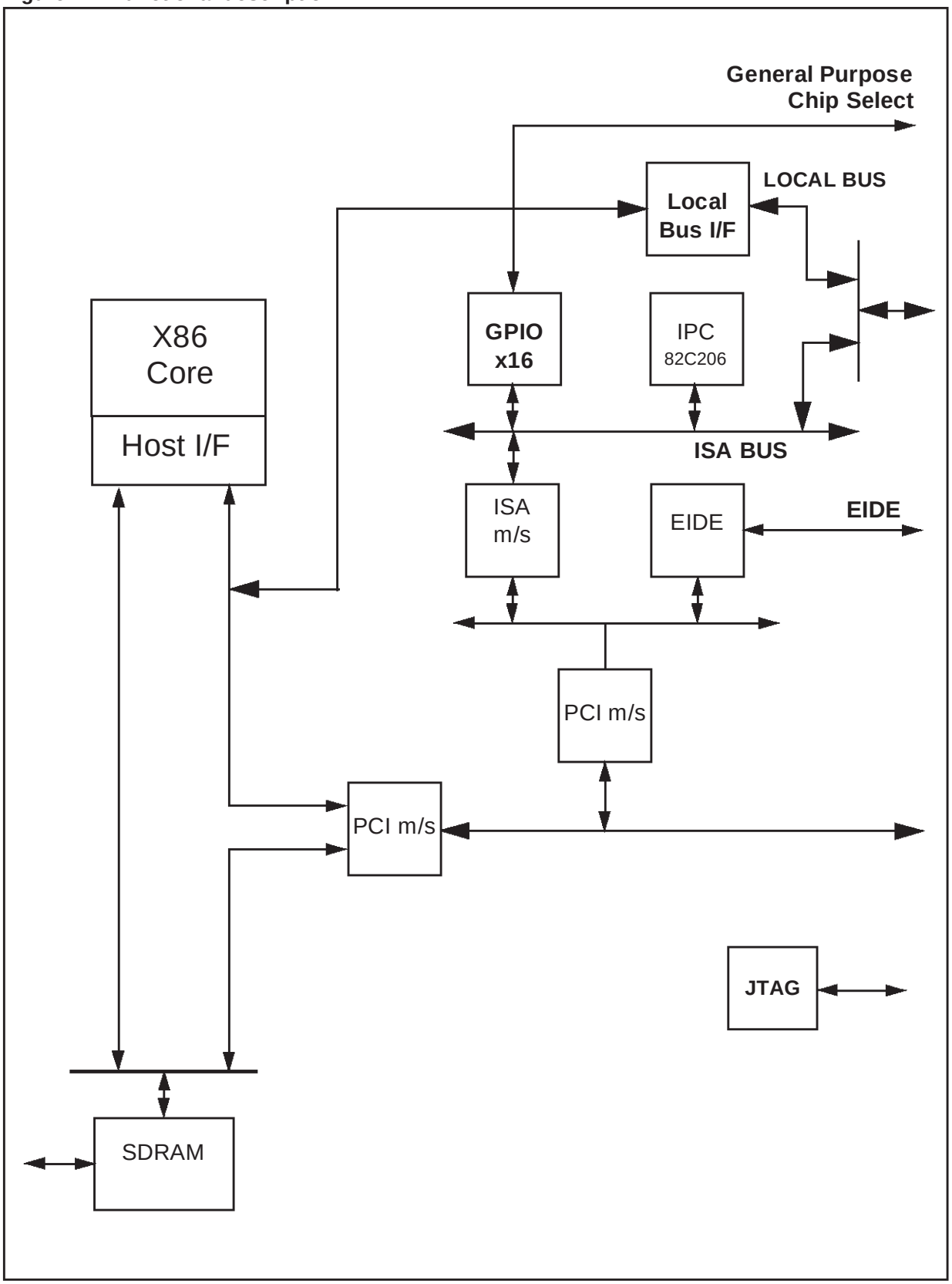
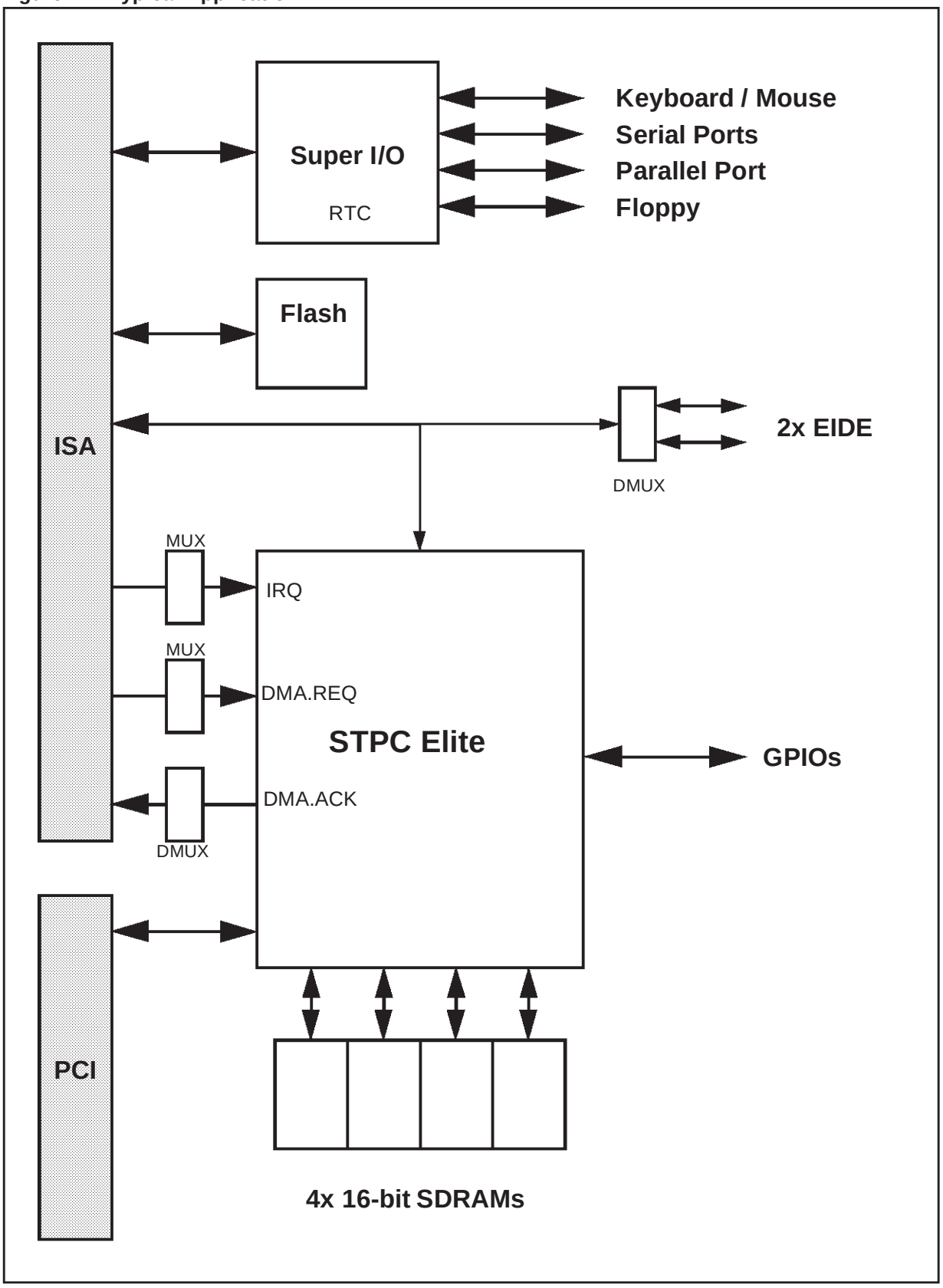


Figure 1-2. Typical Application



2 PIN DESCRIPTION

2.1 INTRODUCTION

The STPC Elite integrates most of the functionalities of the PC architecture. As a result, many of the traditional interconnections between the host PC microprocessor and the peripheral devices are totally internal to the STPC Elite. This offers improved performance due to the tight coupling of the processor core and these peripherals. As a result many of the external pin connections are made directly to the on-chip peripheral functions.

Figure 2-1 shows the STPC Elite external interfaces. It defines the main busses and their function. Table 2-1 describes the physical implementation listing signals type and their functionality. Table 2-2 provides a full pin listing and description of pins. Table 2-5 provides a full listing of pin locations of the STPC Elite package by physical connection.

Table 2-1. Signal Description

Group name	Qty	
Basic Clocks reset & Xtal		6
Memory Interface		96
PCI interface		56
ISA	79	90
IDE	34	
Local Bus	50	
Grounds		69
V_{DD}		24
Miscellaneous		8
GPIO		16
Unconnected		23
Total Pin Count		388

Note: Several interface pins are multiplexed with other functions, refer to Table 2-3 and Table 2-4 for further details

Figure 2-1. STPC Elite External Interfaces

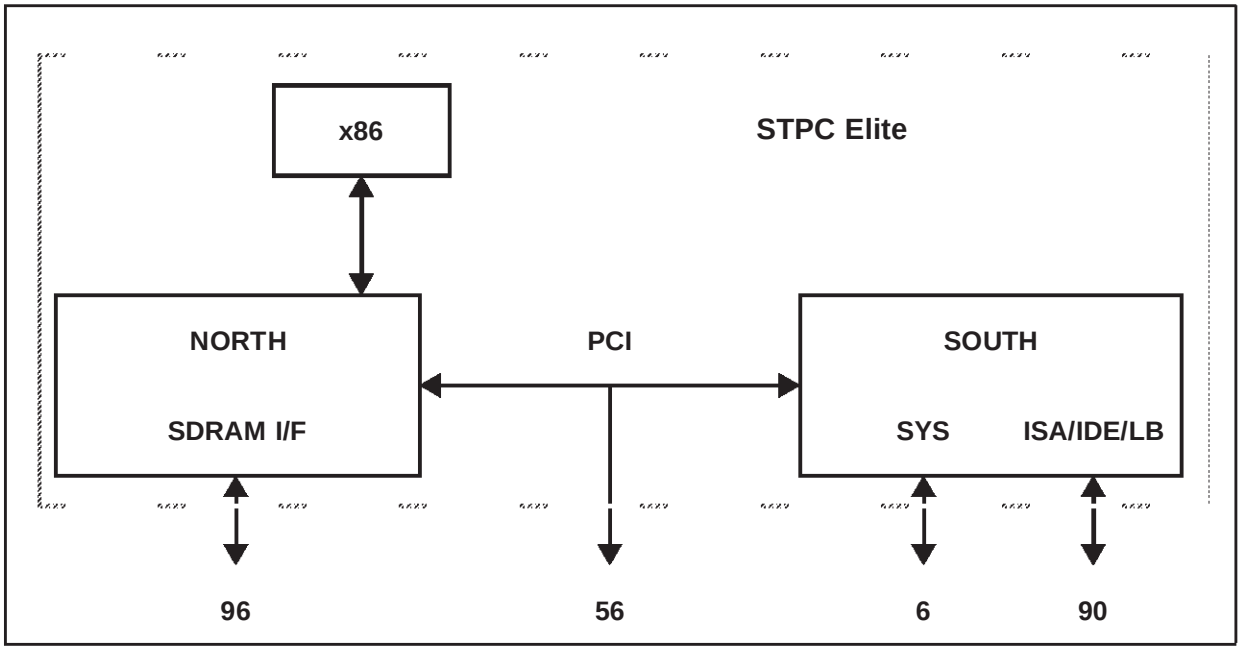


Table 2-2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
BASIC CLOCKS AND RESETS			
SYSRSETI#[2]	I	System Power Good Input	1
SYSRSTO#[2]	O	System Reset Output	1
XTALI	I	14.3MHz Crystal Input	1
XTALO	I/O	14.3MHz Crystal Output - External Oscillator Input	1
HCLK	I/O	Host Clock (Test)	1
GP_CLK	O	General Purpose Clock	1
V_{DD}_xxx_PLL[1]		Power Supply for PLL Clocks	
MEMORY INTERFACE			
MCLKI	I	Memory Clock Input	1
MCLKO	O	Memory Clock Output	1
CS#[1:0]	O	DIMM Chip Select	2
CS#[3]/MA[12]/BA[1]	O	DIMM Chip Select/ Memory Address/ Bank Address	1
CS#[2]/MA[11]	O	DIMM Chip Select/ Bank Address	1
BA[0]	O	Bank Address	
MA[10:0]	O	Memory Row & Column Address	12
MD[63:0][3]	I/O	Memory Data	64
RAS#[1:0]	O	Row Address Strobe	2
CAS#[1:0]	O	Column Address Strobe	2
MWE#	O	Write Enable	1
DQM[7:0]	O	Data Input/Output Mask	8
PCI INTERFACE			
PCI_CLKI	I	33MHz PCI Input Clock	1
PCI_CLKO	O	33MHz PCI Output Clock (from internal PLL)	1
AD[31:0][2]	I/O	PCI Address / Data	32
CBE[3:0][2]	I/O	Bus Commands / Byte Enables	4
FRAME#[2]	I/O	Cycle Frame	1
IRDY#[2]	I/O	Initiator Ready	1
TRDY#[2]	I/O	Target Ready	1
LOCK#[2]	I	PCI Lock	1
DEVSEL#[2]	I/O	Device Select	1
STOP#[2]	I/O	Stop Transaction	1
PAR[2]	I/O	Parity Signal Transactions	1
SERR#[2]	O	System Error	1
PCI_REQ#[2:0][2]	I	PCI Request	3
PCI_GNT#[2:0][2]	O	PCI Grant	3
PCI_INT[3:0][2]	I	PCI Interrupt Request	4
ISA CONTROL			
ISA_CLK	O	ISA Clock Output - Multiplexer Select Line For IPC	1
ISA_CLK2X	O	ISA Clock x2 Output - Multiplexer Select Line For IPC	1
OSC14M[2]	O	ISA bus synchronisation clock	1

Note[1]; These pins must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply.

Note[2]; Denotes that the pin is V_{5T} (see Section 4)

Note [3]; see Table 2-5 for V_{5T} signals

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
LA[23:17][2]	O	Unlatched Address	7
SA[19:0][2]	I/O	Latched Address	20
SD[15:0][2]	I/O	Data Bus	16
ALE[2]	O	Address Latch Enable	1
MEMR#[2], MEMW#[2]	I/O	Memory Read and Memory Write	2
SMEMR#[2], SMEMW#[2]	O	System Memory Read and Memory Write	2
IOR#[2], IOW#[2]	I/O	I/O Read and Write	2
MCS16#[2], IOCS16#[2]	I	Memory/IO Chip Select16	2
BHE#[2]	O	System Bus High Enable	1
ZWS#[2]	I	Zero Wait State	1
REF#[2]	O	Refresh Cycle.	1
MASTER#[2]	I	Add On Card Owns Bus	1
AEN[2]	O	Address Enable	1
IOCHCK#[2]	I	I/O Channel Check.	1
IOCHRDY[2]	I/O	I/O Channel Ready (ISA) - Busy/Ready (IDE)	1
ISAOE#[2]	O	ISA/IDE Selection	1
GPIOCS#[2]	I/O	General Purpose Chip Select	1
IRQ_MUX[3:0][2]	I	Time-Multiplexed Interrupt Request	4
DREQ_MUX[1:0][2]	I	Time-Multiplexed DMA Request	2
DACK_ENC[2:0][2]	O	Encoded DMA Acknowledge	3
TC[2]	O	ISA Terminal Count	1
RTCAS[2]	O	Real Time Clock Address Strobe	1
RMRTCCS#[2]	I/O	ROM/RTC Chip Select	1
KBCS#[2]	I/O	Keyboard Chip Select	1
RTCRW#[2]	I/O	RTC Read/Write	1
RTCDS[2]	I/O	RTC Data Strobe	1
LOCAL BUS			
PA[23:0][2]	O	Address Bus	24
PD[15:0]	I/O	Data Bus	16
PRD1#,PRD0#	O	Peripheral Read Control	2
PWR1#,PWR0#	O	Peripheral Write Control	2
PRDY#	I	Data Ready	1
FCS1#, FCS0#	O	Flash Chip Select	2
IOCS#[3:0]	O	I/O Chip Select	4
IDE CONTROL			
DA[2:0]	O	Address Bus	3
DD[15:0]	I/O	Data Bus	16
PCS3#,PCS1#,SCS3#,SCS1#	O	Primary & Secondary Chip Selects	4
DIORDY	O	Data I/O Ready	1
PIRQ[2], SIRQ[2]	I	Primary & Secondary Interrupt Request	2
PDRQ[2], SDRQ[2]	I	Primary & Secondary DMA Request	2
PDACK#[2], SDACK#[2]	O	Primary & Secondary DMA Acknowledge	2
PDIOR#[2], SDIOR#[2]	O	Primary & Secondary I/O Channel Read	2

Note[1]; These pins must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply.

Note[2]; Denotes that the pin is V_{5T} (see Section 4)

Note [3]; see Table 2-5 for V_{5T} signals

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
PDIOW#[2], SDIOW#[2]	O	Primary & Secondary I/O Channel Write	2
MISCELLANEOUS			
GPIO[15:0][2]	I/O	General Purpose I/Os	16
SPKRD[2]	O	Speaker Device Output	1
SCL[2]	I/O	I C Interface - Clock / Can be used for VGA DDC[1] signal	1
SDA[2]	I/O	I C Interface - Data / Can be used for VGA DDC[0] signal	1
SCAN_ENABLE[2]	I	Reserved (Test pin)	1
TCLK[2]	I	Test clock	1
TDI[2]	I	Test data input	1
TMS[2]	I	Test mode input	1
TDO[2]	O	Test data output	1
Note[1]; These pins must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply.			
Note[2]; Denotes that the pin is V_{5T} (see Section 4)			
Note [3]; see Table 2-5 for V_{5T} signals			

2.2 SIGNAL DESCRIPTIONS

2.2.1 BASIC CLOCKS AND RESETS

SYSRSTI# *System Reset/Power good.* This input is low when the reset switch is depressed. Otherwise, it reflects the power supply's power good signal. This input is asynchronous to all clocks, and acts as a negative active reset. The reset circuit initiates a hard reset on the rising edge of this signal.

SYSRSTO# *Reset Output to System.* This is the system reset signal and is used to reset the rest of the components (not on Host bus) in the system. The ISA bus reset is an externally inverted buffered version of this output and the PCI bus reset is an externally buffered version of this output.

XTALI *14.3MHz Crystal Input*
XTALO *14.3MHz Crystal Output.* These pins are connected to the 14.318 MHz crystal to provide the reference clock for the internal frequency synthesizer to generate all the other clocks.
A 14.318 MHz Series Cut Quartz Crystal should be connected between these two pins. Balance capacitors of 15 pF should also be added. In the event of an external oscillator providing the master clock signal to the STPC Elite device, the TTL signal should be provided on XTALO.

HCLK *Host Clock.* This clock supplies the CPU and the host related blocks. This clock can e doubled inside the CPU and is intended to operate in the range of 25 to 100 MHz. This clock in generated internally from a PLL but can be driven directly from the external system.

GP_CLK *General Purpose clock.* This clock is programmable and its frequency can be as high as 135 MHz.

2.2.2 MEMORY INTERFACE

MCLKI *Memory Clock Input.* This clock is driving the SDRAM controller, the graphics engine and display controller. This input should be a buffered version of the MCLKO signal with the track lengths between the buffer and the pin matched with the track lengths between the buffer and the DIMMs.

MCLKO *Memory Clock Output.* This clock is driving the DIMMs on board and is generated from an internal PLL. The default value is 66MHz.

CS#[2]/MA[11] *Chip Select/ Bank Address* This pin is CS#[2] in the case when 16Mbit devices are used. For all other densities, it becomes MA[11].

CS#[3]/MA[12]/BA[1] *Chip Select/ Memory Address/ Bank Address* This pin is CS#[3] in the case when 16Mbit devices are used. For all other densities, it becomes MA[12] when 2 internal banks devices are used and BA[1] when 4 internal bank devices are used.

MA[10:0] *Memory Address.* Multiplexed row and column address lines.

BA[0] *Memory Bank Address.*

CS#[1:0] *Chip Select* These signals are used to disable or enable device operation by masking or enabling all SDRAM inputs except MCLK, CKE, and DQM.

MD[63:0] *Memory Data.* This is the 64-bit memory data bus. MD[40-0] are read by the device strap option registers during rising edge of SYSRSTI#.

RAS#[1:0] *Row Address Strobe.* These signals enable row access and precharge. Row address is latched on rising edge of MCLK when RAS# is low.

CAS#[1:0] *Column Address Strobe.* These signals enable column access. Column address is latched on rising edge of MCLK when CAS# is low.

MWE# *Write Enable.* Write enable specifies whether the memory access is a read (MWE# = H) or a write (MWE# = L).

DQM#[7:0] *Data Mask.* Makes data output Hi-Z after the clock and masks the SDRAM outputs. Blocks SDRAM data input when DQM active.

2.2.3 PCI INTERFACE

PCI_CLKI *33MHz PCI Input Clock.* This signal is the PCI bus clock input and should be driven from the PCI_CLKO pin.

PCI_CLKO *33MHz PCI Output Clock.* This is the master PCI bus clock output.

AD[31:0] *PCI Address/Data.* This is the 32-bit multiplexed address and data bus of the PCI. This bus is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions.

CBE#[3:0] *Bus Commands/Byte Enables.* These are the multiplexed command and byte enable signals of the PCI bus. During the address phase they define the command and during the data

phase they carry the byte enable information. These pins are inputs when a PCI master other than the STPC Elite owns the bus and outputs when the STPC Elite owns the bus.

FRAME# *Cycle Frame.* This is the frame signal of the PCI bus. It is an input when a PCI master owns the bus and is an output when STPC Elite owns the PCI bus.

IRDY# *Initiator Ready.* This is the initiator ready signal of the PCI bus. It is used as an output when the STPC Elite initiates a bus cycle on the PCI bus. It is used as an input during the PCI cycles targeted to the STPC Elite to determine when the current PCI master is ready to complete the current transaction.

TRDY# *Target Ready.* This is the target ready signal of the PCI bus. It is driven as an output when the STPC Elite is the target of the current bus transaction. It is used as an input when STPC Elite initiates a cycle on the PCI bus.

LOCK# *PCI Lock.* This is the lock signal of the PCI bus and is used to implement the exclusive bus operations when acting as a PCI target agent.

DEVSEL# *I/O Device Select.* This signal is used as an input when the STPC Elite initiates a bus cycle on the PCI bus to determine if a PCI slave device has decoded itself to be the target of the current transaction. It is asserted as an output either when the STPC Elite is the target of the current PCI transaction or when no other device asserts DEVSEL# prior to the subtractive decode phase of the current PCI transaction.

STOP# *Stop Transaction.* Stop is used to implement the disconnect, retry and abort protocol of the PCI bus. It is used as an input for the bus cycles initiated by the STPC Elite and is used as an output when a PCI master cycle is targeted to the STPC Elite.

PAR *Parity Signal Transactions.* This is the parity signal of the PCI bus. This signal is used to guarantee even parity across AD[31:0], CBE#[3:0], and PAR. This signal is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions. (Its assertion is identical to that of the AD bus delayed by one PCI clock cycle)

SERR# *System Error.* This is the system error signal of the PCI bus. It may, if enabled, be asserted for one PCI clock cycle if target aborts a STPC Elite initiated PCI transaction. Its assertion by either the STPC Elite or by another PCI bus agent will trigger the assertion of NMI to the host CPU. This is an open drain output.

PCI_REQ#[2:0] *PCI Request.* This pin are the three external PCI master request pins. They indicates to the PCI arbiter that the external agents desire use of the bus.

PCI_GNT#[2:0] *PCI Grant.* These pins indicate that the PCI bus has been granted to the master requesting it on its PCIREQ#.

PCI_INT[3:0] *PCI Interrupt Request.* These are the PCI bus interrupt signals.

VDD5 *5V Power Supply.* These power pins are necessary for 5V ESD protection. In case the PCI bus is used in 3.3V only, these pins can be connected to 3.3V.

2.2.4 ISA INTERFACE

ISA_CLK, ISA_CLKX2 *ISA Clock x1, x2.* These pins generate the Clock signal for the ISA bus and a Doubled Clock signal. They are also used as the multiplexor control lines for the Interrupt Controller Interrupt input lines. ISA_CLK is generated from either PCICLK/4 or OSC14M/ 2.

OSC14M *ISA bus synchronisation clock Output.* This is the buffered 14.318 Mhz clock for the ISA bus.

LA[23:17] *Unlatched Address.* When the ISA bus is active, these pins are ISA Bus unlatched address for 16-bit devices. When ISA bus is accessed by any cycle initiated from PCI bus, these pins are in output mode. When an ISA bus master owns the bus, these pins are in input mode.

SA[19:0] *ISA Address Bus.* System address bus of ISA on 8-bit slot. These pins are used as an input when an ISA bus master owns the bus and are outputs at all other times.

SD[15:0] *I/O Data Bus.* These pins are the external databus to the ISA bus.

ALE *Address Latch Enable.* This is the address latch enable output of the ISA bus and is asserted by the STPC Elite to indicate that LA23-17, SA19-0, AEN and SBHE# signals are valid. The ALE is driven high during refresh, DMA master or an ISA master cycles by the STPC Elite. ALE is driven low after reset.

MEMR# *Memory Read.* This is the memory read command signal of the ISA bus. It is used as an in-

put when an ISA master owns the bus and is an output at all other times.
The MEMR# signal is active during refresh.

MEMW# *Memory Write.* This is the memory write command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.

SMEMR# *System Memory Read.* The STPC Elite generates SMEMR# signal of the ISA bus only when the address is below one megabyte or the cycle is a refresh cycle.

SMEMW# *System Memory Write.* The STPC Elite generates SMEMW# signal of the ISA bus only when the address is below one megabyte.

IOR# *I/O Read.* This is the IO read command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

IOW# *I/O Write.* This is the IO write command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

MCS16# *Memory Chip Select16.* This is the decode of LA23-17 address pins of the ISA address bus without any qualification of the command signal lines. MCS16# is always an input. The STPC Elite ignores this signal during IO and refresh cycles.

IOCS16# *IO Chip Select16.* This signal is the decode of SA15-0 address pins of the ISA address bus without any qualification of the command signals. The STPC Elite does not drive IOCS16# (similar to PC-AT design). An ISA master access to an internal register of the STPC Elite is executed as an extended 8-bit IO cycle.

BHE# *System Bus High Enable.* This signal, when asserted, indicates that a data byte is being transferred on SD15-8 lines. It is used as an input when an ISA master owns the bus and is an output at all other times.

ZWS# *Zero Wait State.* This signal, when asserted by addressed device, indicates that current cycle can be shortened.

REF# *Refresh Cycle.* This is the refresh command signal of the ISA bus. It is driven as an output when the STPC Elite performs a refresh cycle on the ISA bus. It is used as an input when an ISA master owns the bus and is used to trigger a refresh cycle.
The STPC Elite performs a pseudo hidden refresh. It requests the host bus for two host clocks to drive the refresh address and capture it in external buffers. The host bus is then relinquished while the refresh cycle continues on the ISA bus.

MASTER# *Add On Card Owns Bus.* This signal is active when an ISA device has been granted bus ownership.

AEN *Address Enable.* Address Enable is enabled when the DMA controller is the bus owner to indicate that a DMA transfer will occur. The enabling of the signal indicates to IO devices to ignore the IOR#/IOW# signal during DMA transfers.

IOCHCK# *IO Channel Check.* IO Channel Check is enabled by any ISA device to signal an error condition that can not be corrected. NMI signal becomes active upon seeing IOCHCK# active if the corresponding bit in Port B is enabled.

IOCHRDY *Channel Ready.* IOCHRDY is the IO channel ready signal of the ISA bus and is driven as an output in response to an ISA master cycle targeted to the host bus or an internal register of the STPC Elite. The STPC Elite monitors this signal as an input when performing an ISA cycle on behalf of the host CPU, DMA master or refresh.
ISA masters which do not monitor IOCHRDY are not guaranteed to work with the STPC Elite since the access to the system memory can be considerably delayed due UMA architecture.

ISAOE# *Bidirectional OE Control.* This signal controls the $\overline{OE}$ signal of the external transceiver that connects the IDE DD bus and ISA SA bus.

GPIOCS# *I/O General Purpose Chip Select.* This output signal is used by the external latch on ISA bus to latch the data on the SD[7:0] bus. The latch can be use by PMU unit to control the external peripheral devices or any other desired function.

IRQ_MUX[3:0] *Multiplexed Interrupt Request.* These are the ISA bus interrupt signals. They have to be encoded before connection to the STPC Elite using ISACLK and ISACLKX2 as the input selection strobes.
Note that IRQ8B, which by convention is connected to the RTC, is inverted before being sent to the interrupt controller, so that it may be connected directly to the $\overline{IRQ}$ pin of the RTC.

DREQ_MUX[1:0] *ISA Bus Multiplexed DMA Request.* These are the ISA bus DMA request signals. They are to be encoded before connection to the STPC Elite using ISACLK and ISACLKX2 as the input selection strobes.

DACK_ENC[2:0] *DMA Acknowledge.* These are the ISA bus DMA acknowledge signals. They are encoded by the STPC Elite before output and should be decoded externally using ISACLK and ISACLKX2 as the control strobes.

TC *ISA Terminal Count.* This is the terminal count output of the DMA controller and is connected to the TC line of the ISA bus. It is asserted during the last DMA transfer, when the byte count expires.

2.2.5 X-Bus Interface pins

RTCAS# *Real time clock address strobe.* This signal is asserted for any I/O write to port 70H.

RMRTCCS# *ROM/Real Time clock chip select.* This signal is asserted if a ROM access is decoded during a memory cycle. It should be combined with MEMR# or MEMW# signals to properly access the ROM. During a IO cycle, this signal is asserted if access to the Real Time Clock (RTC) is decoded. It should be combined with IOR or IOW# signals to properly access the real time clock.

KBCS# *Keyboard Chip Select.* This signal is asserted if a keyboard access is decoded during a I/O cycle.

RTCRW# *Real Time Clock* $\overline{RW}$. This pin is a multifunction pin. When ISAOE# is active, this signal is used as RTCRW#. This signal is asserted for any I/O write to port 71H.

RTCDS# *Real Time Clock DS.* This pin is a multifunction pin. When ISAOE# is active, this signal is used as RTCDS. This signal is asserted for any I/O read to port 71H.

Note: RMRTCCS#, KBCS#, RTCRW# and RTCDS# signals must be ORed externally with ISAOE# and then connected to the external device. An LS244 or equivalent function can be used if OE# is connected to ISAOE# and the output is provided with a weak pull-up resistor as shown in Figure 2-2.

2.2.6 LOCAL BUS

PA[23:0] *Address Bus Output.*

PD[15:0] *Data Bus.* This is the 16-bit data bus. D[7:0] is the LSB and PD[15:8] is the MSB.

PRD#[1:0] *Read Control output.* PRD0# is used to read the LSB and PRD1# to read the MSB.

PWR#[1:0] *Write Control output.* PWR0# is used to write the LSB and PWR1# to write the MSB.

PRDY# *Data Ready input.* This signal is used to create wait states on the bus. When low, it completes the current cycle.

FCS#[1:0] *Flash Chip Select output.* These are the Programmable Chip Select signals for up to 2 banks of Flash memory.

IOCS#[3:0] *I/O Chip Select output.* These are the Programmable Chip Select signals for up to 4 external I/O devices.

2.2.7 IDE INTERFACE

DA[2:0] *Address.* These signals are connected to DA[2:0] of IDE devices directly or through a buffer. If the toggling of signals are to be masked during ISA bus cycles, they can be externally ORed with ISAOE# before being connected to the IDE devices.

DD[15:0] *Databus.* When the IDE bus is active, they serve as IDE signals DD[11:0]. IDE devices are connected to SA[19:8] directly and ISA bus is connected to these pins through two LS245 transceivers as described in Figure 2-2.

PCS1#, PCS3# *Primary Chip Select.* These signals are used as the active high primary master & slave IDE chip select signals. These signals must be externally ANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

SCS1#, SCS3# *Secondary Chip Select.* These signals are used as the active high secondary master & slave IDE chip select signals. These signals must be externally ANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

DIORDY *Busy/Ready.* This pin serves as IDE signal DIORDY.

PIRQ *Primary Interrupt Request.*
SIRQ *Secondary Interrupt Request.*
Interrupt request from IDE channels.

PDRQ *Primary DMA Request.*
SDRQ *Secondary DMA Request.*
DMA request from IDE channels.

PDACK# *Primary DMA Acknowledge.*
SDACK# *Secondary DMA Acknowledge.*
DMA acknoledge to IDE channels.

PDIOR#, PDIOW# *Primary I/O Read & Write.*
SDIOR#, SDIOW# *Secondary I/O Read & Write*
Primary & Secondary channel read & write.

2.2.8 MISCELLANEOUS

GPIO[15:0] *General Purpose I/Os*

SPKRD *Speaker Drive.* This the output to the speaker and is AND of the counter 2 output with bit 1 of Port 61, and drives an external speaker driver. This output should be connected to 7407 type high voltage driver.

SCL, SDA I C Interface. These bidirectional pins are connected to CRTC register 3Fh to implement DDC capabilities. They conform to I²C electrical specifications, they have open-collector output drivers which are internally connected to V_{DD} through pull-up resistors.
They can be used for the DDC1 (SCL) and DDC0 (SDA) lines of the VGA interface.

SCAN_ENABLE *Reserved*. The pin is reserved for Test and Miscellaneous functions.

VDD_CORE *2.5V Core Power Supply.* These power pins are necessary to supply the core with 2.5V.

TCLK *Test clock*

TDI *Test data input*

TMS *Test mode input*

TDO *Test data output*

.

Table 2-3. ISA / IDE dynamic multiplexing

ISA BUS (ISAOE# = 0)	IDE (ISAOE# = 1)
RMRTCCS#	DD[15]
KBCS#	DD[14]
RTCRW#	DD[13]
RTCDS	DD[12]
SA[19:8]	DD[11:0]
LA[23]	SCS3#
LA[22]	SCS1#
SA[21]	PCS3#
SA[20]	PCS1#
LA[19:17]	DA[2:0]
IOCHRDY	DIORDY

.

Table 2-4. ISA / Local Bus pin sharing

ISA / IPC	LOCAL BUS
SD[15:0]	PD[15:0]
DREQ_MUX[1:0]	PA[21:20]
SMEMR#	PA[19]
MEMW#	PA[18]
BHE#	PA[17]
AEN	PA[16]
ALE	PA[15]
MEMR#	PA[14]
IOR#	PA[13]
IOW#	PA[12]
REF#	PA[11]
IOCHCK#	PA[10]
GPIOCS#	PA[9]
ZWS#	PA[8]
SA[7:4]	PA[7:4]
TC, DACK_ENC[2:0]	PA[3:0]
SA[3]	PRDY#
ISAOE#,SA[2:0]	IOCS#[3:0]
DEV_CLK, RTCAS#	FCS#[1:0]
IOCS16#, MASTER#	PRD#[1:0]
SMEMW#, MCS16#	PWR#[1:0]
ISACLK, ISA_CLK2X	

Figure 2-2. Typical ISA/IDE Demultiplexing

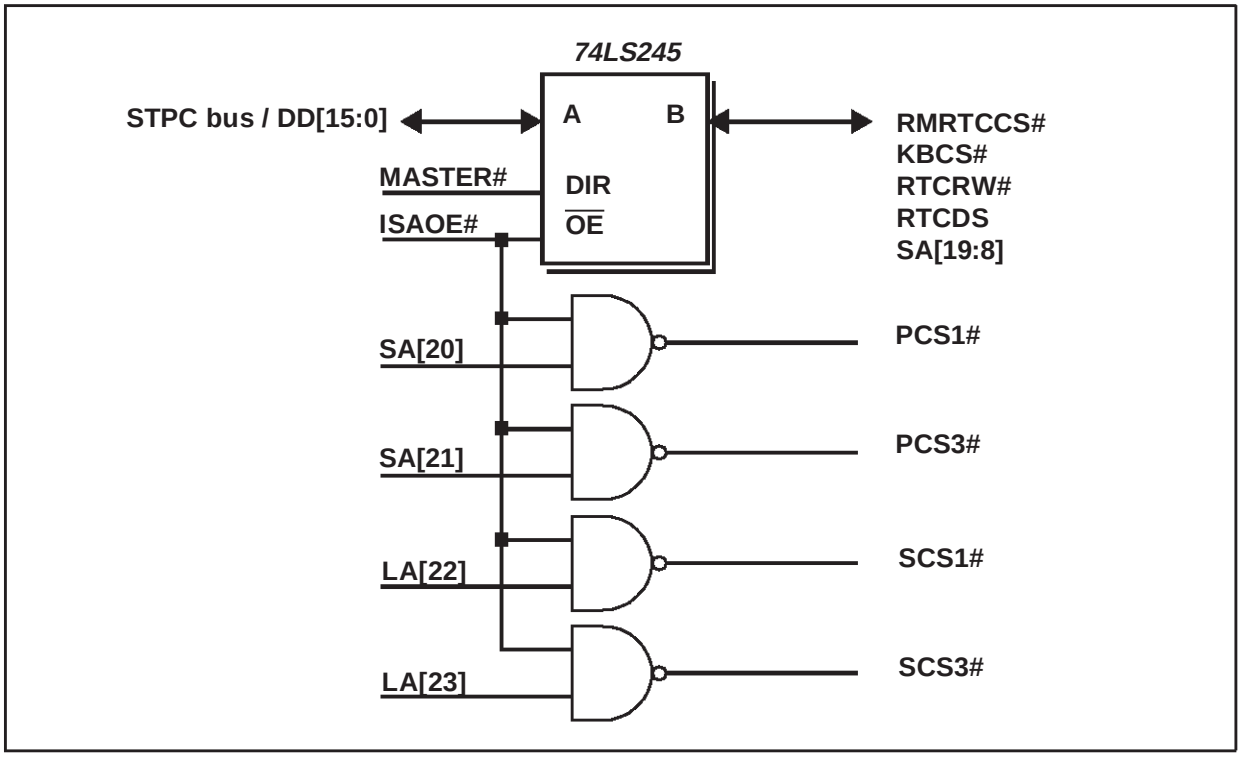


Table 2-5. Pinout.

Pin #	Pin name
AF3	SYSRSETI#
AE4	SYSRSETO#
A3	XTALI
C4	XTALO
G23	HCLK[2]
H24	GP_CLK
AF15	MCLKI
AB23	MCLKO
AE16	MA[0]
AD15	MA[1]
AF16	MA[2]
AE17	MA[3]
AD16	MA[4]
AF17	MA[5]
AE18	MA[6]
AD17	MA[7]
AF18	MA[8]
AE19	MA[9]
AE20	MA[10]
AC19	BA[0]
AF22	CS#[0]
AD21	CS#[1]
AE24	CS#[2]/MA[11]
AD23	CS#[3]/MA[12]/BA[1]
AF23	RAS#[0]
AD22	RAS#[1]
AE21	CAS#[0]
AC20	CAS#[1]
AF20	DQM#[0]
AD19	DQM#[1]
AF21	DQM#[2]
AD20	DQM#[3]
AE22	DQM#[4]
AE23	DQM#[5]
AF19	DQM#[6]
AD18	DQM#[7]
AC22	MWE#
R1	MD[0][3]
T2	MD[1][3]
R3	MD[2]
T1	MD[3]
R4	MD[4]
U2	MD[5]
T3	MD[6]
U1	MD[7]
For Note definition see Table 2-2 Definition of Signal Pins	

Pin #	Pin name
U4	MD[8][3]
V2	MD[9][3]
U3	MD[10]
V1	MD[11]
W2	MD[12]
V3	MD[13]
Y2	MD[14]
W4	MD[15]
Y1	MD[16]
W3	MD[17]
AA2	MD[18]
Y4	MD[19]
AA1	MD[20]
Y3	MD[21]
AB2	MD[22]
AB1	MD[23]
AA3	MD[24]
AB4	MD[25]
AC1	MD[26]
AB3	MD[27]
AD2	MD[28]
AC3	MD[29]
AD1	MD[30]
AF2	MD[31]
AF24	MD[32]
AE26	MD[33]
AD25	MD[34]
AD26	MD[35]
AC25	MD[36]
AC24	MD[37]
AC26	MD[38]
AB25	MD[39]
AB24	MD[40]
AB26	MD[41]
AA25	MD[42]
Y23	MD[43]
AA24	MD[44]
AA26	MD[45]
Y25	MD[46]
Y26	MD[47]
Y24	MD[48]
W25	MD[49][3]
V23	MD[50][3]
W26	MD[51][3]
W24	MD[52][3]
V25	MD[53][3]
V26	MD[54][3]
For Note definition see Table 2-2 Definition of Signal Pins	

Pin #	Pin name
U25	MD[55][3]
V24	MD[56][3]
U26	MD[57][3]
U23	MD[58][3]
T25	MD[59][3]
U24	MD[60][3]
T26	MD[61][3]
R25	MD[62][3]
R26	MD[63][3]
F24	PCI_CLKI[2]
D25	PCI_CLKO
B20	AD[0]
C20	AD[1]
B19	AD[2]
A19	AD[3]
C19	AD[4]
B18	AD[5]
A18	AD[6]
B17	AD[7]
C18	AD[8]
A17	AD[9]
D17	AD[10]
B16	AD[11]
C17	AD[12]
B15	AD[13]
A15	AD[14]
C16	AD[15]
B14	AD[16]
D15	AD[17]
A14	AD[18]
B13	AD[19]
D13	AD[20]
A13	AD[21]
C14	AD[22]
B12	AD[23]
C13	AD[24]
A12	AD[25]
C12	AD[26]
A11	AD[27]
D12	AD[28]
B10	AD[29]
C11	AD[30]
A10	AD[31]
D10	CBE[0]
C10	CBE[1]
A9	CBE[2]
For Note definition see Table 2-2 Definition of Signal Pins	

PIN DESCRIPTION

Pin #	Pin name
B8	CBE[3]
A8	FRAME#
B7	TRDY#
D8	IRDY#
A7	STOP#
C8	DEVSEL#
B6	PAR
D7	SERR#
A6	LOCK#
D20	PCI_REQ#[0]
C21	PCI_REQ#[1]
A21	PCI_REQ#[2]
C22	PCI_GNT#[0]
A22	PCI_GNT#[1]
B21	PCI_GNT#[2]
A5	PCI_INT[0]
C6	PCI_INT[1]
B4	PCI_INT[2]
D5	PCI_INT[3]
F2	LA[17]/DA[0]
G4	LA[18]/DA[1]
F3	LA[19]/DA[2]
F1	LA[20]/PCS1#
G2	LA[21]/PCS3#
G1	LA[22]/SCS1#
H2	LA[23]/SCS3#
J4	SA[0]
H1	SA[1]
H3	SA[2]
J2	SA[3]
J1	SA[4]
K2	SA[5]
J3	SA[6]
K1	SA[7]
K4	SA[8]
L2	SA[9]
K3	SA[10]
L1	SA[11]
M2	SA[12]
M1	SA[13]
L3	SA[14]
N2	SA[15]
M4	SA[16]
M3	SA[17]
P2	SA[18]
P4	SA[19]
For Note definition see Table 2-2 Definition of Signal Pins	

Pin #	Pin name
K25	SD[0]
L24	SD[1]
K26	SD[2]
K23	SD[3]
J25	SD[4]
K24	SD[5]
J26	SD[6]
H25	SD[7]
H26	SD[8]
J24	SD[9]
G25	SD[10]
H23	SD[11]
D24	SD[12]
C26	SD[13]
A25	SD[14]
B24	SD[15]
AD4	ISA_CLK
AF4	ISA_CLK2X
C9	OSC14M
P25	ALE
AE8	ZWS#
R23	BHE#
P26	MEMR#
R24	MEMW#
N25	SMEMR#
N23	SMEMW#
N26	IOR#
P24	IOW#
N24	MCS16#
M26	IOCS16#
M25	MASTER#
L25	REF#
M24	AEN
L26	IOCHCK#
T24	IOCHRDY
M23	ISAOE#
A4	RTCAS#
P3	RTCDS#
R2	RTCRW#
P1	RMRTCCS#
AE3	GPIOCS#
G26	PA[22][2]
A20	PA[23]
B1	PIRQ
For Note definition see Table 2-2 Definition of Signal Pins	

Pin #	Pin name
C2	SIRQ
C1	PDRQ
D2	SDRQ
D3	PDACK#
D1	SDACK#
E2	PDIOR#
E4	PDIOW#
E3	SDIOR#
E1	SDIOW#
E23	IRQ_MUX[0]
D26	IRQ_MUX[1]
E24	IRQ_MUX[2]
C25	IRQ_MUX[3]
A24	DREQ_MUX[0]
B23	DREQ_MUX[1]
C23	DACK_ENC[0]
A23	DACK_ENC[1]
B22	DACK_ENC[2]
D22	TC
N3	KBCS#
AE5	GPIO[0]
AC5	GPIO[1]
AD5	GPIO[2]
AF5	GPIO[3]
AE6	GPIO[4]
AC7	GPIO[5]
AD6	GPIO[6]
AF6	GPIO[7]
AE7	GPIO[8]
AF7	GPIO[9]
AD7	GPIO[10]
AD8	GPIO[11]
AE9	GPIO[12]
AF9	GPIO[13]
AE10	GPIO[14]
AD9	GPIO[15]
C5	SPKRD
B5	SCL
C7	SDA
B3	SCAN_ENABLE
G3	TCLK
N1	TMS
W1	TDI
AC2	TDO
For Note definition see Table 2-2 Definition of Signal Pins	

Pin #	Pin name
G24	VDD_CPUCLK_PLL[1]
F25	VDD_DEVCLK_PLL[1]
AC17	VDD_MCLKI_PLL[1]
AC15	VDD_MCLKO_PLL[1]
F26	VDD_HCLK_PLL[1]
D11	VDD_CORE[1]
L23	VDD_CORE[1]
T4	VDD_CORE[1]
AC6	VDD_CORE[1]
D6	VDD
D16	VDD
D21	VDD
F4	VDD
F23	VDD
L4	VDD
T23	VDD
AA4	VDD
AA23	VDD
AC11	VDD
AC16	VDD
AC21	VDD
E25	VDD_PLL_SKEW
A1:2	VSS
A26	VSS
B2	VSS
B25:26	VSS
C3	VSS
C24	VSS
D4	VSS
D9	VSS
D14	VSS
D19	VSS
D23	VSS
H4	VSS
J23	VSS
L11:16	VSS
M11:16	VSS
N4	VSS
N11:16	VSS
P11:16	VSS
P23	VSS
R11:16	VSS
T11:16	VSS
V4	VSS
W23	VSS
AC4	VSS
For Note definition see Table 2-2 Definition of Signal Pins	

Pin #	Pin name
AC8	VSS
AC13	VSS
AC18	VSS
AC23	VSS
AD3	VSS
AD14	VSS
AD24	VSS
AE1:2	VSS
AE25	VSS
AF1	VSS
AF25	VSS
AF26	VSS
AD11	*Unconnected*
AC9	*Unconnected*
AC10	*Unconnected*
AC12	*Unconnected*
AC14	*Unconnected*
AD10	*Unconnected*
AD12	*Unconnected*
AD13	*Unconnected*
AE11	*Unconnected*
AE12	*Unconnected*
AE13	*Unconnected*
AE14	*Unconnected*
AE15	*Unconnected*
AF8	*Unconnected*
AF10	*Unconnected*
AF11	*Unconnected*
AF12	*Unconnected*
AF13	*Unconnected*
AF14	*Unconnected*
A16	*Unconnected*
B11	*Unconneted*
B9	*Unconnected*
D18	*Unconnected*
E26	*Unconnected*
C15	*Unconnected*
For Note definition see Table 2-2 Definition of Signal Pins	

3 STRAP OPTION

This chapter defines the Strap Options and their location.

Some strap options have been left programmable for future versions of silicon.

.

Memory Data Lines	Refer to	Designation	Location	Actual Settings	Set to '0'	Set to '1'
MD0		*Reserved*	Index 4A, bit 0	-	-	-
MD1		*Reserved*	Index 4A, bit 1	-	-	-
MD2	HCLK PLL Speed	HCKL_PLL	Index 5F, bit 6	User defined	see Section 3.1.4	
MD3	HCLK PLL Speed	HCKL_PLL	Index 5F, bit 7	User defined		
MD4	PCI Clock	PCI_CLKO divisor	Index 4A, bit 4	User defined	see Section 3.1.3	
MD5	MCKL	MCLK_HCLK_Synch	Index4, bit 5	User defined	Unsynch	Synchronized
MD6	PCI Clock	PCI_CLK Setup	Index 4A, bit 6	User defined	see Section 3.1.1	
MD7			Index 4A, bit 7	User defined		
MD8		*Reserved*	Index 4B, bit 0	-	-	-
MD9		*Reserved*	Index 4B, bit 1	-	-	-
MD10	PCI Clock	PCI_CLKI Skew	Index 4B, bit 2	User defined	Enabled	Bypassed
MD11			Index 4B, bit 3	User defined	Default	User control
MD12			Index 4B, bit 4	User defined	Disable	Enabled
MD13			Index 4B, bit 5	User defined	Disable	Enabled
MD14		*Reserved*	Index 4B, bit 6	-	-	-
MD15		*Reserved*	Index 4B, bit 7	-	-	-
MD16	GPIO	GPIO_Config	Index 4C, bit 0	User Defined	Test Mode	Normal
MD17	PCI Clock	PCI_CKLO Divisor	Index 4C, bit 1	User defined	see Section 3.1.3	
MD18	HCLK	HCLK Direction	Index 4C, bit 2	Pull Up	External	Internal
MD19	MCLKO	MCLKO Direction	Index 4C, bit 3	Pull Up	External	Internal
MD20	CPU	Clock Multiplier	Hardware	-	see Section 3.1.7	
MD21		*Reserved*	Index 5F, bit 0	Pull Up	-	-
MD22		*Reserved*	Index 5F, bit 1	Pull up	-	-
MD23		*Reserved*	Index 4C, bit 7	Pull up	-	-
MD24	HCLK	HCLK PLL Speed	Index 5F, bit 3	**MD[3:2] - MD[26:24]**		**MHz**
MD25			Index 5F, bit 4		00-000	25
MD26			Index 5F, bit 5		00-001	50
					00-010	60
					00-100	66
					01-001	75
					01-110	82.5
					10-011	90
					11-001	100
					Others	Reserved
MD27		*Reserved*	Hardware	Pull down		
MD28		*Reserved*	Hardware	Pull down		
MD29		*Reserved*	Hardware	Pull down		
MD30		*Reserved*	Hardware	Pull down		
MD31		*Reserved*	Hardware	Pull down		
MD32		*Reserved*	Hardware	Pull down		
MD33		*Reserved*	Hardware	Pull down		

Memory Data Lines	Refer to	Designation	Location	Actual Settings	Set to '0'	Set to '1'
MD34		*Reserved*	Hardware	Pull down		
MD35	CPU Clock	CPU CLK Skew	Hardware	User defined	CLK Lead	CLK Lag
MD40	CPU	Clock Multiplier	Hardware	User defined	**MD[20,40]**	**Multiplier**
					00	x1
					01	x2
					10	*Reserved*
					11	*Reserved*
MD41		*Reserved*	Hardware	Pull down	-	-
MD42		*Reserved*	Hardware	Pull up	-	-
MD43		*Reserved*	Hardware	Pull down	-	-
MD44		*Reserved*	Hardware	Pull Down	-	-
MD45	HCLK	HCLKI PLL			**MD[46:45]**	**HCLK**
MD46					00	< 32MHz
					01	32 - 64
					10	> 64MHz
					11	Disabled
MD47	SDRAM	Power On sequence	Hardware	User defined	Disabled	Enabled
MD48	MCLKI	Skew corrector PLL	Hardware	User defined	Disabled	Enabled

3.1 POWER ON STRAP REGISTERS DESCRIPTION

3.1.1 Strap register 0 Configuration Index 4Ah (Strap0)

Bits 7-6 PCICLK Programming; the PCICLK PLL is setup through MD[7:6]. The PLL setup will vary depending on the PCICLK frequency.

Bit 7	Bit 6	Description
0	0	PCICLK frequency between 16 & 32 MHz
0	1	PCICLK frequency between 32 & 64 MHz
1	0	PCICLK frequency greater than 64 MHz
1	1	Reserved

Bit 5 This bit reflects the **value sampled on MD[5] pin** and controls the MCLK/HCLK Synchronization. When MCLK and HCLK frequency are the same, when set to 1 it unifies HCLK and MCLK and so improve system performances.

Bit 4 This bit reflects the **value sampled on MD[4] pin** and controls the PCICLKO division. It works with MD[17] refer to Section 3.1.3 bit 1 for more detail.

Bits 3-2 These bits are the same as index 5Fh bits [7:6].

Bits 1-0 *Reserved*.

3.1.2 Strap register 1 Configuration Index 4Bh (Strap1)

Bits 7-6 *Reserved*.

Bits 5-4 These bits reflect the **value sampled on MD[13:12] pin** and controls t he deskew logic on PCICLKI. If bit 3 is set to 1, this programmes the 2 MSB of the delay start point of the deskewer.

Bit 3 This bit reflects the **value sampled on MD[11] pin** and controls the deskew logic on PCI-CLKI. If 1, it allows the user to control the starting point of this logic (see bits 5-4 above). If 0, we use default start.

Bit 2 This bit reflects the **value sampled on MD[10] pin** and controls the deskew logic on PCI-CLKI. If 0, this logic is enabled, if 1 it is bypassed.

Bits 1-0 *Reserved*.

3.1.3 Strap register 2 Configuration Index 4Ch (Strap2)

Bits 7-4 *Reserved*.

Bit 3 This bit reflects the **value sampled on MD[19] pin** and controls the Memory clock output (MCLKO) source as follows:

0: External. MCLKO pin is tristated.

1: Internal. MCLKO pin is an output and is connected to the internal frequency synthesizer output.

Bit 2 This bit reflects the **value sampled on MD[18] pin** and controls the Host/CPU clock source as follows:

0: External. HCLK pin is an input.

1: Internal. HCLK pin is an output and is connected to the internal frequency synthesizer output.

Bit 1 This bit reflects the **value sampled on MD[17] pin** and controls the PCI clock output as follows and is programmed in parallel with MD[4]:

MD[4]	MD[17]	Description
0	0	PCI clock output = HCLK / 4
0	1	PCI clock output = HCLK / 4
1	0	PCI clock output = HCLK / 3
1	1	PCI clock output = HCLK / 2

Bit 0 This bit reflects the **value sampled on MD[16] pin** and controls the configuration of GPIO[8:0].

0: Configured as test bus.

1: Configured as normal IOs.

This register defaults to the values sampled on MD[23] & MD[20:16] pins after re set.

3.1.4 Strap register 0 Configuration Index 5Fh

Bits 7-3 These bits reflect the **values sampled on MD[3:2] and MD[26:24] pins** respectively and control the Host clock frequency synthesizer as follows:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	HCLK Frequency
0	0	0	0	0	25 MHz
0	0	0	0	1	50 MHz
0	0	0	1	0	60 MHz
0	0	0	1	1	66 MHz
0	1	0	0	1	75 MHz
0	1	1	1	0	82.5 MHz
1	0	0	1	1	90 MHz
1	1	0	0	1	100 MHz

Bit 2-0 *Reserved*

This register defaults to the values sampled on above pins after reset.

3.1.5 Delay Programming For DLL

The bits MD[30:27] are used to set the delay of the host clock entering the on c hip DLL used to generate PCI_CLKO that is synchronous with HCLK. these bits must be set to the values stated in the table above.

3.1.6 HCLKI Programming

The HCLKI clock signal is selected and programmed through strap values on MD[35:31] & MD[46:45].

MD[46:45] set the source of the HCLKI and the programming value if the PLL option is chosen.

MD[46:45] HCLKI source

Bit 46	Bit 45	HCLK Source
0	0	HCLKI PLL enabled & HCLKI frequency between 16 & 32 MHz
0	1	HCLKI PLL enabled & HCLKI frequency between 32 & 64 MHz
1	0	HCLKI PLL enabled & HCLKI frequency greater than 64 MHz
1	1	HCLKI PLL disabled; delay chains selected

The bits MD[35:31] are used to set the correct skew between the chipset host clock (HCLKI) and the CPU clock. MD[35] controls whether the CPU clock leads (strap to vss) or lags (strap to vdd) the chipset host clock. MD[34:31] must be set to the values stated in the table above. These bits are only enabled when MD[46:45] are set to 11.

3.1.7 X86 Clock Programming

The bits MD[40] and MD[20] are used to set the clock multiplication factor of the 486 core.

MD20	MD40	X86 Mode
0	0	X1(x1)
0	1	X2 (x2)
1	0	*Reserved*
1	1	*Reserved*

The default value of the resistors on these strap inputs should be 2 resistors to gnd (DX mode).

3.1.8 SDRAMC Power On Sequence

This bit reflects the **value sampled on MD[47] pin**. When this bit is strapped to logic one, then the SDRAM power on sequence is activated. When strapped to logic one the power on sequence is disabled.

3.1.9 MCLKI Selection

This bit reflects the **value sampled on MD[48] pin**. When this bit is strapped to logic one, then the MCLKI skew corrector PLL is disabled; otherwise it is enabled, as it should be in user mode.

4 ELECTRICAL SPECIFICATIONS

4.1 Introduction

The electrical specifications in this chapter are valid for the STPC Elite.

4.2 Electrical Connections

4.2.1 Power/Ground Connections/Decoupling

Due to the high frequency of operation of the STPC Elite, it is necessary to install and test this device using standard high frequency techniques. The high clock frequencies used in the STPC Elite and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the VSS and VDD pins.

4.2.2 Unused Input Pins

All inputs not used by the designer and not listed in the table of pin connections in Chapter 3 should be connected either to VDD or to VSS. Connect active-high inputs to VDD through a 20 kΩ (±10%) pull-down resistor and active-low inputs to VSS and connect active-low inputs to VCC through a 20 kΩ (±10%) pull-up resistor to prevent spurious operation.

4.2.3 Reserved Designated Pins

Pins designated reserved should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

4.3 Absolute Maximum Ratings

The following table lists the absolute maximum ratings for the STPC Elite device. Stresses beyond those listed under Table 4-1 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those specified in section 14.4 ”Operating Conditions”. Exposure to conditions beyond Table 4-1 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings (Table 4-1) may also result in reduced useful life and reliability.

Table 4-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
V_{DDx}	DC Supply Voltage	-0.3	4.0	V
V_{CORE}	DC Supply Voltage for Core		2.75	V
V_I, V_O	Digital Input and Output Voltage	-0.3	VDD + 0.5	V
V_{5T}	5Volt Tolerance		5.5	V
V_{ESD}	ESD Capacity (Human body mode)		2000	V
T_{STG}	Storage Temperature	-40	+150	°C
T_{OPER}	Operating Temperature (Tcase)	-40	+115°	°C
P_{TOT}	Total Power Dissipation (package)		5	W

4.4 DC Characteristics

Table 4-2. DC Characteristics

Recommended Operating conditions :

VDD = 3.3V ±0.3V, Vcore = 2.5V ±0.25V, Tcase = -40 to 115°C unless otherwise specified

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
V_{CORE}	Operating Voltage		2.25	2.50	2.75	V
V_{DD5}	5V operating voltage	Note 3	4.5	5	5.5	V
P_{DD}	Supply Power	V_{DD} = 3.3V, V_{CORE} = 2.5V, H_{CLK} = 100Mhz		1.5		W
H_{CLK}	Internal Clock	(Note 1)			133	MHz
V_{OL}	Output Low Voltage	I_{Load} =1.5 to 8mA depending of the pin			0.5	V
V_{OH}	Output High Voltage	I_{Load} =-0.5 to -8mA depending of the pin	2.4			V
V_{IL}	Input Low Voltage	Except XTALI	-0.3		0.8	V
		XTALI	-0.3		0.9	V
V_{IH}	Input High Voltage (Note 3)	Except XTALI	2		V_{DD}+0.5	V
		XTALI	2.35		V_{DD}+0.5	V
I_{LK}	Input Leakage Current	Input, I/O	-1		2	µA
C_{IN}	Input Capacitance	(Note 2)				pF
C_{OUT}	Output Capacitance	(Note 2)				pF
C_{CLK}	Clock Capacitance	(Note 2)				pF

Notes:

1. MHz ratings refer to CPU clock frequency.
2. Not 100% tested.
3. Consider VDD = 5V for 5V tolerant I/Os.

4.5 AC Characteristics

Table 4-4 through Table 4-7 list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1 and Figure 4-2. The rising clock edge reference level VREF , and other reference levels are shown in Table 4-3 below for the STPC Elite. Input or output signals must cross these levels during testing.

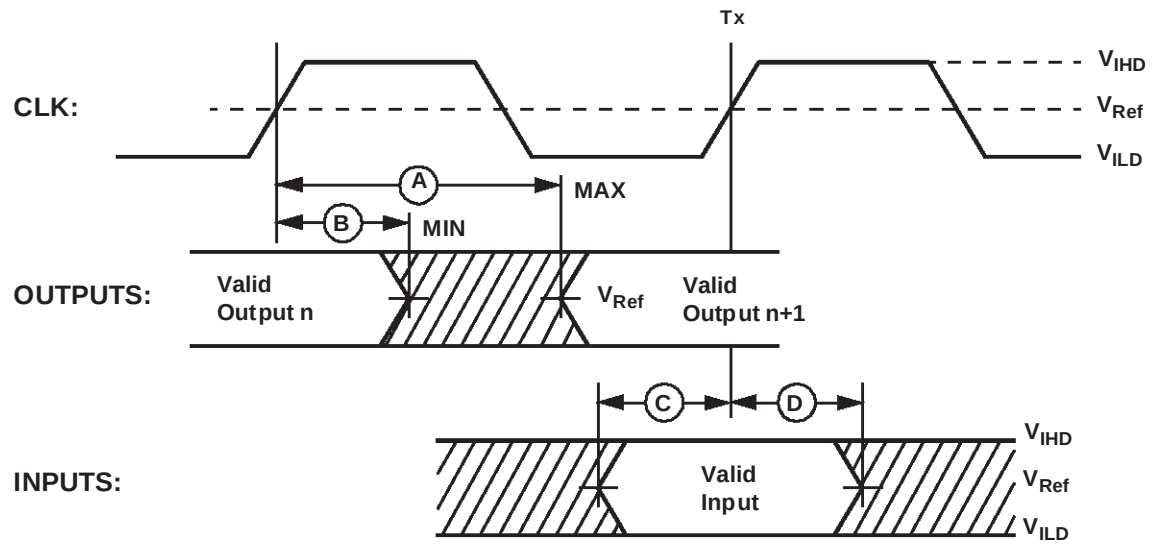
Figure 4-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

Table 4-3. Drive Level and Measurement Points for Switching Characteristics

Symbol	Value	Units
V_{REF}	1.5	V
V_{IHD}	3.0	V
V_{ILD}	0.0	V

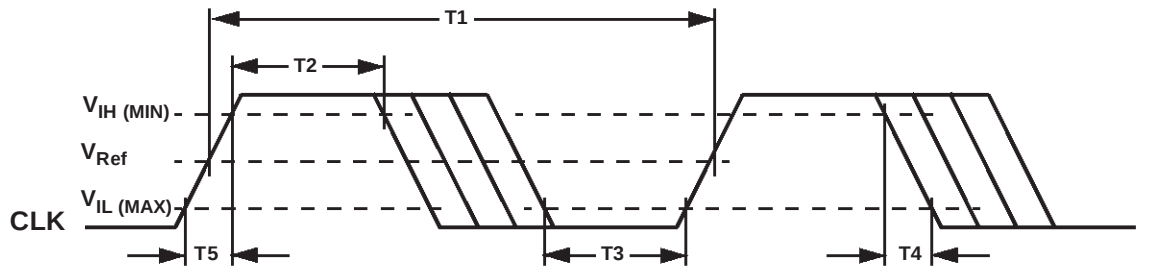
Note: Refer to Figure 4-1.

Figure 4-1. Drive Level and Measurement Points for Switching Characteristics



LEGEND:
A - Maximum Output Delay Specification
B - Minimum Output Delay Specification
C - Minimum Input Setup Specification
D - Minimum Input Hold Specification

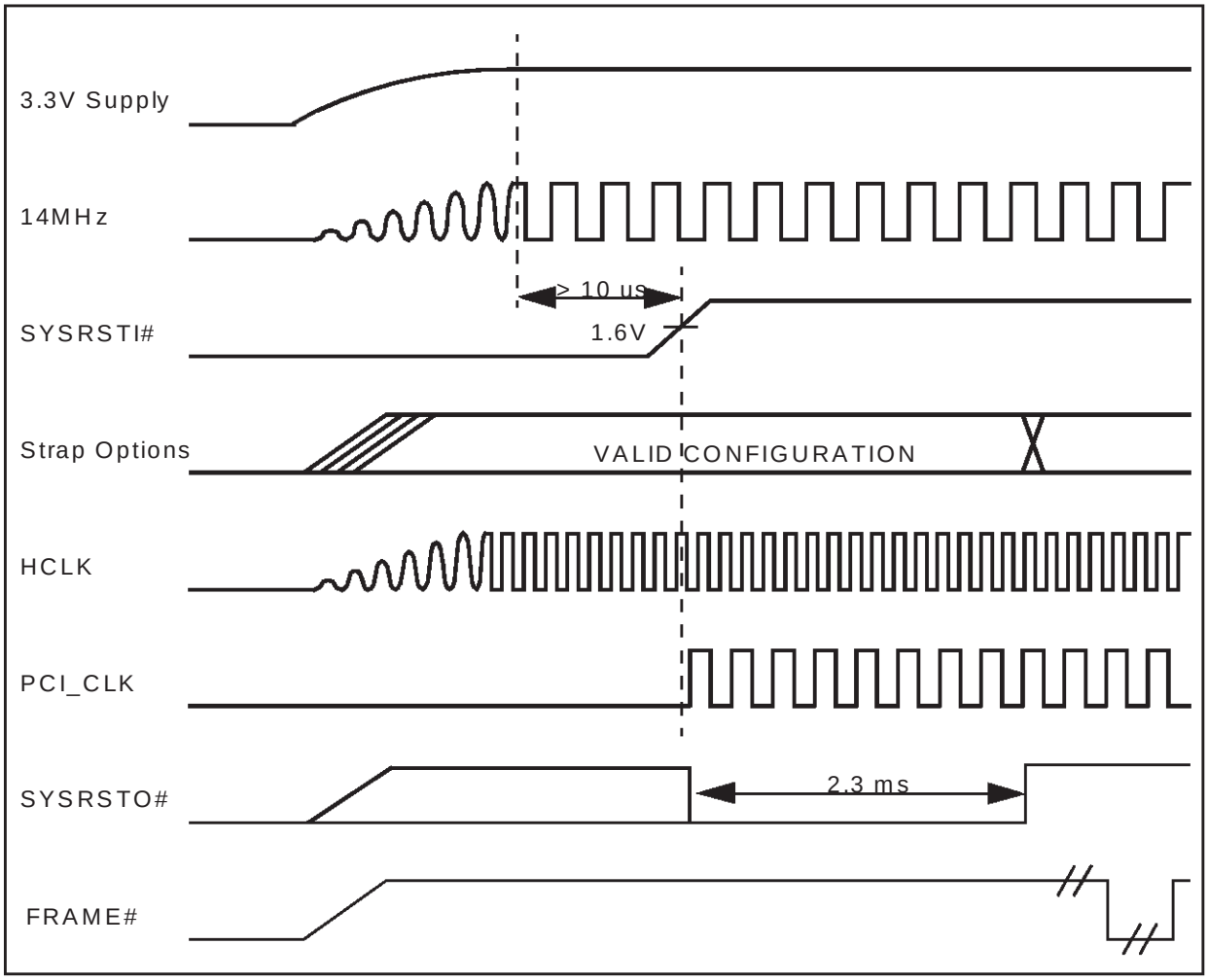
Figure 4-2. CLK Timing Measurement Points



LEGEND:
T1 - One Clock Cycle
T2 - Minimum Time at V_{IH}
T3 - Minimum Time at V_{IL}
T4 - Clock Fall Time
T5 - Clock Rise Time

NOTE; All signals are sampled on the rising edge of the CLK.

4.5.1 POWER ON SEQUENCE



SYSRSTI# has no constraint on its rising time but needs to be set to high at least 10µs after power supply is stable.

Strap Options are continuously sampled during SYSRSTI# low and should be stable. Once SYSRSTI# is high, they MUST NOT CHANGE until SYSRSTO# is high.

4.5.2 AC Timing characteristics

Table 4-4. PCI Bus AC Timing

Name	Parameter	Min	Max	Unit
t1	PCI_CLKI to AD[31:0] valid	2	11	ns
t2	PCI_CLKI to $\overline{\text{FRAME}}$ valid	2	11	ns
t3	PCI_CLKI to $\overline{\text{CBE}}$[3:0] valid	2	11	ns
t4	PCI_CLKI to PAR valid	2	11	ns
t5	PCI_CLKI to $\overline{\text{TRDY}}$ valid	2	11	ns
T6	PCI_CLKI to $\overline{\text{IRDY}}$ valid	2	11	ns
T7	PCI_CLKI to $\overline{\text{STOP}}$ valid	2	11	ns
T8	PCI_CLKI to $\overline{\text{DEVSEL}}$ valid	2	11	ns
T9	PCI_CLKI to $\overline{\text{PCI\_GNT}}$ valid	2	12	ns
t10	AD[31:0] bus setup to PCI_CLKI	7		ns
t11	AD[31:0] bus hold from PCI_CLKI	0		ns
t12	$\overline{\text{PCI\_REQ}}$[2:0] setup to PCI_CLKI	10		ns
t13	$\overline{\text{PCI\_REQ}}$[2:0] hold from PCI_CLKI	0		ns
t14	$\overline{\text{CBE}}$[3:0] setup to PCI_CLKI	7		ns
t15	$\overline{\text{CBE}}$[3:0] hold to PCI_CLKI	0		ns
t16	$\overline{\text{IRDY}}$ setup to PCI_CLKI	7		ns
t17	$\overline{\text{IRDY}}$ hold to PCI_CLKI	0		ns
t18	$\overline{\text{FRAME}}$ setup to PCI_CLKI	7		ns
t19	$\overline{\text{FRAME}}$ hold from PCI_CLKI	0		ns

Table 4-5. IDE Bus AC Timing

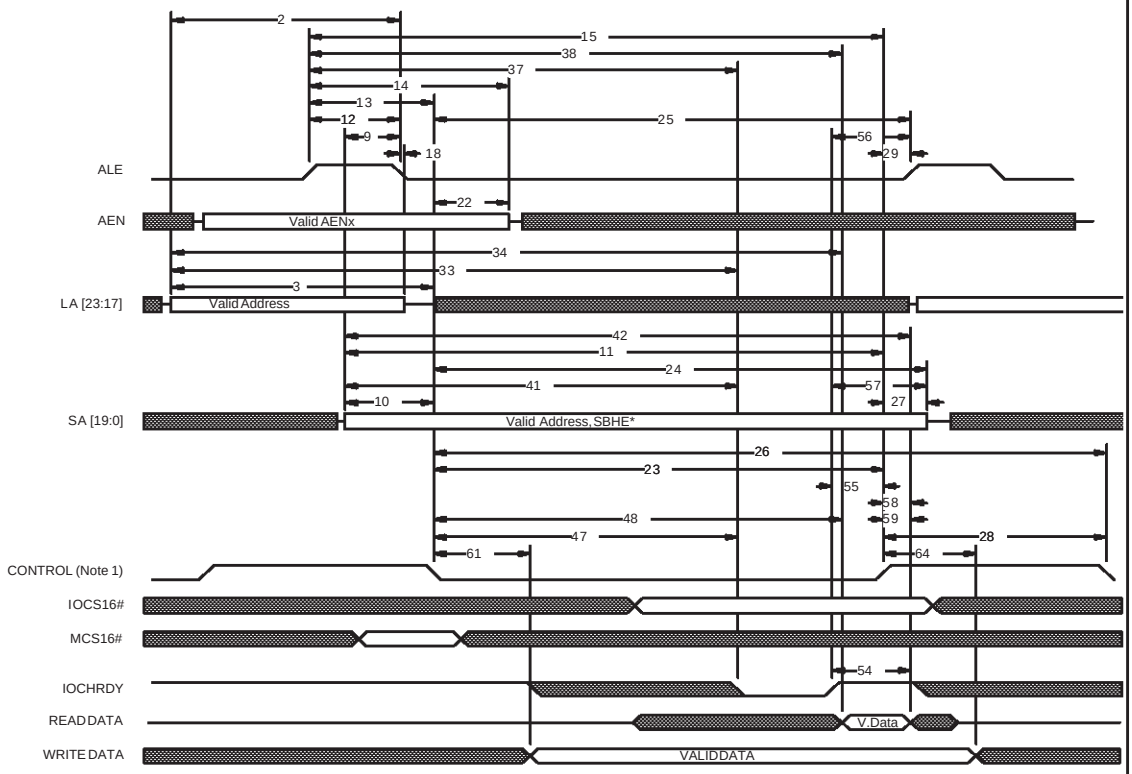
Name	Parameter	Min	Max	Unit
t20	DD[15:0] setup to $\overline{\text{PIOR}}$/$\overline{\text{SIOR}}$ falling	15		ns
t21	DD[15:0} hold to $\overline{\text{PIOR}}$/$\overline{\text{SIOR}}$ falling	12		ns

Table 4-6. SDRAM Bus AC Timing

Name	Parameter	Min	Max	Unit
t22	MCLKI to output signal valid on MA[11:0], RAS#[1:0], CAS#[1:0], MWE#	1.5	6.2	ns
t23	MCLKI to output signal valid on CS#	1.5	7.6	ns
t24	MCLKI to output signal valid on DQM[7:0]	1.5	8.1	ns
t25	MCLKI to output signal valid on MD[63:0]	1.5	8.2	ns
t26	Input setup time to MCLKI on MD[63:0]	3.1	-	ns
t27	Input hold time from MCLKI on MD[[63:0]	3.0	-	ns

4.5.3 ISA INTERFACE AC TIMING CHARCTERISTICS

Figure 4-3 ISA Cycle (ref table Table 4-7**)**



Note 1; Stands for SMEMR#, SMEMW#, MEMR#, MEMW#, IOR# & IOW#.

Note; The clock has not been represented as it cannot be accuratly represented depending on the ISA Slave mode.

Table 4-7. ISA Bus AC Timing

Name	Parameter	Min	Max	Units
2[4]	LA[23:17] valid before ALE# negated	5T		Cycles
3[4]	**LA[23:17] valid before MEMR#, MEMW# asserted**			
3a[4]	Memory access to 16 bit ISA Slave	5T		Cycles
3b[4]	Memory access to 8 bit ISA Slave	5T		Cycles
9[4]	SA[19:0] & SBHE valid before ALE# negated	1T		Cycles
10[4]	**SA[19:0] & SBHE valid before MEMR#, MEMW# asserted**			
10a[4]	Memory access to 16 bit ISA Slave	2T		Cycles
10b[4]	Memory access to 8 bit ISA Slave	2T		Cycles
10[4]	**SA[19:0] & SHBE valid before SMEMR#, SMEMW# asserted**			
10c[4]	Memory access to 16 bit ISA Slave	2T		Cycle
10d[4]	Memory access to 8 bit ISA Slave	2T		Cycle

Note; The signal numbering refers to Table 4-3

Note 4; These timings are extracted from simulations and are not garanteed by testing

Table 4-7. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
10e[4]	SA[19:0] & SBHE valid before IOR#, IOW# asserted		2T		Cycles
11[4]	**XTALO to IOW# valid**				
11a[4]		Memory access to 16 bit ISA Slave - 2BCLK	2T		Cycles
11b[4]		Memory access to 16 bit ISA Slave - Standard 3BCLK	2T		Cycles
11c[4]		Memory access to 16 bit ISA Slave - 4BCLK	2T		Cycles
11d[4]		Memory access to 8 bit ISA Slave - 2BCLK	2T		Cycles
11e[4]		Memory access to 8 bit ISA Slave - Standard 3BCLK	2T		Cycles
12[4]	ALE# asserted before ALE# negated		1T		Cycles
13[4]	**ALE# asserted before MEMR#, MEMW# asserted**				
13a[4]		Memory Access to 16 bit ISA Slave	2T		Cycles
13b[4]		Memory Access to 8 bit ISA Slave	2T		Cycles
13[4]	**ALE# asserted before SMEMR#, SMEMW# asserted**				
13c[4]		Memory Access to 16 bit ISA Slave	2T		Cycles
13d[4]		Memory Access to 8 bit ISA Slave	2T		Cycles
13e[4]	ALE# asserted before IOR#, IOW# asserted		2T		Cycles
14[4]	**ALE# asserted before AL[23:17]**				
14a[4]		Non compressed	15T		Cycles
14b[4]		Compressed	15T		Cycles
15[4]	**ALE# asserted before MEMR#, MEMW#, SMEMR#, SMEMW# negated**				
15a[4]		Memory Access to 16 bit ISA Slave- 4 BCLK	11T		Cycles
15e[4]		Memory Access to 8 bit ISA Slave- Standard Cycle	11T		Cycles
18a[4]	ALE# negated before LA[23:17] invalid (non compressed)		14T		Cycles
18a[4]	ALE# negated before LA[23:17] invalid (compressed)		14T		Cycles
22[4]	**MEMR#, MEMW# asserted before LA[23:17]**				
22a[4]		Memory access to 16 bit ISA Slave.	13T		Cycles
22b[4]		Memory access to 8 bit ISA Slave.	13T		Cycles
23[4]	**MEMR#, MEMW# asserted before MEMR#, MEMW# negated**				
23b[4]		Memory access to 16 bit ISA Slave Standard cycle	9T		Cycles
23e[4]		Memory access to 8 bit ISA Slave Standard cycle	9T		Cycles
23[4]	**SMEMR#, SMEMW# asserted before SMEMR#, SMEMW# negated**				
23h[4]		Memory access to 16 bit ISA Slave Standard cycle	9T		Cycles
23l[4]		Memory access to 16 bit ISA Slave Standard cycle	9T		Cycles
23[4]	**IOR#, IOW# asserted before IOR#, IOW# negated**				
23o[4]		Memory access to 16 bit ISA Slave Standard cycle	9T		Cycles
23r[4]		Memory access to 8 bit ISA Slave Standard cycle	9T		Cycles
24[4]	**MEMR#, MEMW# asserted before SA[19:0]**				
24b[4]		Memory access to 16 bit ISA Slave Standard cycle	10T		Cycles
24d[4]		Memory access to 8 bit ISA Slave - 3BLCK	10T		Cycles
24e[4]		Memory access to 8 bit ISA Slave Standard cycle	10T		Cycles
24f[4]		Memory access to 8 bit ISA Slave - 7BCLK	10T		Cycles
24[4]	**SMEMR#, SMEMW# asserted before SA[19:0]**				
24h		Memory access to 16 bit ISA Slave Standard cycle	10T		Cycles
24i[4]		Memory access to 16 bit ISA Slave - 4BCLK	10T		Cycles
24k[4]		Memory access to 8 bit ISA Slave - 3BCLK	10T		Cycles
24l[4]		Memory access to 8 bit ISA Slave Standard cycle	10T		Cycles
Note; The signal numbering refers to Table 4-3					
Note 4; These timings are extracted from simulations and are not garanteed by testing					

Table 4-7. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
24[4]	**IOR#, IOW# asserted before SA[19:0]**				
	24o[4]	I/O access to 16 bit ISA Slave Standard cycle	19T		Cycles
	24r[4]	I/O access to 16 bit ISA Slave Standard cycle	19T		Cycles
25[4]	**MEMR#, MEMW# asserted before next ALE# asserted**				
	25b[4]	Memory access to 16 bit ISA Slave Standard cycle	10T		Cycles
	25d[4]	Memory access to 8 bit ISA Slave Standard cycle	10T		Cycles
25[4]	**SMEMR#, SMEMW# asserted before next ALE# aserted**				
	25e[4]	Memory access to 16 bit ISA Slave - 2BCLK	10T		Cycles
	25f[4]	Memory access to 16 bit ISA Slave Standard cycle	10T		Cycles
	25h[4]	Memory access to 8 bit ISA Slave Standard cycle	10T		Cycles
25[4]	**IOR#, IOW# asserted before next ALE# asserted**				
	25i[4]	I/O access to 16 bit ISA Slave Standard cycle	10T		Cycles
	25k[4]	I/O access to 16 bit ISA Slave Standard cycle	10T		Cycles
26[4]	**MEMR#, MEMW# asserted before next MEMR#, MEMW# asserted**				
	26b[4]	Memory access to 16 bit ISA Slave Standard cycle	12T		Cycles
	26d[4]	Memory access to 8 bit ISA Slave Standard cycle	12T		Cycles
26[4]	**SMEMR#, SMEMW# asserted before next SMEMR#, SMEMW# asserted**				
	26f[4]	Memory access to 16 bit ISA Slave Standard cycle	12T		Cycles
	26h[4]	Memory access to 8 bit ISA Slave Standard cycle	12T		Cycles
26[4]	**IOR#, IOW# asserted before next IOR#, IOW# asserted**				
	26i[4]	I/O access to 16 bit ISA Slave Standard cycle	12T		Cycles
	26k[4]	I/O access to 8 bit ISA Slave Standard cycle	12T		Cycles
28[4]	**Any command negated to MEMR#, SMEMR#, MEMR#, SMEMW# asserted**				
	28a[4]	Memory access to 16 bit ISA Slave	3T		Cycles
	28b[4]	Memory access to 8 bit ISA Slave	3T		Cycles
28[4]	**Any command negated to IOR#, IOW# asserted**				
	28c[4]	I/O access to ISA Slave	3T		Cycles
29a[4]	MEMR#, MEMW# negated before next ALE# asserted		1T		Cycles
29b[4]	SMEMR#, SMEMW# negated before next ALE# asserted		1T		Cycles
29c[4]	IOR#, IOW# negated before next ALE# asserted		1T		Cycles
33[4]	**LA[23:17] valid to IOCHRDY negated**				
	33a[4]	Memory access to 16 bit ISA Slave - 4 BCLK	8T		Cycles
	33b[4]	Memory access to 8 bit ISA Slave - 7 BCLK	14T		Cycles
34[4]	**LA[23:17] valid to read data valid**				
	34b[4]	Memory access to 16 bit ISA Slave Standard cycle	8T		Cycles
	34e[4]	Memory access to 8 bit ISA Slave Standard cycle	14T		Cycles
37[4]	**ALE# asserted to IOCHRDY# negated**				
	37a[4]	Memory access to 16 bit ISA Slave - 4 BCLK	6T		Cycles
	37b[4]	Memory access to 8 bit ISA Slave - 7 BCLK	12T		Cycles
	37c[4]	I/O access to 16 bit ISA Slave - 4 BCLK	6T		Cycles
	37d[4]	I/O access to 8 bit ISA Slave - 7 BCLK	12T		Cycles
38[4]	**ALE# asserted to read data valid**				
	38b[4]	Memory access to 16 bit ISA Slave Standard Cycle	4T		Cycles
	38e[4]	Memory access to 8 bit ISA Slave Standard Cycle	10T		Cycles
	38h[4]	I/O access to 16 bit ISA Slave Standard Cycle	4T		Cycles
Note; The signal numbering refers to Table 4-3 **Note 4; These timings are extracted from simulations and are not garanteed by testing**					

Table 4-7. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
	38l[4]	I/O access to 8 bit ISA Slave Standard Cycle	10T		Cycles
41[4]	**SA[19:0] SBHE valid to IOCHRDY negated**				
	41a[4]	Memory access to 16 bit ISA Slave	6T		Cycles
	41b[4]	Memory access to 8 bit ISA Slave	12T		Cycles
	41c[4]	I/O access to 16 bit ISA Slave	6T		Cycles
	41d[4]	I/O access to 8 bit ISA Slave	12T		Cycles
42[4]	**SA[19:0] SBHE valid to read data valid**				
	42b[4]	Memory access to 16 bit ISA Slave Standard cycle	4T		Cycles
	42e[4]	Memory access to 8 bit ISA Slave Standard cycle	10T		Cycles
	42h[4]	I/O access to 16 bit ISA Slave Standard cycle	4T		Cycles
	42l[4]	I/O access to 8 bit ISA Slave Standard cycle	10T		Cycles
47[4]	**MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW# asserted to IOCHRDY negated**				
	47a[4]	Memory access to 16 bit ISA Slave	2T		Cycles
	47b[4]	Memory access to 8 bit ISA Slave	5T		Cycles
	47c[4]	I/O access to 16 bit ISA Slave	2T		Cycles
	47d[4]	I/O access to 8 bit ISA Slave	5T		Cycles
48[4]	**MEMR#, SMEMR#, IOR# asserted to read data valid**				
	48b[4]	Memory access to 16 bit ISA Slave Standard Cycle	2T		Cycles
	48e[4]	Memory access to 8 bit ISA Slave Standard Cycle	5T		Cycles
	48h[4]	I/O access to 16 bit ISA Slave Standard Cycle	2T		Cycles
	48l[4]	I/O access to 8 bit ISA Slave Standard Cycle	5T		Cycles
54[4]	**IOCHRDY asserted to read data valid**				
	54a[4]	Memory access to 16 bit ISA Slave	1T(R)/2T(W)		Cycles
	54b[4]	Memory access to 8 bit ISA Slave	1T(R)/2T(W)		Cycles
	54c[4]	I/O access to 16 bit ISA Slave	1T(R)/2T(W)		Cycles
	54d[4]	I/O access to 8 bit ISA Slave	1T(R)/2T(W)		Cycles
55a[4]	IOCHRDY asserted to MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW# negated		1T		Cycles
55b[4]	IOCHRY asserted to MEMR#, SMEMR# negated (refresh)		1T		Cycles
56[4]	IOCHRDY asserted to next ALE# asserted		2T		Cycles
57[4]	IOCHRDY asserted to SA[19:0], SBHE invalid		2T		Cycles
58[4]	MEMR#, IOR#, SMEMR# negated to read data invalid		0T		Cycles
59[4]	MEMR#, IOR#, SMEMR# negated to daabus float		0T		Cycles
61[4]	**Write data before MEMW# asserted**				
	61a[4]	Memory access to 16 bit ISA Slave	2T		Cycles
	61b[4]	Memory access to 8 bit ISA Slave (Byte copy at end of start)	2T		Cycles
61[4]	**Write data before SMEMW# asserted**				
	61c[4]	Memory access to 16 bit ISA Slave	2T		Cycles
	61d[4]	Memory access to 8 bit ISA Slave	2T		Cycles
61[4]	**Write Data valid before IOW# asserted**				
	61e[4]	I/O access to 16 bit ISA Slave	2T		Cycles
	61f[4]	I/O access to 8 bit ISA Slave	2T		Cycles
64a[4]	MEMW# negated to write data invalid - 16 bit		1T		Cycles
64b[4]	MEMW# negated to write data invalid - 8 bit		1T		Cycles
Note; The signal numbering refers to Table 4-3					
Note 4; These timings are extracted from simulations and are not garanteed by testing					

Table 4-7. ISA Bus AC Timing

Name	Parameter	Min	Max	Units
64c[4]	SMEMW# negated to write data invalid - 16 bit	1T		Cycles
64d[4]	SMEMW# negated to write data invalid - 8 bit	1T		Cycles
64e[4]	IOW# negated to write data invalid	1T		Cycles
64f[4]	MEMW# negated to copy data float, 8 bit ISA Slave, odd Byte by ISA Master	1T		Cycles
64g[4]	IOW# negated to copy data float, 8 bit ISA Slave, odd Byte by ISA Master	1T		Cycles
Note; The signal numbering refers to Table 4-3 **Note 4; These timings are extracted from simulations and are not garanteed by testing**				

5. MECHANICAL DATA

5.1 388-Pin Package Dimension

The pin numbering for the STPC 388-pin Plastic BGA package is shown in Figure 5-1.

Dimensions are shown in Figure 5-2, Table 5-1 and Figure 5-3, Table 5-2.

Figure 5-1. 388-Pin PBGA Package - Top View

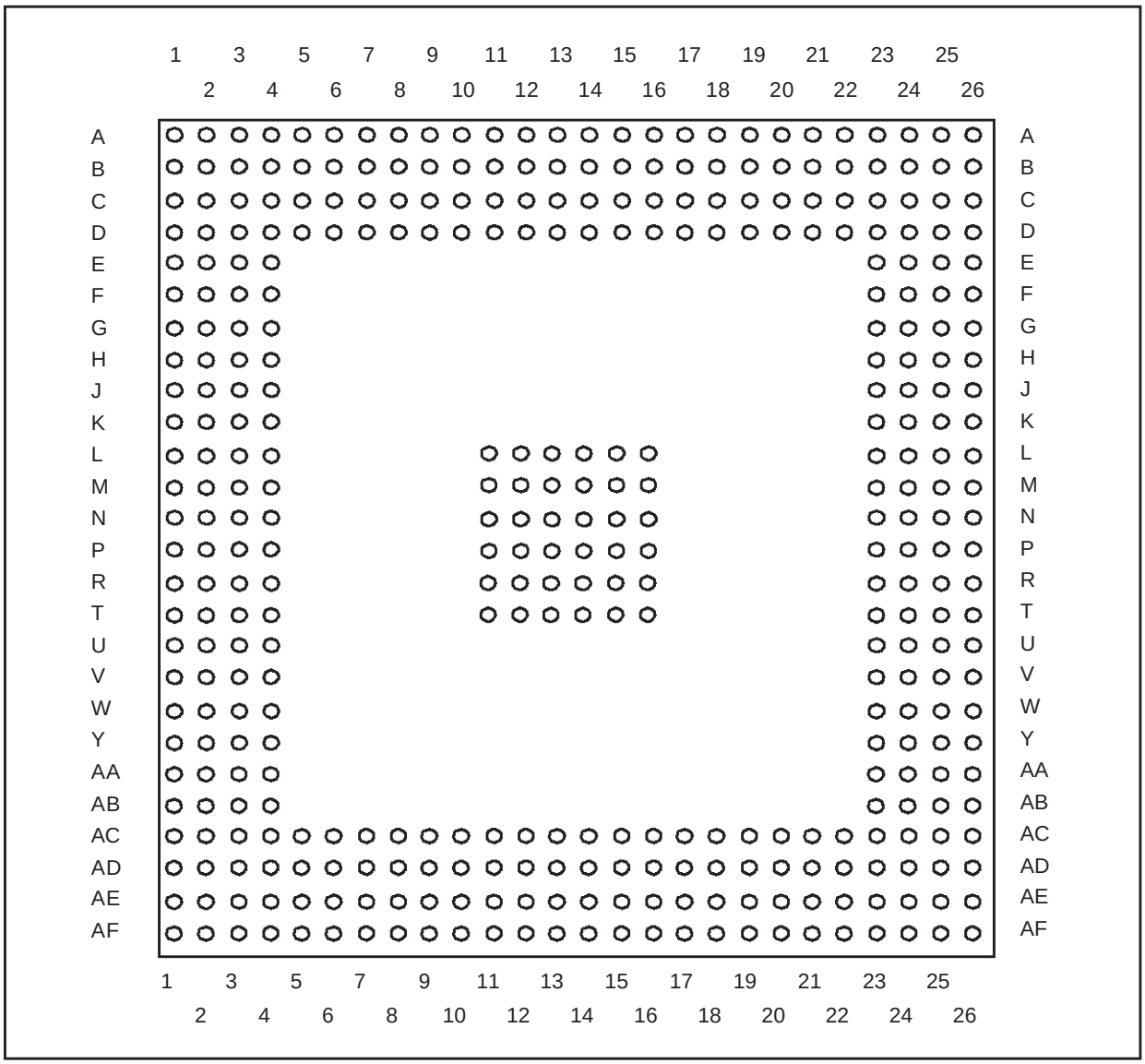


Figure 5-2. 388-pin PBGA Package - PCB Dimensions

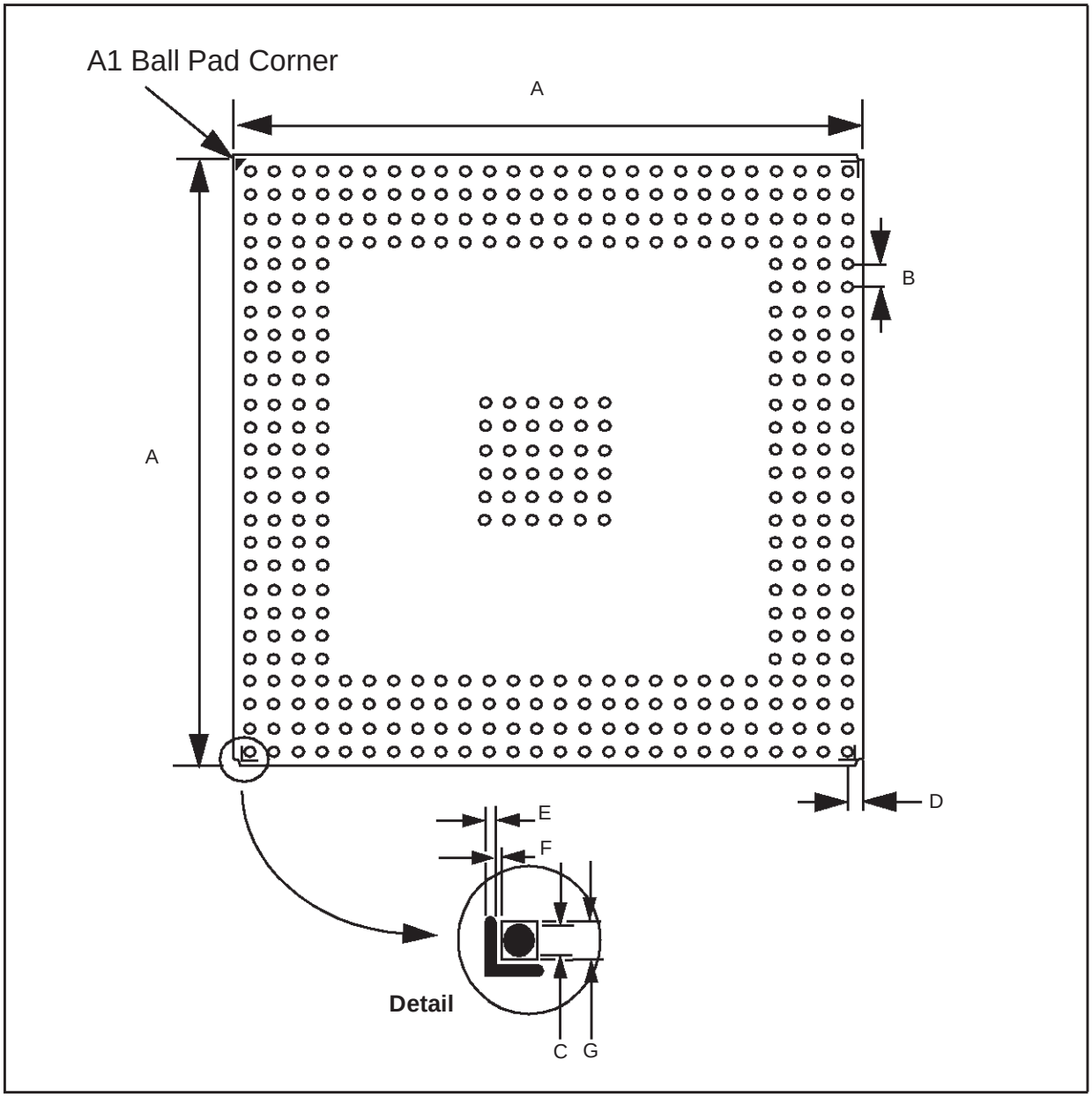


Table 5-1. 388-pin PBGA Package - PCB Dimensions

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	34.95	35.00	35.05	1.375	1.378	1.380
B	1.22	1.27	1.32	0.048	0.050	0.052
C	0.58	0.63	0.68	0.023	0.025	0.027
D	1.57	1.62	1.67	0.062	0.064	0.066
E	0.15	0.20	0.25	0.006	0.008	0.001
F	0.05	0.10	0.15	0.002	0.004	0.006
G	0.75	0.80	0.85	0.030	0.032	0.034

Figure 5-3. 388-pin PBGA Package - Dimensions

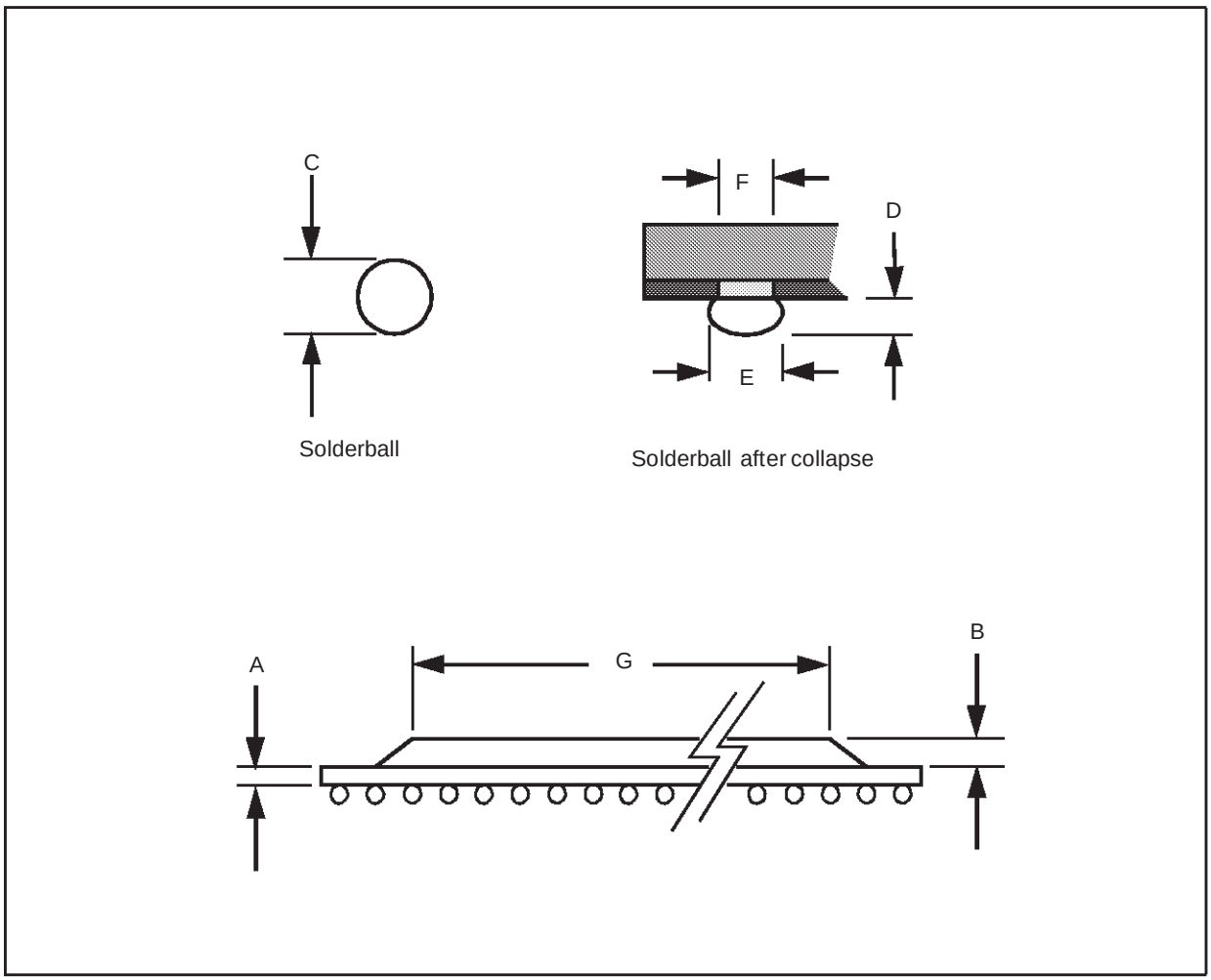


Table 5-2. 388-pin PBGA Package - Dimensions

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.56	0.62	0.020	0.022	0.024
B	1.12	1.17	1.22	0.044	0.046	0.048
C	0.60	0.76	0.92	0.024	0.030	0.036
D	0.52	0.53	0.54	0.020	0.021	0.022
E	0.63	0.78	0.93	0.025	0.031	0.037
F	0.60	0.63	0.66	0.024	0.025	0.026
G		30.0			11.8	

5.2 388-Pin Package thermal data

388-pin PBGA package has a Power Dissipation Capability of 4.5W which increases to 6W when used with a Heatsink.

Structure in shown in Figure 5-4.

Thermal dissipation options are illustrated in Figure 5-5 and Figure 5-6.

Figure 5-4. 388-Pin PBGA structure

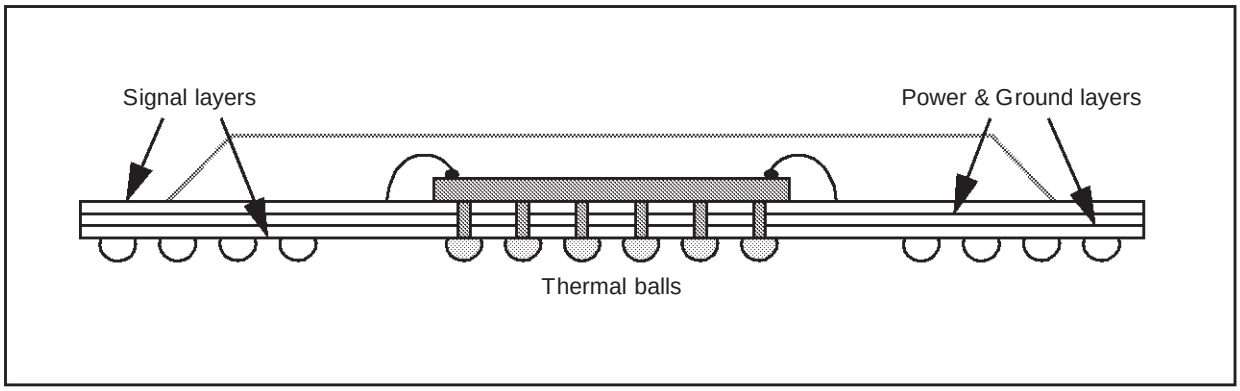


Figure 5-5. Thermal dissipation without heatsink

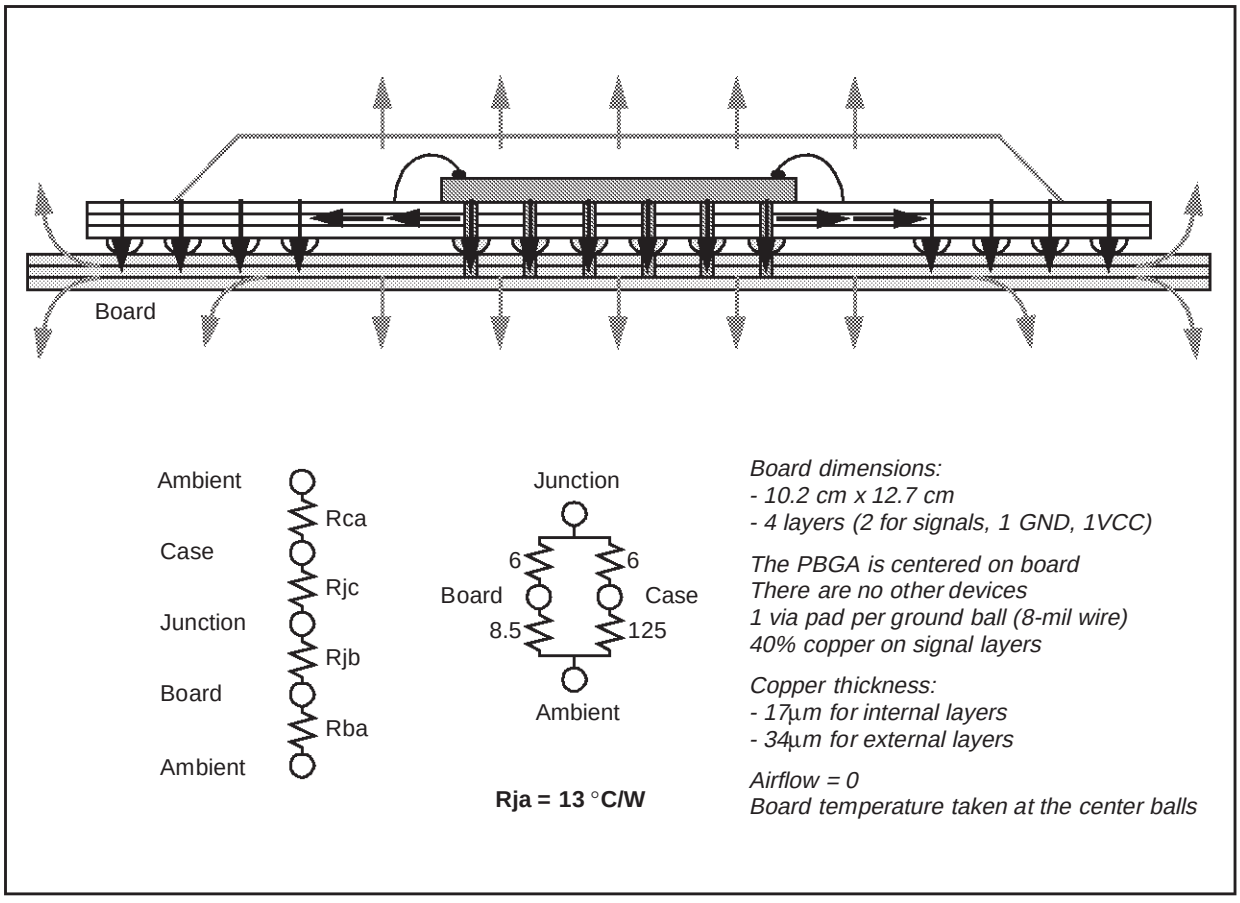
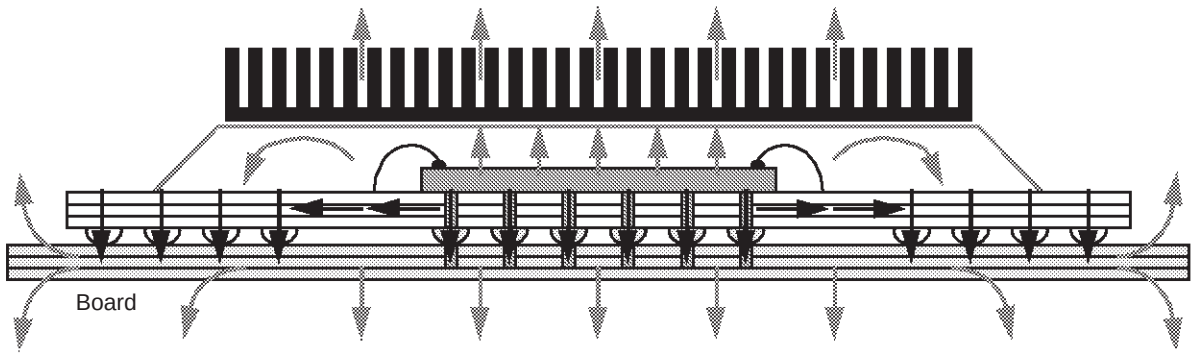
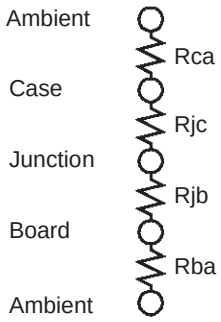
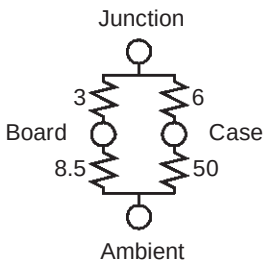


Figure 5-6. Thermal dissipation with heatsink







Rja = 9.5 °C/W

Board dimensions:
- 10.2 cm x 12.7 cm
- 4 layers (2 for signals, 1 GND, 1VCC)

The PBGA is centered on board
There are no other devices
1 via pad per ground ball (8-mil wire)
40% copper on signal layers

Copper thickness:
- 17µm for internal layers
- 34µm for external layers

Airflow = 0
Board temperature taken at the center balls
Heat sink is 11.1°C/W

6. BOARD LAYOUT

6.1 Thermal dissipation

Thermal dissipation of the STPC depends mainly on supply voltage. As a result, when the system does not need to work at 3.45V, it is interesting to reduce the voltage to 3.15V, for example, if it is possible. This may save few 100's of mW.

The second area to look at is unused interfaces and functions. Depending on the application, some input signals can be grounded, and some blocks not powered or shutdown. Clock speed dynamic adjustment is also a solution that can be used along with the integrated power management unit.

The standard way to route thermal balls to internal ground layer implements only one via pad for each ball pad, connected using a 8-mil wire.

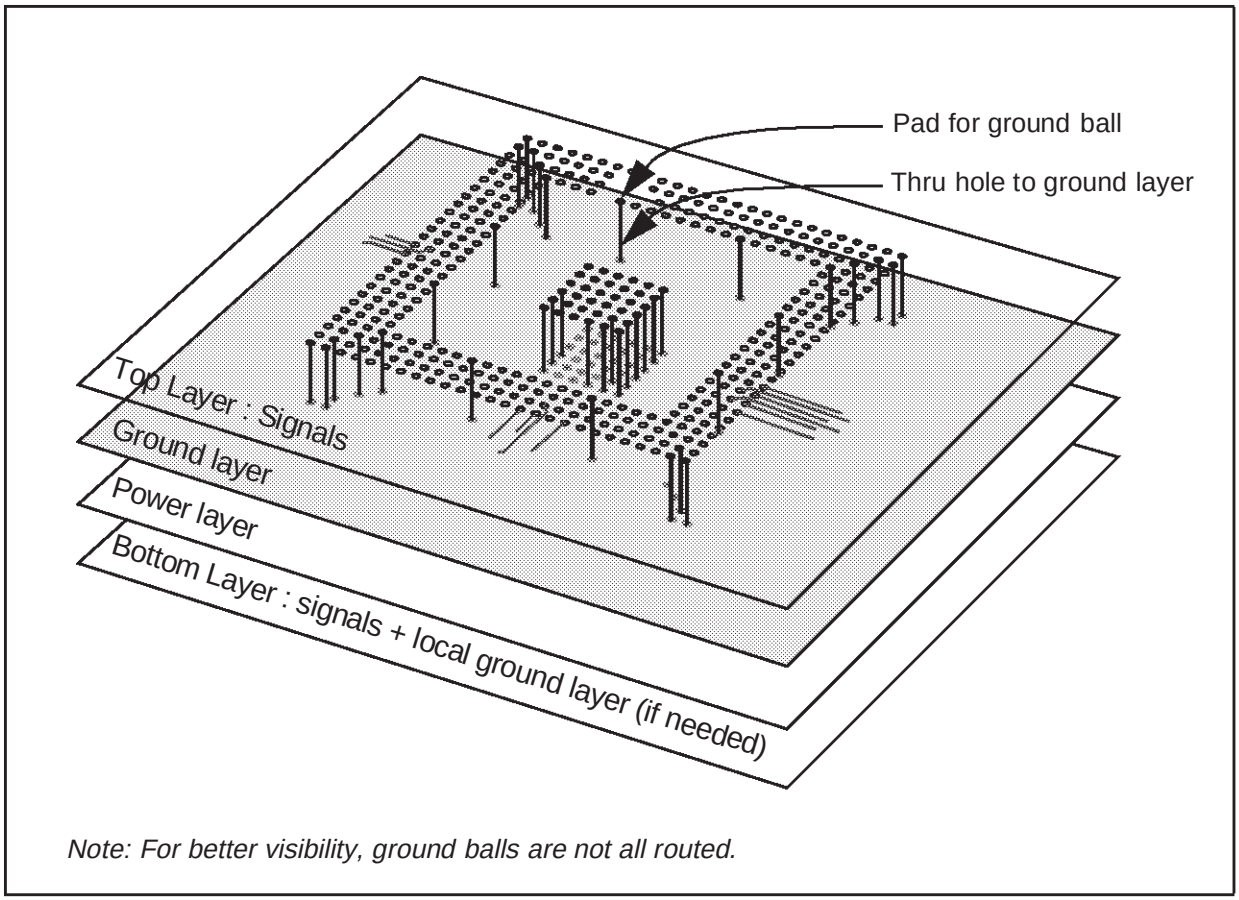
With such configuration the Plastic BGA 388 package does 90% of the thermal dissipation through the ground balls, and especially the central thermal balls which are directly connected to the die, the remaining 10% is dissipated through the case. Adding a heat sink reduces this value to 85%.

As a result, some basic rules has to be applied when routing the STPC in order to avoid thermal problems.

First of all, the whole ground layer acts as a heat sink and ground balls must be directly connected to it as illustrated in Figure 6-1.

If one ground layer is not enough, a second ground plane may be added on solder side.

Figure 6-1. Ground routing



Note: For better visibility, ground balls are not all routed.

BOARD LAYOUT

When considering thermal dissipation, the most important - and not the more obvious - part of the layout is the connection between the ground balls and the ground layer.

A 1-wire connection is shown in Figure 6-2. The use of a 8-mil wire results in a thermal resistance of 105°C/W assuming copper is used (418 W/ m.°K). This high value is due to the thickness (34 µm) of the copper on the external side of the PCB.

Considering only the central matrix of 36 thermal balls and one via for each ball, the global thermal resistance is 2.9°C/W. This can be easily improved using four 10 mil wires to connect to the four vias around the ground pad link as inFigure 6-3. This gives a total of 49 vias and a global resistance for the 36 thermal balls of 0.6°C/W.

The use of a ground plane like in Figure 6-4 is even better.

To avoid solder wicking over to the via pads during soldering, it is important to have a solder mask of 4 mil around the pad (NSMD pad), this gives a diameter of 33 mil for a 25 mil ground pad.

To obtain the optimum ground layout, place the vias directly under the ball pads. In this case no local boar d distortion is tolerated.

The thickness of the copper on PCB layers is typically 34 µm for external layers and 17 µm for internal layers. That means thermal dissipation is not good and temperature of the board is concentrated around the devices and falls quickly with increased distance.

When it is possible to place a metal layer inside the PCB, this improves dramatically the heat spreading and hence thermal dissipation of the board.

Figure 6-2. Recommended 1-wire ground pad layout

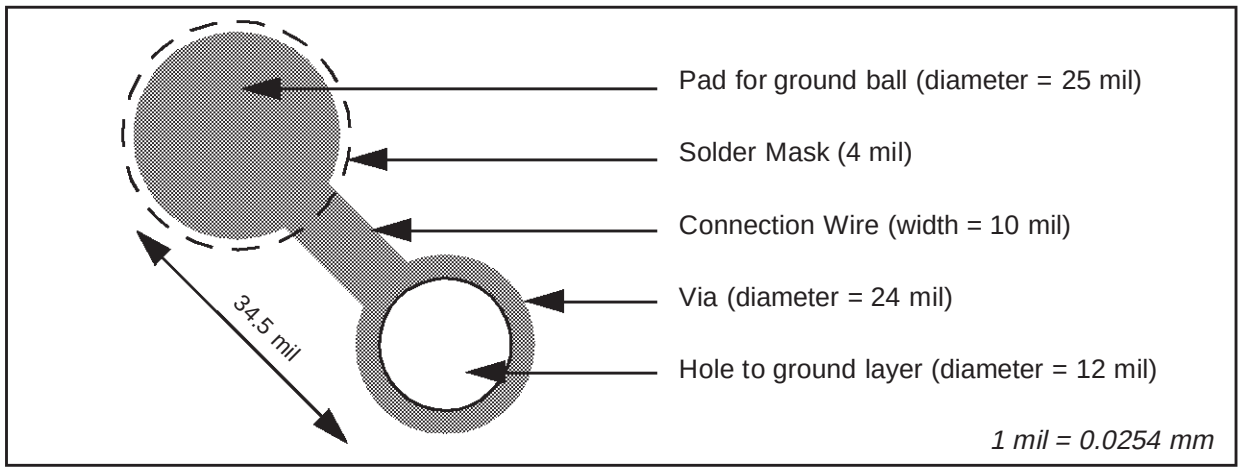


Figure 6-3. Recommended 4-wire ground pad layout

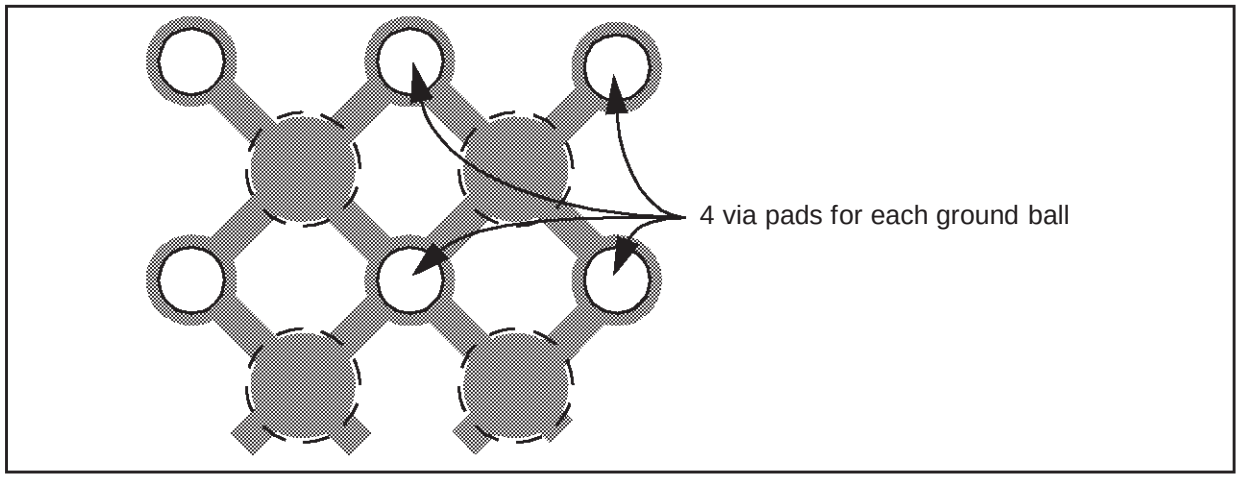
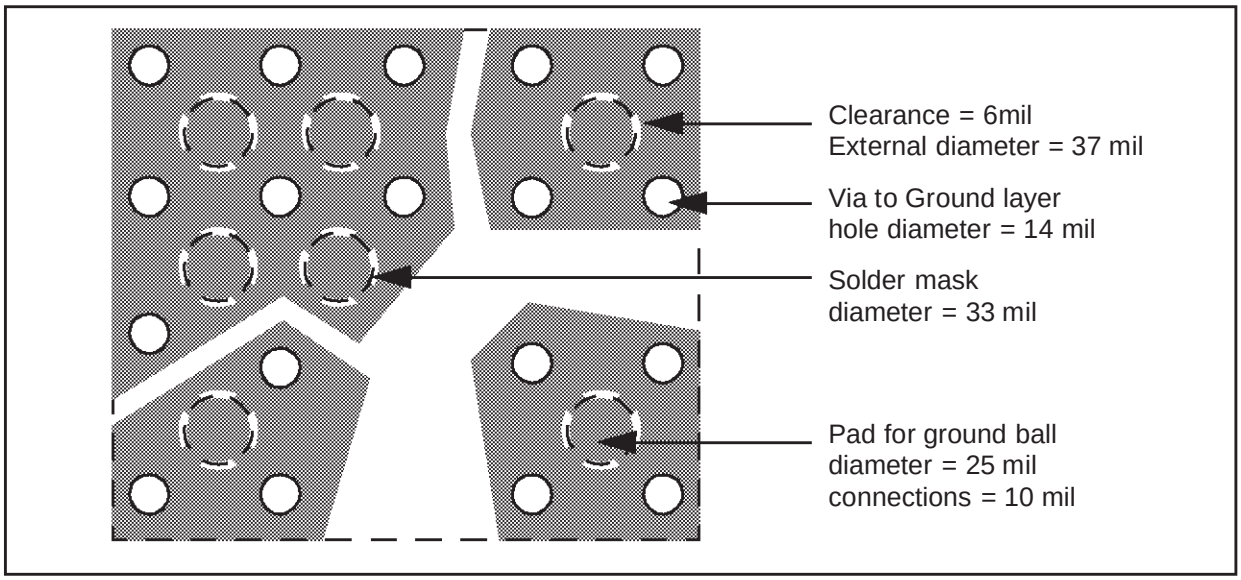


Figure 6-4. Optimum layout for central ground ball



The PBGA Package dissipates also through peripheral ground balls. When a heat sink is placed on the device, heat is more uniformely spread throughout the moulding increasing heat dissipation through the peripheral ground balls.

The more via pads are connected to each ground ball, the more heat is dissipated . The only limitation is the risk of lossing routing channels.

Figure 6-5 shows a routing with a good trade off between thermal dissipation and number of routing channels.

A local ground plane on opposite side of the board as shown in Figure 6-6 improves thermal dissipation. It is used to connect decoupling capacitances but can also be used for connection to a heat sink or to the system's metal box for better dissipation.

This possibility of using the whole system's box for thermal dissipation is very usefull in case of high temperature inside the system and low temperature outside. In that case, both sides of the PBGA should be thermally connected to the metal chassis in order to propagate the heat flow through the metal. Figure 6-7 illustrates such implementation.

6.2 High speed signals

Some Interfaces of the STPC run at high speed and have to be carefully routed or even shielded.

Here is the list of these interfaces, in decreasing speed order:

1) Memory Interface.

2) Graphics and video interfaces

3) PCI bus

4) 14MHz oscillator stage

All the clocks haves to be routed first and shielded for speeds of 27MHz or more. The high speed signals follow the same contrainsts, like the memory control signals and the PCI control signals.

The next interfaces to be routed are Memory, Video/graphics, and PCI.

All the analog noise sensitive signals have to be routed in a separate area and hence can be routed indepedently.

Figure 6-5. Global ground layout for good thermal dissipation

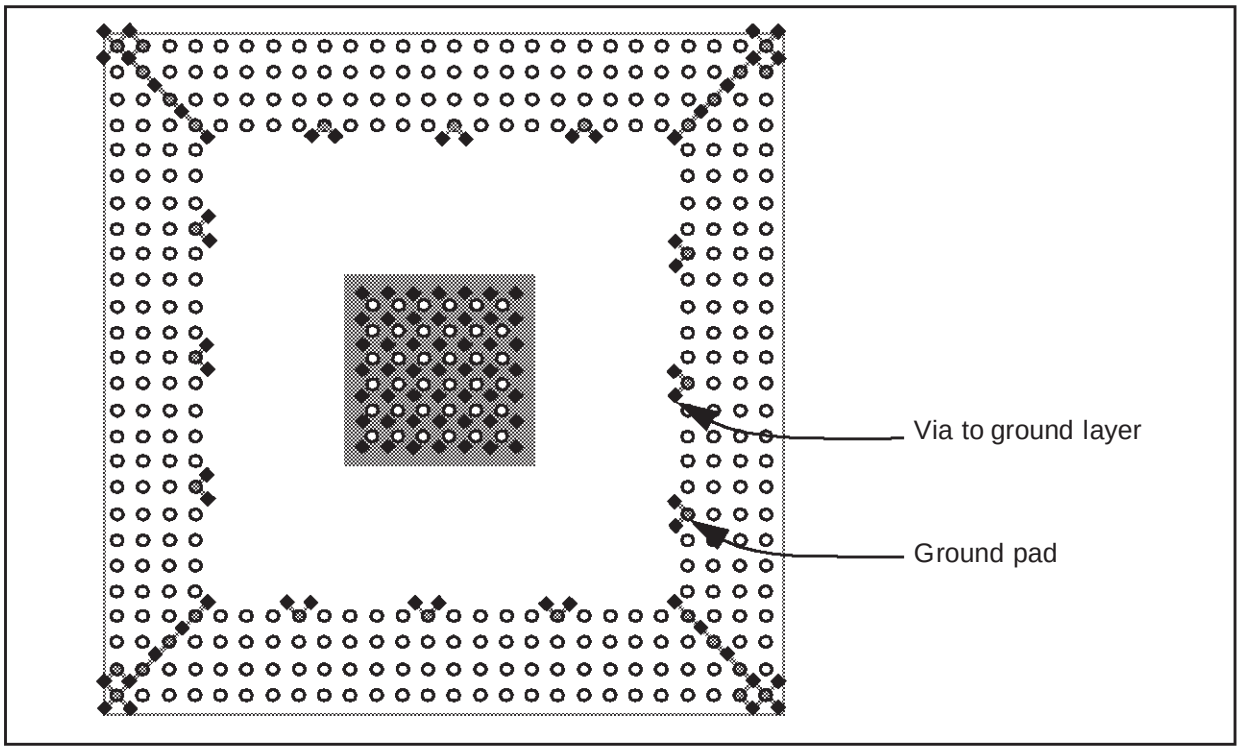


Figure 6-6. Bottom side layout and decoupling

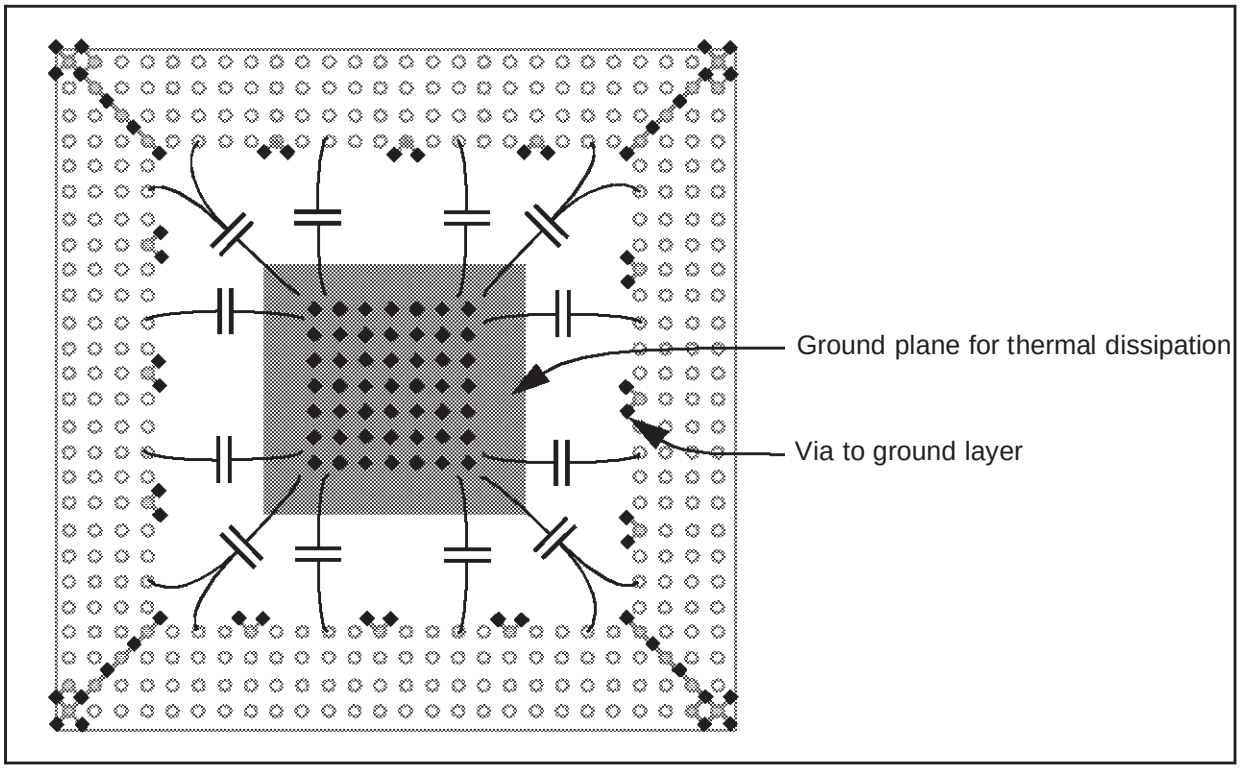


Figure 6-7. Use of metal plate for thermal dissipation

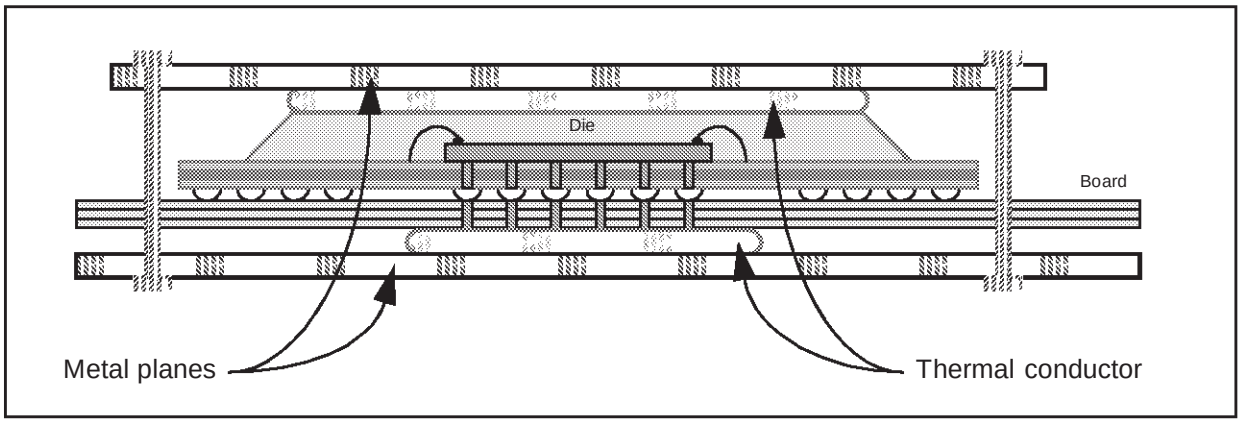
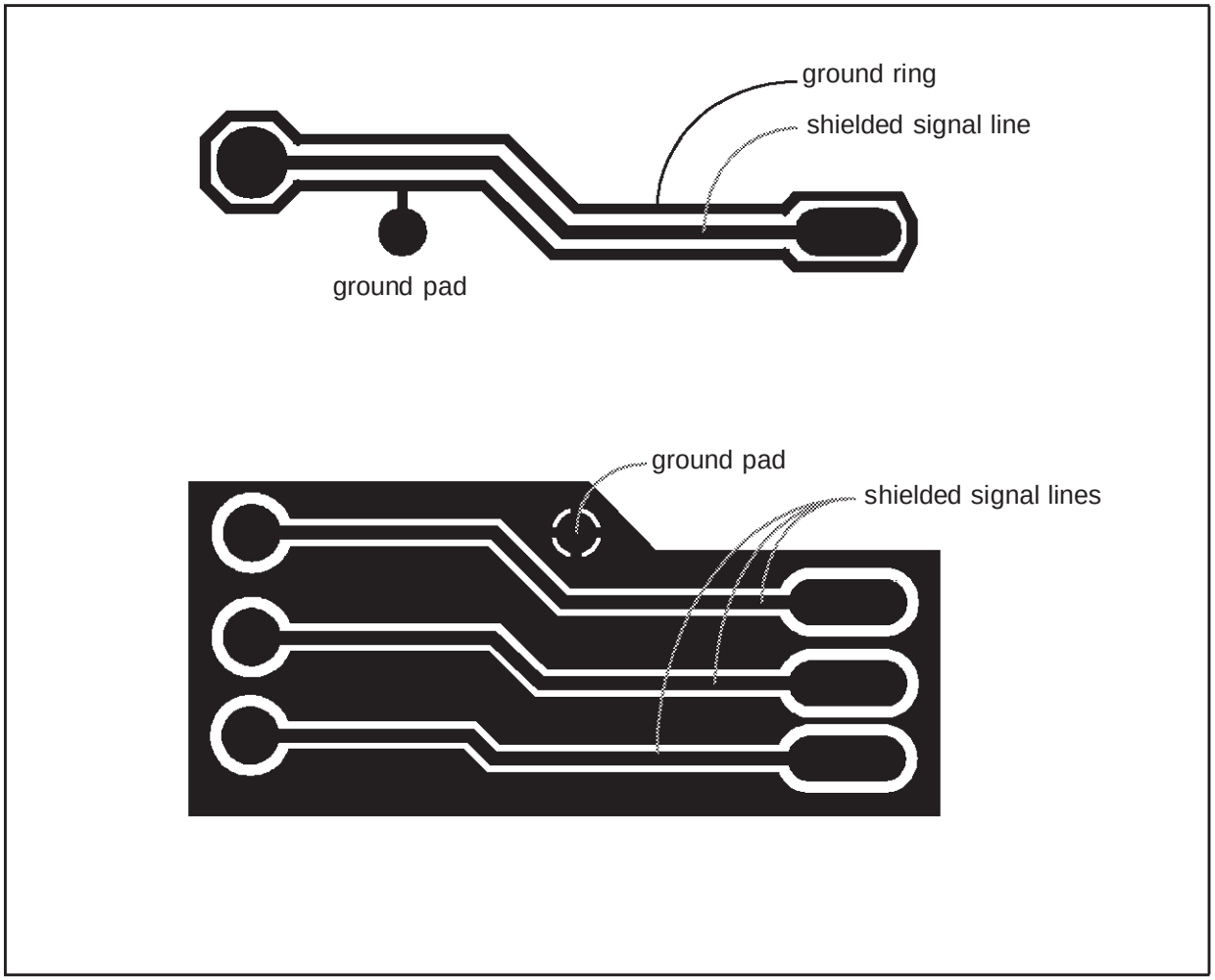


Figure 6-8. Shielding signals



6.3 Memory interface

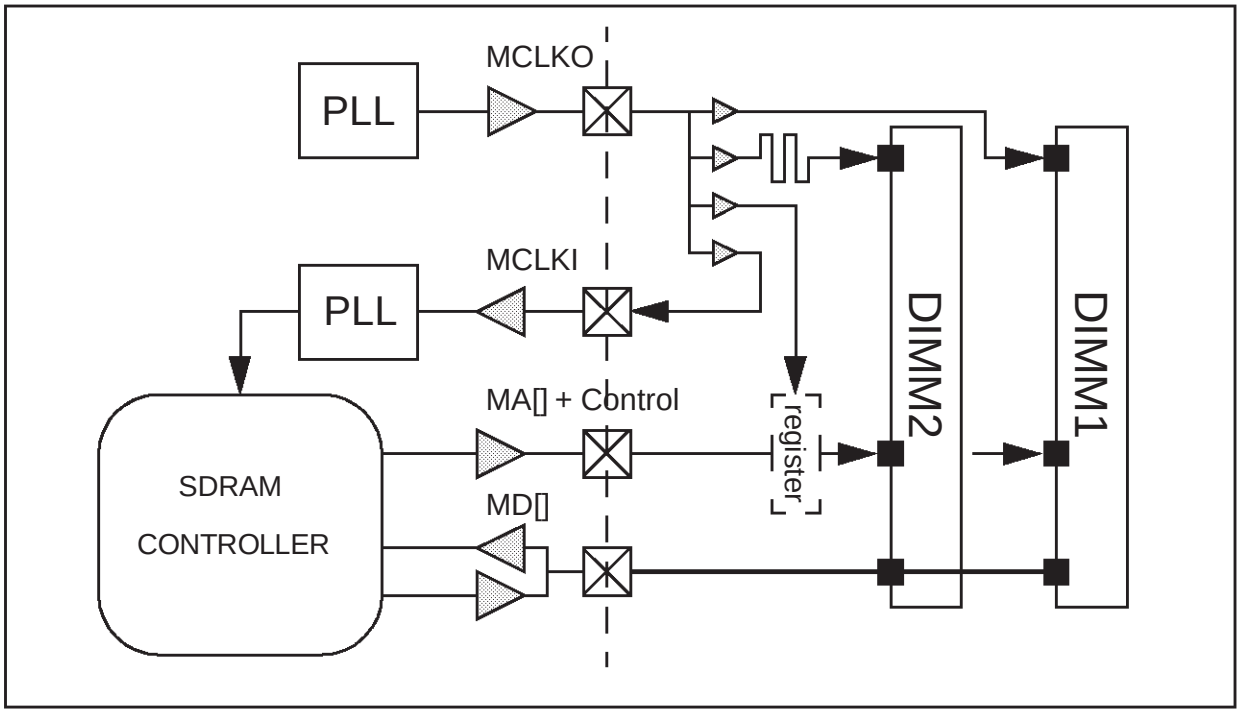
6.3.1 Introduction

In order to achieve SDRAM memory interfaces which work at clock frequencies of 100MHz and above, careful consideration has to be given to the timing of the interface with all the various electrical and physical constraints taken into consideration. The guidelines described below are related to SDRAM components on DIMM modules. For applications where the memories are directly soldered to the motherboard, the PCB should be laid out such that the trace lengths fit within the constraints shown here. The traces could be slightly longer since the extra routing on the DIMM PCB is no longer present but it is then up to the user to verify the timings.

6.3.2 SDRAM Clocking Scheme

The SDRAM Clocking Scheme deserves a special mention here. Basically the memory clock is generated on-chip through a PLL and goes directly to the MCLKO output pin of the STPC. The nominal frequency is 100MHz. Because of the high load presented to the MCLK on the board by the DIMMs it is recommeded to rebuffer the MCLKO signal on the board and balance the skew to the clock ports of the different DIMMs and the MCLKI input pin of STPC.

Figure 6-9. Clock scheme



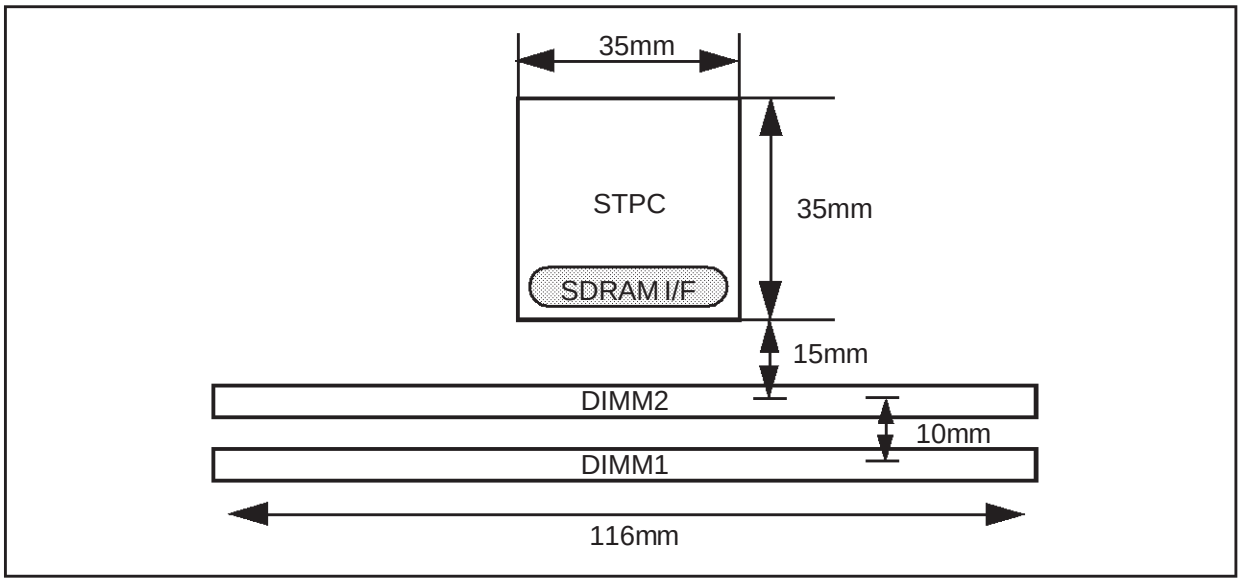
6.3.3 Board Layout Issues

The physical layout of the motherboard PCB assumed in this presentation is as shown inFigure 6-10. Because all the memory interface signal balls are located in the same region of the STPC device it is possible to orientate the device to reduce the trace lengths. The worst case routing length to the DIMM1 is estimated to be 100mm.

Solid power and ground planes are a must in order to provide good return paths for the signals and to reduce EMI and noise. Also there should be ample high frequency decoupling between the power and ground planes to provide a low impedance path between the planes for the return paths for signal routings which change layers. If possible the traces should be routed adjacent to the same power or ground plane for the length of the trace.

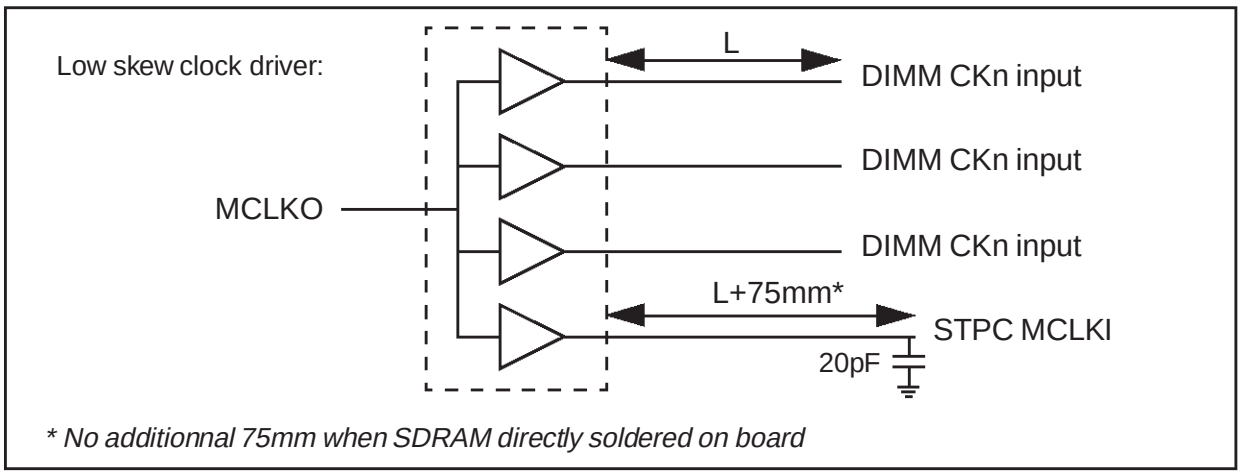
For the SDRAM interface the most critical signal is the clock. Any skew between the clocks at the SDRAM components and the memory controller will impact the timing budget. In order to get well matched clocks at all the components it is recommended that all the DIMM clock pins, STPC memory clock input (MCLKI) and any other component using the memory clock are individually driven

Figure 6-10. DIMM placement



from a low skew clock driver with matched routing lengths. This is shown in Figure 6-11.

Figure 6-11. Clock routing



The maximum skew between pins for this part is 250ps. The important factors for the clock buffer are a consistent drive strength and low skew between the outputs. The delay through the buffer is not important so it does not have to be a zero delay PLL type buffer. The trace lengths from the clock driver to the DIMM CKn pins should be matched exactly. Since the propagation speed can vary between PCB layers the clocks should be routed in a consistent way. The routing to the STPC memory input should be longer by 75mm to compensate for the extra clock routing on the DIMM. Also a 20pF capacitor should be placed as near as possible to the clock input of the STPC to compensate for the DIMM's higher clock load. The impedance of the trace used for the clock routing should be matched to the DIMM clock trace impedance (60-75 ohms). To minimise crosstalk the clocks should be routed with spacing to adjacent tracks of at least twice the clock trace width. For designs which use SDRAMs directly mounted on the motherboard PCB all the clock trace lengths should be matched exactly.

The DIMM sockets should be populated starting with the furthest DIMM from the STPC device first (DIMM1). There are 2 types of DIMM devices; single row and dual row. The dual row devices re-

quire 2 chip select signals to select between the two rows. A STPC device with 4 chip select control lines could control either 4 single row DIMMs or 2 dual row DIMMs.

When using DIMM modules, schematics have to be done carefully in order to avoid data busses completely crossed on the board. This has to be checked at the library level. In order to achive layout shown in Figure 6-12, schematics have to implement the crossing described on Figure 6-13. The DQM signals must be exchanged using the same order.

Figure 6-12. Optimum data bus layout for DIMM

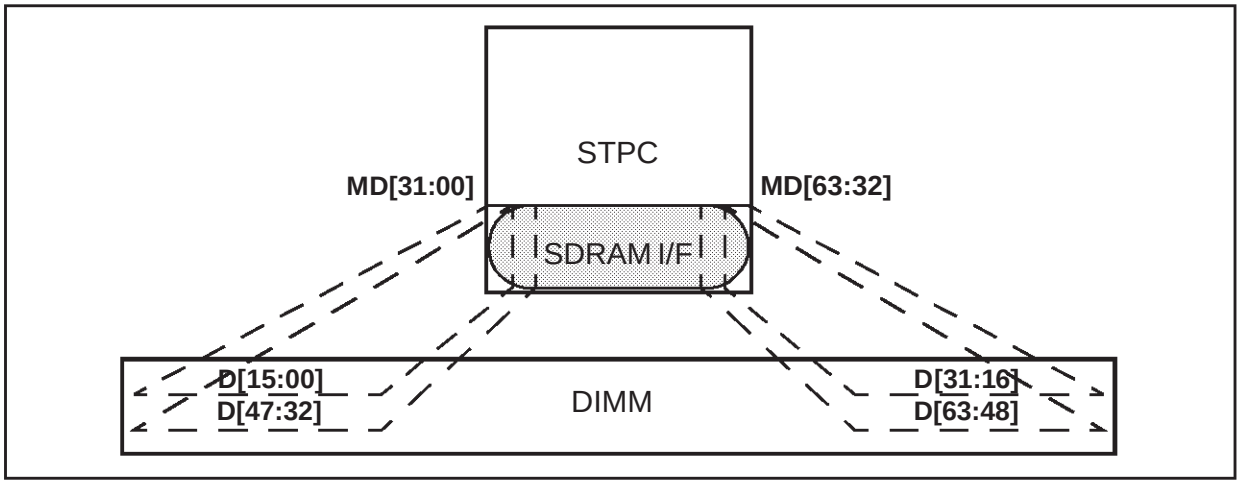
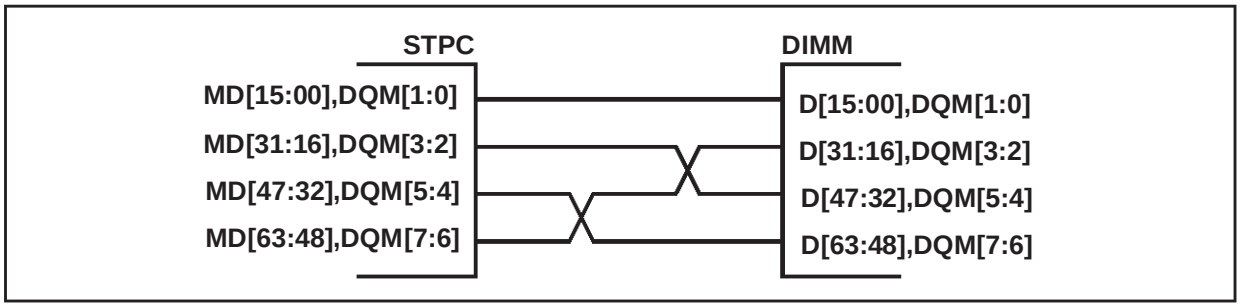


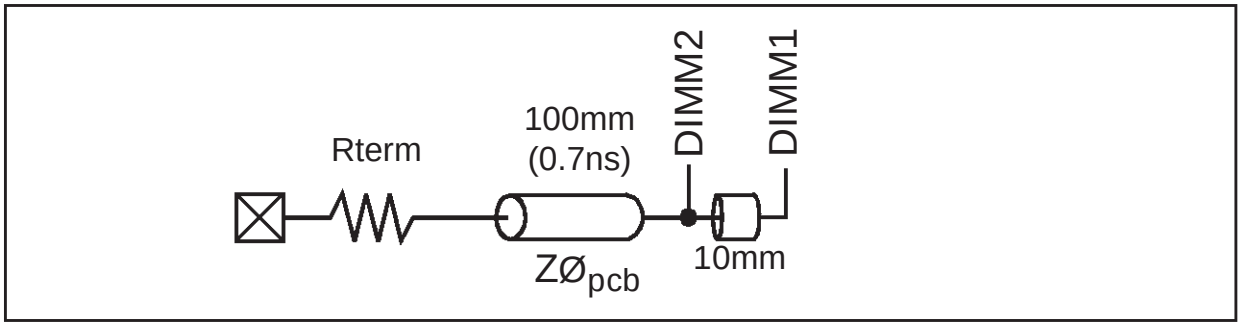
Figure 6-13. Schematics for optimum data bus layout for DIMM



6.3.4 Address & Control Signals

This group encompasses the memory address MA[10:0], bank address BA[0], RAS, CAS and write enable WE signals. The load of the DIMM module on these signals is the most important one and depends upon the type of SDRAM components used (x4, x8 or x16) and whether the DIMM module is single or dual row. The capacitive loading of the SDRAM inputs alone for an x8 single row DIMM will be about 30-40pF. An equivalent circuit for the timing simulation is shown inFigure 6-14 Most of the delays are due to the PCB traces and loading rather than the pad itself.

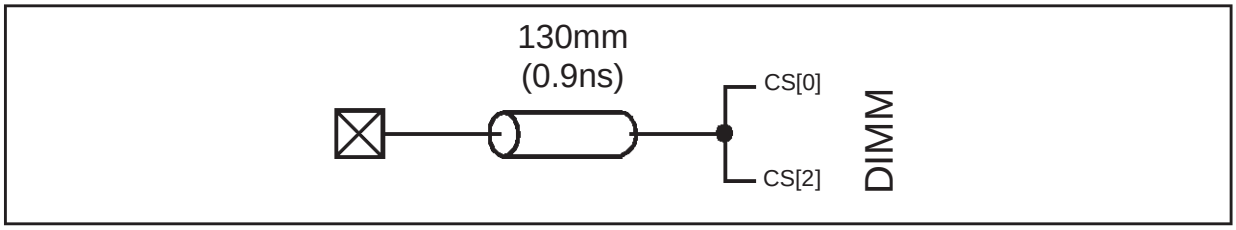
Figure 6-14. Address/control equivalent circuit



6.3.5 Chip Select Signals (CS#[3:0])

There are 4 chip select pins per DIMM. Chip selects 0 and 2 are always used to select the first row of SDRAMs and chip selects 1 and 3 select the second row on dual bank SDRAMs. The chip select outputs only have to drive one DIMM each

Figure 6-15. CS# equivalent circuit



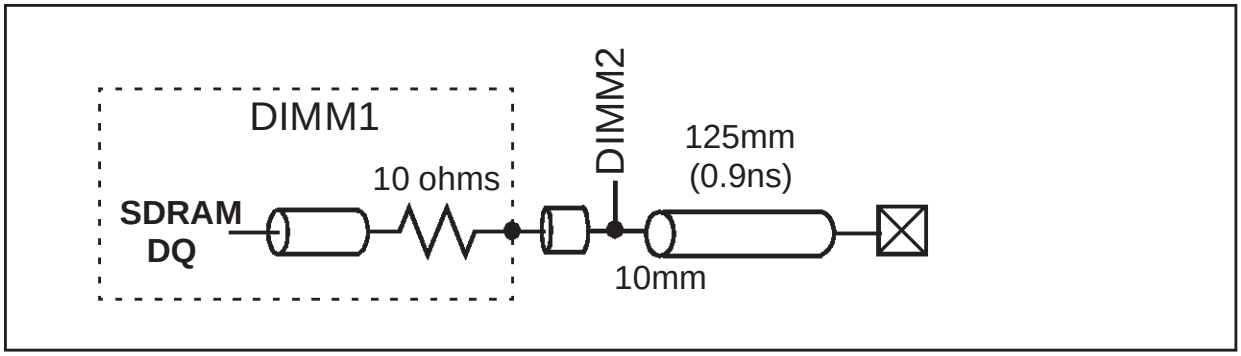
6.3.6 Data Write (MD[63:0])

The load on the data signals is much lower than the address/control signals for an unbuffered DIMM. For a registered DIMM the data signals are the only memory pins of the DIMM which are not registered. For the design to get maximum benefit from using registered DIMMs the timings should be compared to the timings for registered DIMMs for the other pins.

6.3.7 Data Read (MD[63:0])

The data read simulation circuit is shown below..

Figure 6-16. Data read equivalent circuit



6.3.8 Data Mask (DQM[7:0])

The data mask load is quite similar to that of the data signals.

6.3.9 Summary

For unbuffered DIMMs the address/control signals will be the most critical for timing. The simulations show that for these signals the best way to drive them is to use a parallel termination. For applications where speed is not so critical series termination can be used as this will save power. Using a low impedance such as 50Ω for these critical traces is recommended as it both reduces the delay and the overshoot.

The other memory interface signals will typically be not as critical as the address/control signals for unbuffered DIMMs. When using registered DIMMs the other signals will probably be just as critical as the address/control signals so to gain maximum benefit from using registered DIMMs the timings should also be considered in that situation. Using lower impedance traces is also beneficial for the other signals but if their timing is not as critical as the address/control signals they could use the default value. Using a lower impedance implies using wider traces which may have an impact on the routing of the board.

6.4 SDRAM LAYOUT EXAMPLES

The STPC provides MA, RAS#, CAS#, WE#, CS#, DQM#, BA0 (MA[11])and MD for SDRAM control. From 2 to 128 MBytes of main memory are supported in 1 to 4 banks. All Banks must be 64 bits wide.

The following memory devices are supported:

4Mbit x 4, 8Mbit x 2 & 16Mbit x 1 or if in the case of two internal bank chips, 2Mbit x 4 x 2, 4Mbit x 2 x 2 & 8Mbit x 1 x 2 .

The following Figure 6-17 and Figure 6-18, shows two possible SDRAM organizations based on one or two bank configurations.

Notes for Figure 6-17 and Figure 6-18;

All buffers must be low skew clock buffers

One clock driver can operate upto four memory chips.

All the clock lines must follow the rules below;

MCLKI = MCLK0 + MCLK0A

= .....

= MCLK0 + MCLK0D

= MCLK1 + MCLK1A

= .....

= MCLK1 + MCLK1D

This means that all line lengths must go from the buffer to the memory chips (MCLK1 or MCLK0 or ...) and from the buffer to the STPC (MCLKI) must be identical.

6.4.1 Host Address to MA bus Mapping

Graphics memory resides at the beginning of Bank 0. Host memory begins at the top of graphics memory and extends to the top of populated SDRAM.

The bank attributes can be retrieved from a lookup table to select the final SDRAM row and column address mappings. (Table 6-2). Also Table 6-1 shows the Standard DIMM Pinout for the users that wish to design with DIMMs.

.

Figure 6-17. One memory Bank with eight chips (8-Bit)

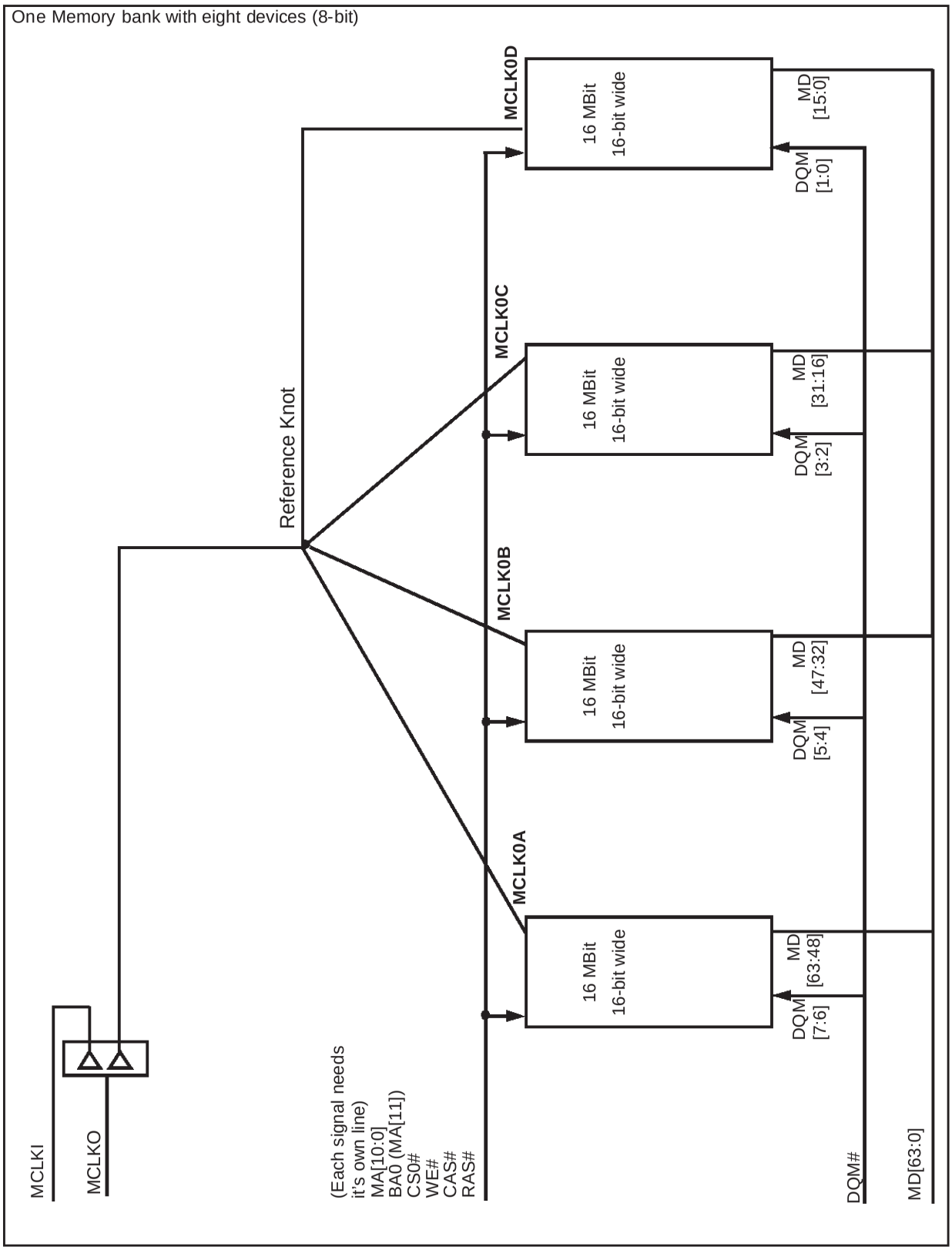


Figure 6-18. Two memory banks with eight chips on each (8-Bit)

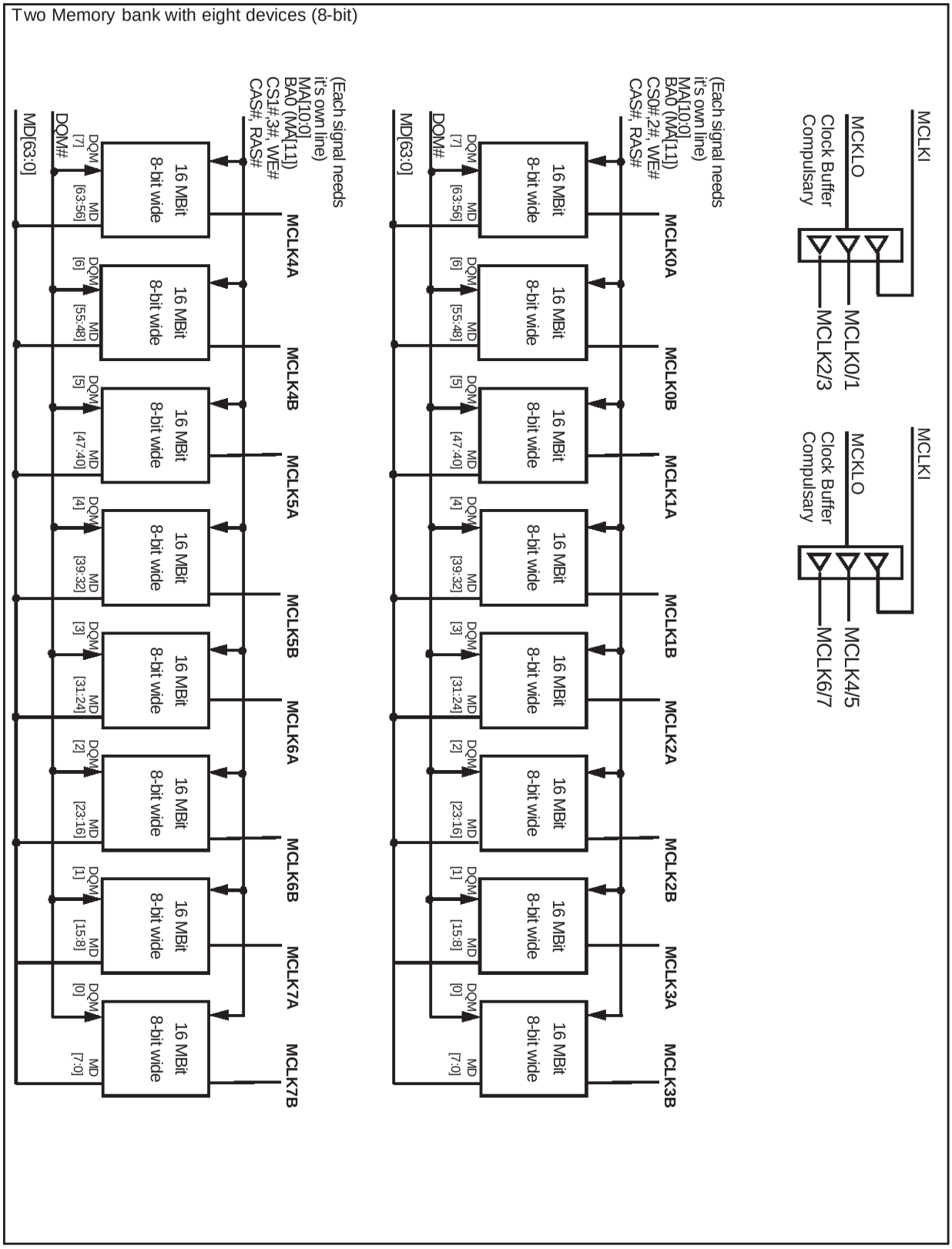


Table 6-1. Standard Memory DIMM Pinout

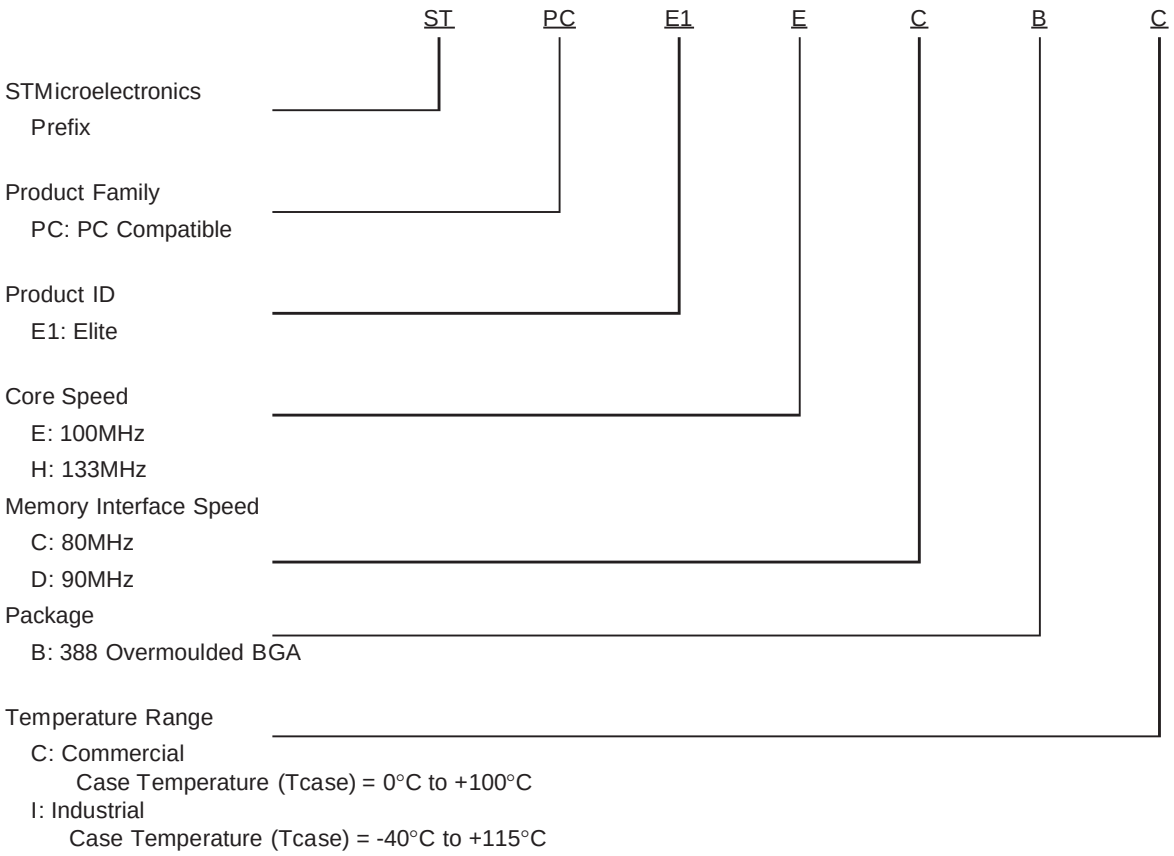
Memory Banks pin number	16Mbit(2 banks)
...	MA[10:0]
123	-
126	-
39	-
122	BA0(MA11)

Table 6-2. Address Mapping

Address Mapping: 16 Mbit - 2 banks												
STPC I/F	BA0(MA11)	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
RAS ADDRESS	A11	A22	A21	A2	A19	A18	A17	A16	A15	A14	A13	A12
CAS ADDRESS	A11	0	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3

7 ORDERING DATA

7.1 Ordering Codes



7.2 Available Part Numbers

Part Number	Core Frequency (MHz)	CPU Mode (X1 / X2)	Memory Interface Speed (MHz)	Tcase Range (°C)
STPCE1DDBC	90	X1	90	0°C to +100°
STPCE1EDBC	100	X1	90	
STPCE1HDC	133	X2	90	
STPCE1DDBI	90	X1	90	-40°C to +115°
STPCE1EDBI	100	X1	90	
STPCE1HDBI	133	X2	90	

7.3 Customer Service

More informations are available on STMicroelectronics internet site *http://www.st.com/stpc*