REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23										
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
97-05-21

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, MULTICHIP MICROCIRCUIT, MICROPROCESSOR WITH STATIC RAM, SILICON

SIZE	CAGE CODE	
A	67268	5962-97536

SHEET 1 OF 23

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5962-E188 -97

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited

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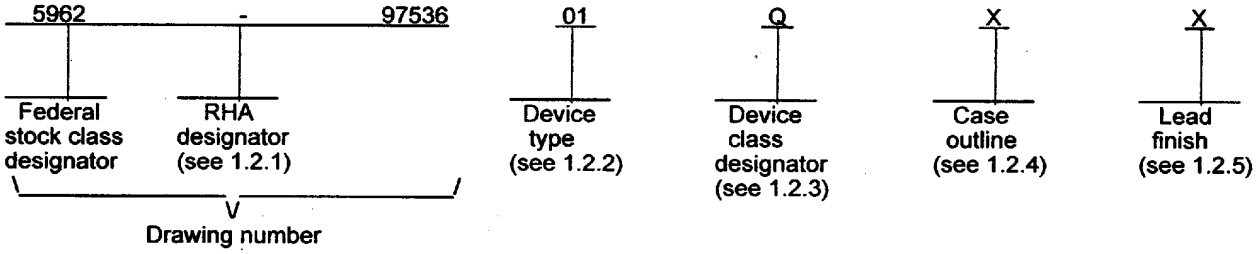
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Memory	Operating frequency	Circuit function
01	320MCM41	128K	40 MHz	Digital signal processor multichip module
02	320MCM41	128K	50 MHz	Digital signal processor multichip module

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	see figure 1	352	Ceramic Quad Flat Pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V dc to + 7.0 V dc 2/
Voltage range on any pin (V_{IN})	-0.3 V dc to + 7.0 V dc
Output voltage range (V_{OUT})	-0.3 V dc to + 7.0 V dc
Storage temperature range (T_{STG})	-65°C to + 150°C
Maximum allowed junction temperature (T_J)	150°C
Maximum solder temperature (10s duration)	260°C
Power dissipation (P_D)	5.2 W
Thermal impedance, Junction-to-case (Θ_{JC})	1.3°C/W

1.4 Recommended operating conditions. 2/

Supply voltage range (V_{CC})	+4.75 V ≤ V_{CC} ≤ +5.25 V
High level input voltage range (V_{IH}) 3/	
CLKIN, COMM	+2.6 V≤ V_{IH} ≤ V_{CC} + 0.3 V
$\overline{CSTRBx}$, $\overline{CRDYx}$, $\overline{CREQx}$, $\overline{CACKx}$	+2.2 V≤ V_{IH} ≤ V_{CC} + 0.3 V
All other pins	+2.0 V≤ V_{IH} ≤ V_{CC} + 0.3 V
Low level input voltage range (V_{IL})	-0.3 ≤ V_{IL} ≤ 0.8 V 3/
High level output current (I_{OH})	-300 µA
Low level output current (I_{OL})	2 mA
Case operating temperature range (T_C)	-55°C to 125°C
Maximum operating free-air temperature (T_A)	+125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.
MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values are with respect to V_{SS}.
3/ Maximum V_{IH} levels and minimum V_{IL} levels are characterized but not tested.
4/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The element evaluation for passive components shall be in accordance with MIL-PRF-38534 and as specified herein. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and Figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on Figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on Figure 3.

3.2.4 Boundry scan codes. The boundry scan codes shall be specified on Figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.75\ V \le V_{CC} \le +5.25\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
DC Electricals							
High-level output voltage 1/	V_{OH}	V_{CC} = MIN, I_{OH} = MAX	All	1,2,3	2.4		V
Low-level output voltage 1/	V_{OL}	V_{CC} = MIN, I_{OL} = MAX	All	1,2,3		0.6	V
Three-state current 1/2/	I_Z	$V_I = V_{SS}$ to V_{CC}	All	1,2,3	-20	20	µA
Input current 1/	I_I	$V_I = V_{SS}$ to V_{CC}	All	1,2,3	-10	10	µA
Input current, internal pullup 1/2/ 3/	I_{IPU}	$V_I = V_{SS}$ to V_{CC}	All	1,2,3	-400	30	µA
Input current, internal pulldown 1/2/ 3/ 4/	I_{IPD}	$V_I = V_{SS}$ to V_{CC}	All	1,2,3	-20	400	µA
Input current, CLKIN 1/2/	I_{IC}	$V_I = V_{SS}$ to V_{CC}	All	1,2,3	-50	50	µA
Supply current 1/	I_{CC}	V_{CC} = MAX	All	1, 2, 3		0.6	A
Input capacitance 5/	C_I	See 4.5.1c	All	4		40	pF
Output capacitance 5/	C_O	See 4.5.1c	All	4		40	pF
Functional testing		See 4.5.1b	All	7,8			
AC testing		6/	All	9,10,11			

1/ These parameters are guaranteed but not tested.
2/ Electrical characteristics are calculated algebraically from SMD 5962-94669 limits.
3/ Pins with internal pullup devices TDI, TDK, TMS.
4/ Applies to signal TRST.
5/ This paramater is guaranteed by simulation and not tested.
6/ Electrical parameters for the microprocessor die shall be per SMD 5962-94669. Electrical parameters for the SRAM die shall be per 5962-89598 with the following exceptions: I_{CC2} max = 40 mA, data retention test is not performed on the modules SRAM's. The placement of die into the module will not add more than 1 ns to the propagations delay limits, this limit will be gauranteed, but no tested.

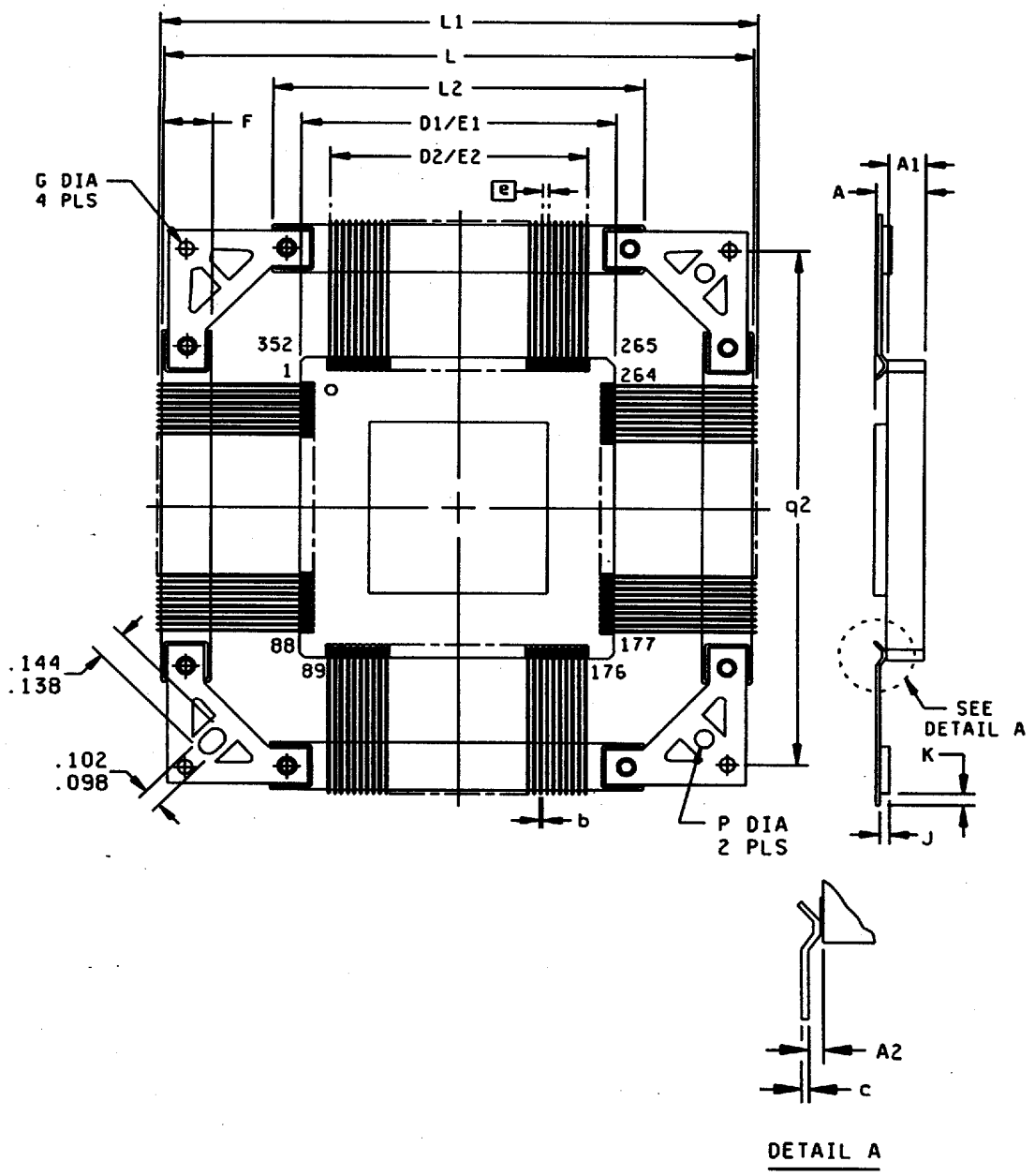


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216	SIZE **A**		**5962-97536**
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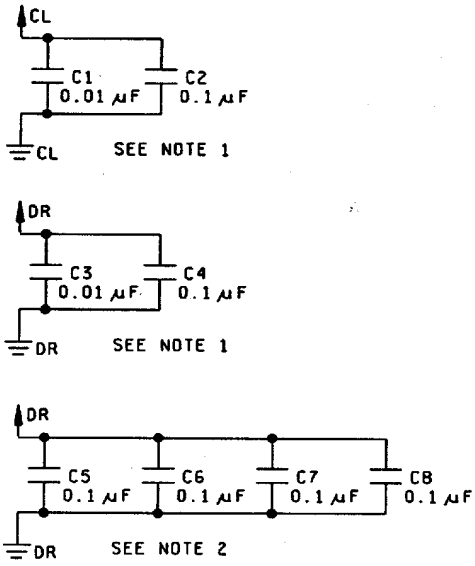
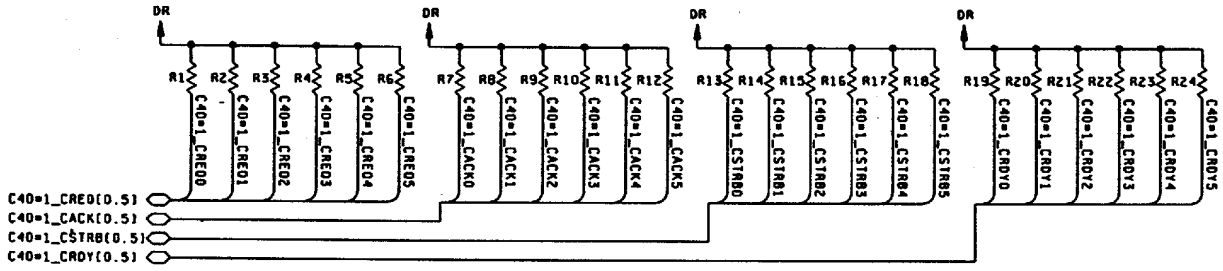
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.55		0.179
A1		4.00		0.157
A2	0.05	0.35	0.002	0.013
b2	0.18	0.25	0.007	0.010
c	0.10	0.20	0.004	0.008
D1/E1	47.52	48.48	1.870	1.908
D2/E2	43.50 BSC		1.712 BSC	
e		0.50		0.019
G	1.45	1.55	0.057	0.061
L	74.85	76.40	2.946	3.007
L1	74.60	75.40	2.937	2.968
L2	55.60	57.00	2.189	2.244
Q1		70.00		2.755
K		0.50		0.019
J	0.75	1.05	0.029	0.041
G	1.45	1.55	0.057	0.061
P	2.50	2.60	0.098	0.102

FIGURE 1. Case outline. - Continued





Notes:

1. Capacitors are physically located near the microprocessor die.
2. Capacitors are physically located near the SRAM die.

FIGURE 1. Case outline. - Continued

Case X

Terminal	Terminal symbol	Terminal	Terminal symbol	Terminal	Terminal symbol
1	D31	49	VDDL 4/	97	C5D2
2	D30	50	VSSL 5/	98	C5D1
3	D29	51	CE0	99	C5D0
4	D28	52	RDY0	100	DVDD 1/
5	D27	53	DE	101	C4D7
6	D26	54	TCK	102	C4D6
7	GDDVDD 1/	55	TDO	103	C4D5
8	D25	56	TDI	104	C4D4
9	D24	57	TMS	105	C4D3
10	D23	58	TRST	106	C4D2
11	D22	59	EMU0	107	C4D1
12	D21	60	EMU1	108	C4D0
13	D20	61	DVSS 3/	109	CVSS 2/
14	D19	62	DVSS 3/	110	DVSS 3/
15	D18	63	DVDD1/	111	DVSS 3/
16	D17	64	PAGE1	112	DVDD 1/
17	D16	65	R/W1	113	C3D7
18	CVSS 2/	66	STRB1	114	C3D6
19	CVSS 2/	67	STAT0	115	C3D5
20	IVSS 2/	68	STAT1	116	C3D4
21	GDDVDD 1/	69	IVSS2/	117	C3D3
22	GDDVDD 1/	70	STAT2	118	C3D2
23	DVSS 3/	71	STAT3	119	C3D1
24	DVSS 3/	72	PAGE0	120	C3D0
25	D15	73	R/W0	121	DVDD 1/
26	D14	74	STRB0	122	IVSS 2/
27	D13	75	AE	123	IVSS 2/
28	D12	76	RESETLOC1	124	C2D7
29	D11	77	DVDD 1/	125	C2D6
30	D10	78	RESETLOC0	126	C2D5
31	D9	79	RESET	127	C2D4
32	D8	80	CRDY5	128	C2D3
33	D7	81	CSTRB5	129	C2D2
34	D6	82	CACK5	130	C2D1
35	D5	83	CREQ5	131	C2D0
36	GDDVDD 1/	84	CRDY4	132	CVSS 2/
37	D4	85	CSTRB4	133	DVSS 3/
38	D3	86	CACK4	134	DVSS 3/
39	D2	87	CREQ4	135	DVDD 1/
40	D1	88	CVSS 2/	136	CRDY3
41	D0	89	DVSS 3/	137	CSTRB3
42	CE1	90	DVSS 3/	138	CACK3
43	RDY1	91	DVDD 1/	139	CREQ3
44	DVSS 3/	92	C5D7	140	VDDL 4/
45	DVSS 3/	93	C5D6	141	VSSL 5/
46	CVSS2/	94	C5D5	142	CRDY2
47	CVSS2/	95	C5D4	143	CSTRB2
48	LOCK	96	C5D3	144	CACK2

FIGURE 2. Terminal connections.

Case X

Terminal	Terminal symbol	Terminal	Terminal symbol	Terminal	Terminal symbol
145	CREQ2	193	NC	241	CVSS 2/
146	DVDD 1/	194	LR/W1	242	DVSS 3/
147	CRDY1	195	DVDD 1/	243	DVSS 3/
148	CSTRB1	196	CVSS 2/	244	NC
149	CACK1	197	NC	245	NC
150	CREQ1	198	NC	246	NC
151	CRDY0	199	NC	247	NC
152	XSTRB0	200	NC	248	NC
153	CACK0	201	TCLK0	249	NC
154	CREQ0	202	TCLK1	250	NC
155	CVSS 2/	203	H3	251	NC
156	CVSS 2/	204	H1	252	NC
157	DVSS 3/	205	NC	253	NC
158	DVSS 3/	206	IVSS 2/	254	NC
159	IVSS 2/	207	NC	255	NC
160	DVDD 1/	208	NC	256	LADVDD 1/
161	C1D7	209	NC	257	NC
162	C1D6	210	NC	258	NC
163	C1D5	211	NC	259	NC
164	C1D4	212	IACK	260	NC
165	C1D3	213	VDDL 4/	261	DVSS 3/
166	C1D2	214	VSSL 5/	262	DVSS 3/
167	C1D1	215	X1	263	CVSS 2/
168	C1D0	216	X2/CLKIN	264	NC
169	DVDD 1/	217	CVSS 2/	265	NC
170	C0D7	218	CVSS 2/	266	NC
171	C0D6	219	DVDD 1/	267	NC
172	C0D5	220	DVSS 3/	268	LDDVDD 1/
173	C0D4	221	DVSS 3/	269	NC
174	C0D3	222	NC	270	NC
175	C0D2	223	NC	271	NC
176	C0D1	224	NC	272	NC
177	C0D0	225	NC	273	NC
178	CVSS 2/	226	LADVDD 1/	274	NC
179	DVDD 1/	227	NC	275	NC
180	ROMEN	228	NC	276	NC
181	IIOF0	229	NC	277	NC
182	DVSS 3/	230	NC	278	NC
183	DVSS 3/	231	NC	279	NC
184	IIOF1	232	NC	280	LADVDD 1/
185	IIOF2	233	NC	281	LADVDD 1/
186	IIOF3	234	NC	282	CVSS 2/
187	NMI	235	NC	283	DVSS 3/
188	NC	236	NC	284	DVSS 3/
189	NC	237	NC	285	IVSS 2/
190	NC	238	LADVDD 1/	286	NC
191	NC	239	LADVDD 1/	287	NC
192	NC	240	CVSS 2/	288	NC

FIGURE 2. Terminal connections.

Case X

Terminal	Terminal symbol	Terminal	Terminal symbol
289		329	DVSS 3/
290	NC	330	DVSS 3/
291	NC	331	A16
292	NC	332	A15
293	NC	333	A14
294	NC	334	A13
295	NC	335	A12
296	NC	336	A11
297	NC	337	A10
298	NC	338	A9
299	LDDVDD 1/	339	A8
300	NC	340	A7
301	NC	341	A6
302	NC	342	A5
303	NC	343	A4
304	NC	344	GADVDD 1/
305	VDDL 4/	345	A3
306	VSSL 5/	346	A2
307	CVSS 2/	347	A1
308	CVSS 2/	348	A0
309	DVSS 3/	349	CVSS 2/
310	DVSS 3/	350	DVSS 3/
311	A30	351	DVSS 3/
312	A29	352	SUBS
313	A28		
314	GADVDD 1/		
315	A27		
316	A26		
317	A25		
318	A24		
319	A23		
320	A22		
321	A21		
322	A20		
323	A19		
324	A18		
325	A17		
326	GADVDD 1/		
327	GADVDD 1/		
328	CVSS 2/		
	CVSS 2/		

1/ CVSS and IVSS pins are connected internally
2/ DVDD, LADVDD, LDDVDD, GDDVDD, AND GADVDD pins are connected internally.
3/ DVSS pins are connected internally.
4/ VDDL pins are connected internally.
5/ VSSL pins are connected internally.

FIGURE 2. Terminal connections.

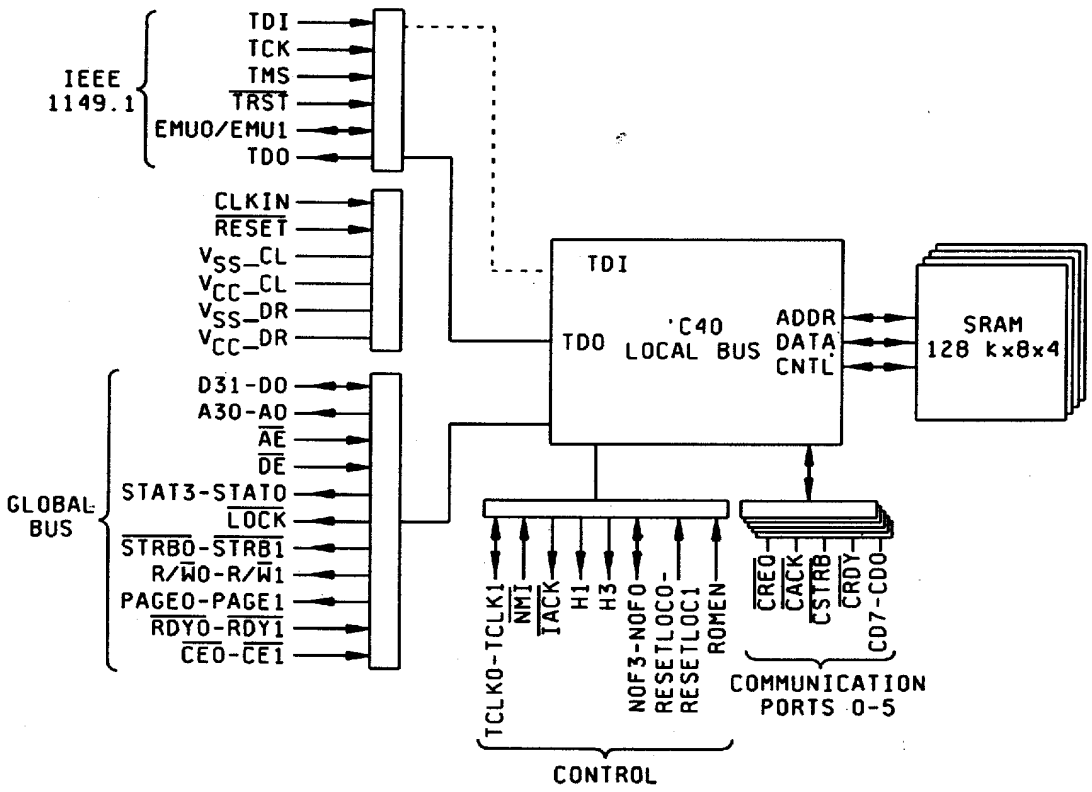
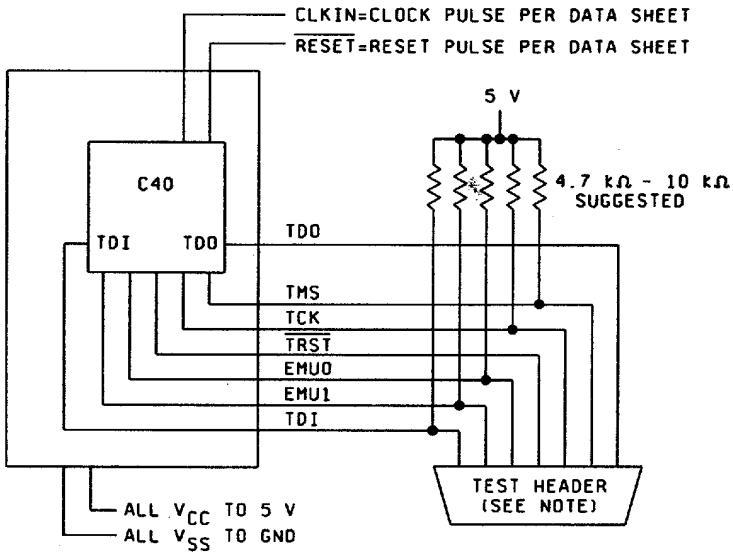


FIGURE 3. Block diagram.



Instruction code	Instruction name
00000000	EXTEST
11111111	BYPASS
00000010	SAMPLE
00000110	HIGHZ
00000011	PRIVATE1
00100000	PRIVATE2
00100001	PRIVATE3
00100010	PRIVATE4
00100011	PRIVATE5
00100100	PRIVATE6
00100101	PRIVATE7
00100110	PRIVATE8
00100111	PRIVATE9
00101000	PRIVATE10
00101001	PRIVATE11

FIGURE 4. Boundry scan instruction codes.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number H (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Element evaluation.

4.2.1 Microcircuit dice. Microcircuit dice shall be produced on a QML certified line and probed at wafer level according to the manufacturers QM plan.

4.2.2 Capacitors. Capacitor element evaluation shall be performed according to the manufacturer's QM plan.

4.2.3 Package evaluation. Packages shall be electrically tested by the package manufacturer. Element evaluation shall be performed according to the manufacturer's QM plan.

4.3 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. Constant acceleration shall be in accordance with MIL-PRF-38535 except the peak level shall be at test condition A (5000 g's). External ambient pressure shall not exceed 45 psi during screening.

4.3.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.3.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.4 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.5.1 through 4.5.4).

4.5 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.5.1 through 4.5.4).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters	---	---	1
Final electrical parameters	1, 2, 3, 4, 7, 8 1/	1, 2, 3, 7, 8 1/	1, 2, 3, 7, 8 1/
Group A test requirements	1, 2, 3, 4, 7, 8	1, 2, 3, 4, 7, 8	1, 2, 3, 4, 7, 8
Group C end-point electrical parameters	2, 8A	2, 8A	2, 7, 8
Group D end-point electrical parameters	2, 8A	2, 8A	2, 7, 8
Group E end-point electrical parameters	2, 8	2, 8	2, 7, 8

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.5.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_I and C_O measurements) shall be measured only for initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.5.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.5.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.5.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.5.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.5.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply CenterColumbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and as follows:

TABLE III. Pin descriptions.

Signal	Pins	Type 1/	Description
Global bus external interface (80 pins)			
D31-D0	32	I/O/Z	32-bit data port of the global external interface
$\overline{DE}$	1	I	Data bus enable signal for the global external interface
A30-A0	31	O/Z	31-bit address port of the global external interface
$\overline{AE}$	1	I	Address bus enable signal for the global bus interface
STAT3-STAT0	4	O	Status signals for the global bus interface
$\overline{LOCK}$	1	O	Lock signal for the global bus interface
$\overline{STRB0}$ 2/	1	O/Z	Access strobe 0 for the global bus interface
R/$\overline{W0}$ 2/	1	O/Z	Read/write signal for $\overline{STRB0}$ accesses
PAGE0 2/	1	O/Z	Page signal for $\overline{STRB0}$ accesses
$\overline{RDY0}$ 2/	1	I	Ready signal for $\overline{STRB0}$ accesses
$\overline{CE0}$ 2/	1	I	Control enable for the $\overline{STRB0}$, PAGE0, and R/$\overline{W0}$ signals
$\overline{STRB1}$ 2/	1	O/Z	Access strobe 1 for the global bus interface
R/$\overline{W1}$ 2/	1	O/Z	Read/write signal for $\overline{STRB1}$ accesses
PAGE1 2/	1	O/Z	Page signal for $\overline{STRB1}$ accesses
$\overline{RDY1}$ 2/	1	I	Ready signal for $\overline{STRB1}$ accesses
$\overline{CE1}$ 2/	1	I	Control enable for the $\overline{STRB1}$, PAGE1, and R/$\overline{W1}$ signals

TABLE III. Pin descriptions - Continued.

Signal	Pins	Type 1/	Description
Local bus external interface (80 pins)			
LD31-LD0	32	I/O/Z	32-bit data port of the local external interface
$\overline{\text{LDE}}$	1	I	Data bus enable signal for the local external interface
LA30-LA0	31	O/Z	31-bit address port of the local external interface
$\overline{\text{LAE}}$	1	I	Address bus enable signal for the local bus interface
LSTAT3-LSTAT0	4	O	Status signals for the local bus interface
$\overline{\text{LLOCK}}$	1	O	Lock signal for the local bus interface
$\overline{\text{LSTRB0}}$ 2/	1	O/Z	Access strobe 0 for the local bus interface
LR/$\overline{\text{W0}}$	1	O/Z	Read/write signal for $\overline{\text{LSTRB0}}$ accesses
LPAGE0	1	O/Z	Page signal for $\overline{\text{LSTRB0}}$ accesses
$\overline{\text{LRDY0}}$	1	I	Ready signal for $\overline{\text{LSTRB0}}$ accesses
$\overline{\text{LCE0}}$	1	I	Control enable for the $\overline{\text{LSTRB0}}$, LPAGE0, and LR/$\overline{\text{W0}}$ signals
$\overline{\text{LSTRB1}}$ 2/	1	O/Z	Access strobe 1 for the local bus interface
LR/$\overline{\text{W1}}$	1	O/Z	Read/write signal for $\overline{\text{LSTRB1}}$ accesses
LPAGE1	1	O/Z	Page signal for $\overline{\text{LSTRB1}}$ accesses
$\overline{\text{LRDY1}}$	1	I	Ready signal for $\overline{\text{LSTRB1}}$ accesses
$\overline{\text{LCE1}}$	1	I	Control enable for the $\overline{\text{LSTRB1}}$, LPAGE1, and LR/$\overline{\text{W1}}$ signals

TABLE III. Pin descriptions - Continued.

Signal	Pins	Type 1/	Description
Communication port 0 interface (12 pins)			
C0D7-C0D0	8	I/O	Communication port 0 data bus
$\overline{\text{CREQ0}}$	1	I/O	Communication port 0 token request signal
$\overline{\text{CACK0}}$	1	I/O	Communication port 0 token request acknowledge signal
$\overline{\text{CSTRB0}}$	1	I/O	Communication port 0 data strobe signal
$\overline{\text{CRDY0}}$	1	I/O	Communication port 0 data ready signal
Communication port 1 interface (12 Pins)			
C1D7-C1D0	8	I/O	Communication port 1 data bus
$\overline{\text{CREQ1}}$	1	I/O	Communication port 1 token request signal
$\overline{\text{CACK1}}$	1	I/O	Communication port 1 token request acknowledge signal
$\overline{\text{CSTRB1}}$	1	I/O	Communication port 1 data strobe signal
$\overline{\text{CRDY1}}$	1	I/O	Communication port 1 data ready signal
Communication port 2 interface (12 Pins)			
C2D7-C2D0	8	I/O	Communication port 2 data bus
$\overline{\text{CREQ2}}$	1	I/O	Communication port 2 token request signal
$\overline{\text{CACK2}}$	1	I/O	Communication port 2 token request acknowledge signal
$\overline{\text{CSTRB2}}$	1	I/O	Communication port 2 data strobe signal
$\overline{\text{CRDY2}}$	1	I/O	Communication port 2 data ready signal

TABLE III. Pin descriptions - Continued.

Signal	Pins	Type 1/	Description
Communication port 3 interface (12 pins)			
C3D7-C3D0	8	I/O	Communication port 3 data bus
$\overline{\text{CREQ3}}$	1	I/O	Communication port 3 token request signal
$\overline{\text{CACK3}}$	1	I/O	Communication port 3 token request acknowledge signal
$\overline{\text{CSTRB3}}$	1	I/O	Communication port 3 data strobe signal
$\overline{\text{CRDY3}}$	1	I/O	Communication port 3 data ready signal
Communication port 4 interface (12 Pins)			
C4D7-C4D0	8	I/O	Communication port 4 data bus
$\overline{\text{CREQ4}}$	1	I/O	Communication port 4 token request signal
$\overline{\text{CACK4}}$	1	I/O	Communication port 4 token request acknowledge signal
$\overline{\text{CSTRB4}}$	1	I/O	Communication port 4 data strobe signal
$\overline{\text{CRDY4}}$	1	I/O	Communication port 4 data ready signal
Communication port 5 interface (12 Pins)			
C5D7-C5D0	8	I/O	Communication port 5 data bus
$\overline{\text{CREQ5}}$	1	I/O	Communication port 5 token request signal
$\overline{\text{CACK5}}$	1	I/O	Communication port 5 token request acknowledge signal
$\overline{\text{CSTRB5}}$	1	I/O	Communication port 5 data strobe signal
$\overline{\text{CRDY5}}$	1	I/O	Communication port 5 data ready signal

TABLE III. Pin descriptions - Continued.

Signal	Pins	Type 1/	Description
Interrupts, I/O flags, RESET, timer (12 pins)			
IIOF3-IIOF0	4	I/O	Interrupt and I/O flags
$\overline{\text{NMI}}$	1	I	Nonmaskable interrupt. It is sensitive to a low-going edge.
$\overline{\text{IACK}}$	1	O	Interrupt acknowledge
$\overline{\text{RESET}}$	1	I	Reset signal
RESETLOC1- RESETLOC0	2	I	Reset-vector location pins
ROMEN	1	I	On-chip ROM enable (0 = disable, 1 = enable)
TCLK0	1	I/O	Timer 0 pin
TCLK1	1	I/O	Timer 1 pin
CLOCK (4 Pins)			
X1	1	O	Crystal pin
X2/CLKIN	1	I	Crystal/oscillator pin
H1	1	O	H1 clock
H3	1	O	H3 clock

TABLE III. Pin descriptions - Continued.

Signal	Pins	Type 1/	Description
Power (70 pins)			
CV_{SS}	15	I	Ground pins
DV_{SS}	15	I	Ground pins
IV_{SS}	6	I	Ground pins
DV_{DD}	13	I	+ 5-V_{DC} supply pins
$GADV_{DD}$	3	I	+ 5-V_{DC} supply pins
$GDDV_{DD}$	3	I	+ 5-V_{DC} supply pins
$LADV_{DD}$	3	I	+ 5-V_{DC} supply pins
$LDDV_{DD}$	3	I	+ 5-V_{DC} supply pins
SUBS	1	I	Substrate pin (tie to ground)
V_{DDL}	4	I	+ 5-V_{DC} supply pins
V_{SSL}	4	I	Ground pins
Emulation (7 pins)			
TCK	1	I	JTAG test port clock
TDO	1	O/Z	JTAG test port data out
TDI	1	I	JTAG test port data in
TMS	1	I	JTAG test port mode select
TRST	1	I	JTAG test port reset
EMU0	1	I/O	Emulation pin 0
EMU1	1	I/O	Emulation pin 1

1/ I = input, O = ouput, Z = high impedance.
2/ STRB0 and STRB1 and associated signals (R/$\overline{W}$1, R/$\overline{W}$0, PAGE0, PAGE1, etc.) are effective over the address ranges defined by the STRB ACTIVE bits.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-05-21

Approved sources of supply for SMD 5962-97536 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9753601QXC	01295	SMJ320MCM41DHFHM40
5962-9753602QXC	01295	SMJ320MCM41DHFHM50

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instrument, Incorporated 13500 North Central Expressway P.O. Box 655303 Dallas TX 75265 Point of contact: I-20 at FM 1788 Midland TX 79711-0448

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.