Features

- **Bipolar Speed in JEDEC Standard EPROM Pinout**
  - **Read Access Time - 55 ns**
  - **28-Lead 600 mil CERDIP and OTP Plastic DIP**
  - **32-Pad LCC and JLCC**
- **Low Power CMOS Operation**
  - **50 mA max. Active at 10 MHz**
- **High Output Drive Capability**
- **High Reliability Latch-Up Resistant CMOS Technology**
- **Rapid Programming - 100 µs/byte (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Industrial and Commercial Temperature Ranges**

256K (32K x 8) High Speed UV Erasable CMOS EPROM

Description

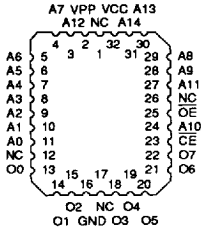
The AT27HC256R is a high-speed, low-power 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 32K x 8 bits. The AT27HC256R is suited for very high-speed applications, and requires only one 5 V power supply in normal read mode operation. Any byte can be accessed in less than 55 ns on the AT27HC256R, making this part ideal for high-performance systems. Power consumption is typically only 35 mA in Active Mode, and less than 15 mA in Standby Mode.

Atmel's high-speed CMOS technology provides optimum speed, lower power and high noise immunity. The high-speed CMOS process is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology.

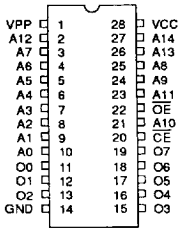
Pin Configurations

Pin Name	Function
A0-A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect
O0-O7	Outputs

LCC, JLCC
Top View



DIP
Top View



Description (Continued)

The AT27HC256R comes in a choice of industry standard JEDEC-approved packages including: 28-pin DIP ceramic, 32-pad ceramic leadless chip carrier (LCC), and 32-lead ceramic (JLCC). The device features two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

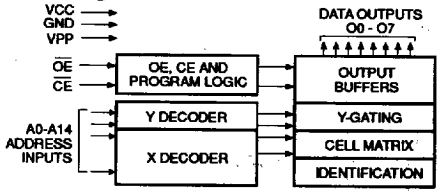
With a storage capacity of 32K bytes, Atmel's 27HC256R allows firmware to be stored reliably and to be accessed at very high speeds. The AT27HC256R has exceptional output drive capability — source 4 mA and sink 16 mA per output.

The AT27HC256R has additional features to ensure high-quality and efficient production use. The Rapid programming algorithm reduces the time required to program the chip and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27HC256R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm²

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify(2)	X	V_{IL}	Ai	V_{PP}	V_{CC}	D_{OUT}
Optional PGM Verify(2)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
PGM Inhibit(2)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A14 = V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5 V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27HC256R	
		-55	-70
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%

4

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC} + 1 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC} + 0.1 V			10	µA
I_{PP} [2]	V_{PP} [1] Read/Standby Current	V_{PP} = 3.8 to V_{CC}+0.3 V			20	µA
I_{SB}	V_{CC} [1] Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V			30	mA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC}+1.0 V			35	mA
I_{CC}	V_{CC} Active Current	f = 10 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}	Com.		50	mA
			Ind.,Mil.		55	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -2.5 mA		3.5		V
		I_{OH} = -4.0 mA		2.4		V
V_{PP}	V_{PP} Read Voltage	V_{CC} = 5 ± 0.5 V		3.8	V_{CC}+0.3	V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

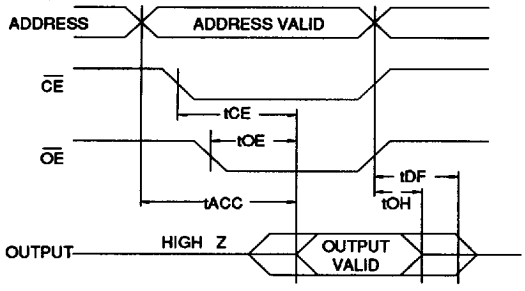
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27HC256R				
				-55		-70		
Symbol	Parameter	Condition		Min	Max	Min	Max	Units
t_{ACC} [4]	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.,Ind.		55		70	ns
			Mil.				70	ns
t_{CE} [3]	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			55		70	ns
t_{OE} [3,4]	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			25		30	ns
t_{DF} [2,5]	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$ = V_{IL}			25		30	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		0		0		ns

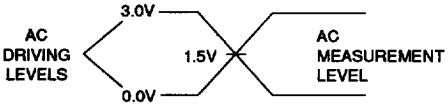
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation

A.C. Waveforms for Read Operation [1]



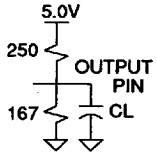
Notes:
1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.
   C_L = 30 pF, add 10 ns for C_L = 100 pF.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. t_{DF} is measured at V_{OH}-0.5 V or V_{OL}+0.5 V with C_L = 5 pF.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load



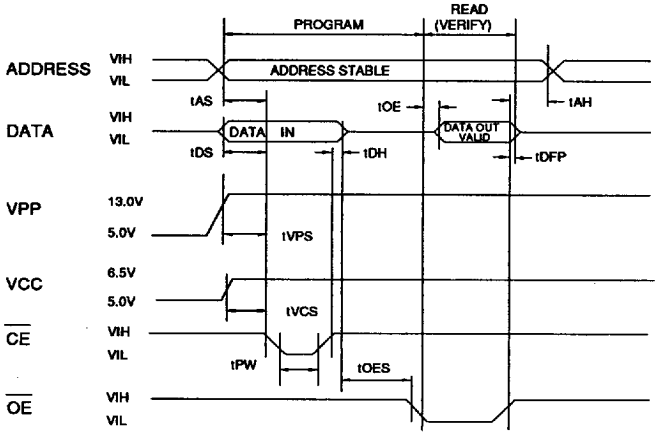
Note: C_L = 30 pF including jig capacitance.

Pin Capacitance (f = 1MHz, T= 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27HC256R a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL} = 16$ mA		.45	V
V_{OH}	Output High Volt.	$I_{OH} = -4.0$ mA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			60	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 5 ns
Input Pulse Levels ..... 0.0 V to 3.0 V
Input Timing Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V

Notes:

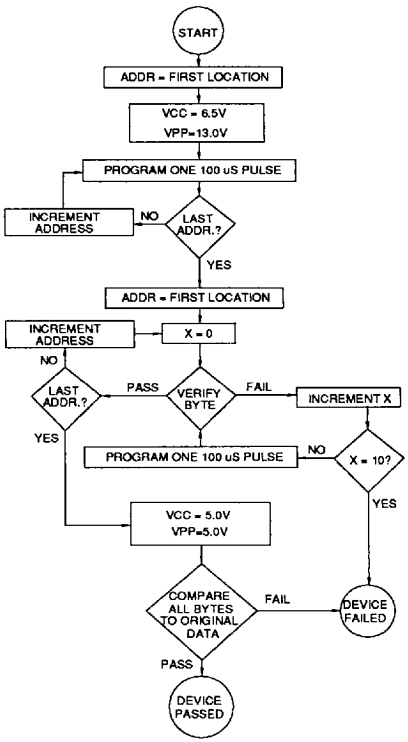
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ±5%.

Atmel's 27HC256R Integrated Product Identification Code

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	1	0	1	0	0	94

Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	50	30	AT27HC256R-55DC AT27HC256R-55KC AT27HC256R-55LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
55	55	30	AT27HC256R-55DI AT27HC256R-55KI AT27HC256R-55LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
70	50	30	AT27HC256R-70DC AT27HC256R-70KC AT27HC256R-70LC	28DW6 32KW 32LW	Commercial
70	55	30	AT27HC256R-70DI AT27HC256R-70KI AT27HC256R-70LI	28DW6 32KW 32LW	Industrial
			AT27HC256R-70DM AT27HC256R-70LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27HC256R-70DM/883 AT27HC256R-70LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	55	30	5962-86063 08 XX 5962-86063 08 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	55	30	AT27HC256R-70KM	32KW	Military (-55°C to 125°C)
			AT27HC256R-70KM	32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	55	30	5962-86063 08 ZX	32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)