

## 2-Mbit (128K x 16) Static RAM

### Features

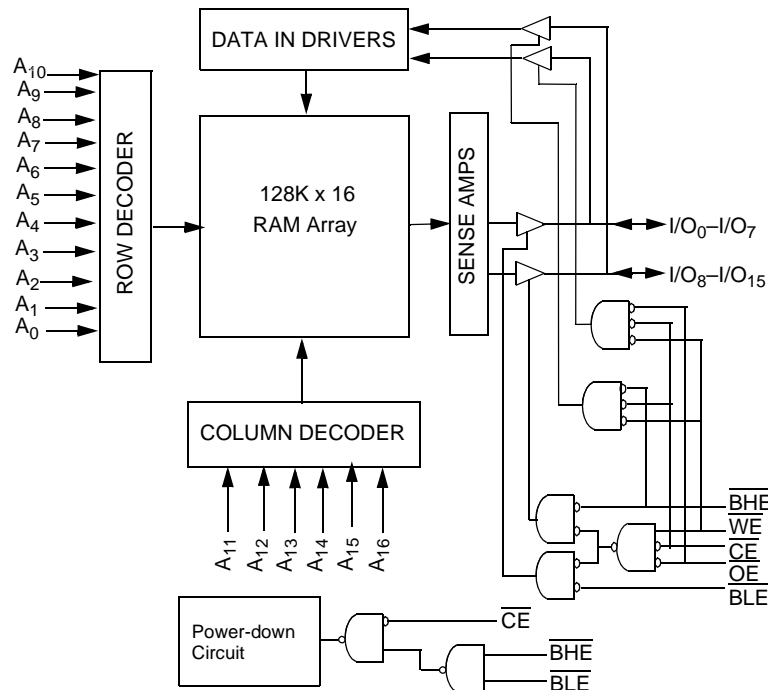
- **Temperature Ranges**
  - Industrial:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - Automotive-A:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - Automotive-E:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- **High Speed: 55 ns**
- **Wide voltage range: 2.7V–3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free 44-pin TSOP Type II package**

### Functional Description<sup>[1]</sup>

The CY62137VN is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in

portable applications such as cellular telephones. The device also has an automatic power-down feature that reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected (CE HIGH) or when CE is LOW and both BLE and BHE are HIGH. The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when deselected (CE HIGH), outputs are disabled (OE HIGH), BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE LOW, and WE LOW). Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

### Logic Block Diagram

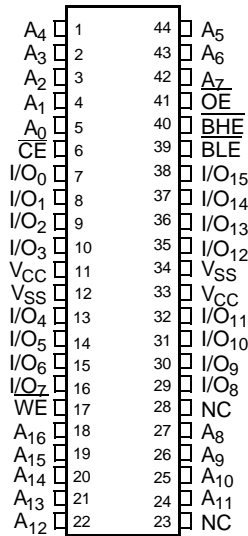


#### Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Product Portfolio**

Product		V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation			
						Operating, I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (μA)	
		Min.	Typ. <sup>[3]</sup>	Max.		Typ. <sup>[3]</sup>	Max.	Typ. <sup>[3]</sup>	Max.
CY62137VNLL	Industrial	2.7	3.0	3.6	55	7	20	1	15
CY62137VNLL					70	7	15	1	15
CY62137VNLL	Automotive-A				70	7	15	1	15
CY62137VNLL	Automotive-E				70	7	15	1	20

**Pin Configurations**
**TSOP II (Forward)  
Top View**

**Pin Definitions**

Pin Number	Type	Description
1–5, 18–22, 24–27, 42–45	Input	<b>A<sub>0</sub>–A<sub>16</sub></b> . Address Inputs
7–10, 13–16, 29–32, 35–38	Input/Output	<b>I/O<sub>0</sub>–I/O<sub>15</sub></b> . Data lines. Used as input or output lines depending on operation
23	No Connect	<b>NC</b> . This pin is not connected to the die
17	Input/Control	<b>WE</b> . When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
6	Input/Control	<b>CE</b> . When LOW, selects the chip. When HIGH, deselects the chip
40, 39	Input/Control	<b>Byte Write Select Inputs, active LOW</b> . <b>BHE</b> controls I/O <sub>15</sub> –I/O <sub>8</sub> , <b>BLE</b> controls I/O <sub>7</sub> –I/O <sub>0</sub> .
41	Input/Control	<b>OE</b> . Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins
12, 34	Ground	<b>V<sub>SS</sub></b> . Ground for the device
11, 33	Power Supply	<b>V<sub>CC</sub></b> . Power supply for the device

**Notes:**

- NC pins are not connected on the die.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(TYP)</sub>, T<sub>A</sub> = 25°C.



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage to Ground Potential ..... -0.5V to +4.6V
- DC Voltage Applied to Outputs in High-Z State<sup>[4]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V
- DC Input Voltage<sup>[4]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

- Output Current into Outputs (LOW) ..... 20 mA
- Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
- Latch-up Current..... > 200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	2.7V to 3.6V
Automotive-A	-40°C to +85°C	
Automotive-E	-40°C to +125°C	

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	-55			-70			Unit
			Min.	Typ. <sup>[3]</sup>	Max.	Min.	Typ. <sup>[3]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 2.7V, I <sub>OH</sub> = -1.0 mA	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 2.7V, I <sub>OL</sub> = 2.1 mA			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2		V <sub>CC</sub> + 0.5V	2.2		V <sub>CC</sub> + 0.5V	V
V <sub>IL</sub>	Input LOW Voltage		-0.5		0.8	-0.5		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , CMOS Levels	V <sub>CC</sub> = 3.6V	Ind'I	7	20	7	15	mA
				Auto-A/ Auto-E			7	15	
		I <sub>OUT</sub> = 0 mA, f = 1 MHz, CMOS Levels	Ind'I	1	2	1	2	mA	
			Auto-A/ Auto-E			1	2		
I <sub>SB1</sub>	Automatic CE Power-down Current—CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = f <sub>MAX</sub>	V <sub>CC</sub> = 3.6V	Ind'I		100		100	μA
				Auto-A/ Auto-E				100	
I <sub>SB2</sub>	Automatic CE Power-down Current—CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	V <sub>CC</sub> = 3.6V	Ind'I/	1	15	1	15	μA
				Auto-A			1	15	
				Auto-E			1	20	

**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

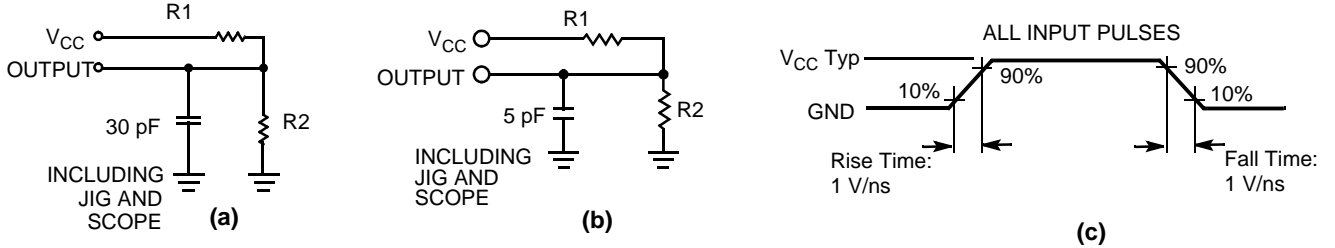
**Thermal Resistance<sup>[5]</sup>**

Parameter	Description	Test Conditions	TSOPII	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 2-layer printed circuit board	60	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		22	°C/W

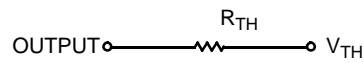
**Notes:**

- 4. V<sub>IL</sub>(min.) = -2.0V for pulse durations less than 20 ns.
- 5. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**



Equivalent to: THÉVENIN EQUIVALENT

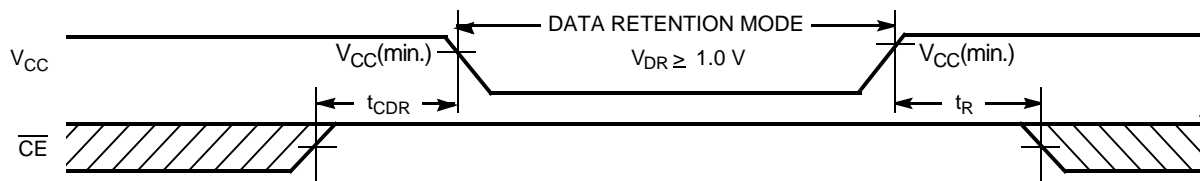


Parameters	Value	Unit
R1	1105	Ohms
R2	1550	Ohms
$R_{TH}$	645	Ohms
$V_{TH}$	1.75	Volts

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions	Min.	Typ. <sup>[3]</sup>	Max.	Unit	
$V_{DR}$	$V_{CC}$ for Data Retention		1.0			V	
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.0V, \overline{CE} \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V;$ No input may exceed $V_{CC} + 0.3V$	Ind/I/Auto-A		0.5	7.5	$\mu A$
			Auto-E			10	
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0			ns	
$t_R$	Operation Recovery Time		$t_{RC}$			ns	

**Data Retention Waveform**



**Switching Characteristics** Over the Operating Range <sup>[6]</sup>

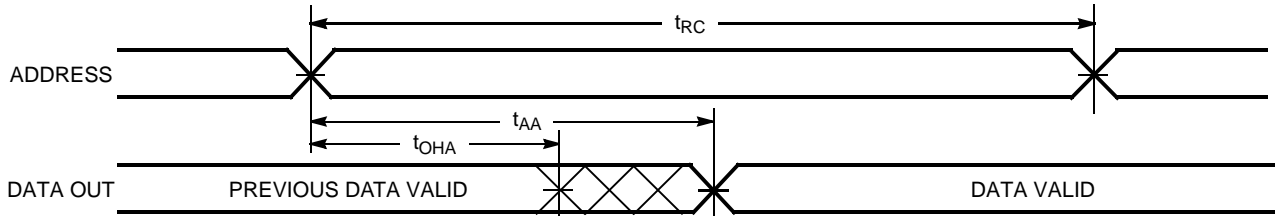
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{RC}$	Read Cycle Time	55		70		ns
$t_{AA}$	Address to Data Valid		55		70	ns
$t_{OHA}$	Data Hold from Address Change	10		10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		55		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z <sup>[7]</sup>	5		5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[7, 8]</sup>		25		25	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low-Z <sup>[7]</sup>	10		10		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High-Z <sup>[7, 8]</sup>		25		25	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-up	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-down		55		70	ns
$t_{DBE}$	$\overline{BHE}$ / $\overline{BLE}$ LOW to Data Valid		55		70	ns
$t_{LZBE}$ <sup>(9)</sup>	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low-Z	5		5		ns
$t_{HZBE}$	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High-Z		25		25	ns
<b>Write Cycle<sup>[10, 11]</sup></b>						
$t_{WC}$	Write Cycle Time	55		70		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	45		60		ns
$t_{AW}$	Address Set-up to Write End	45		60		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	40		50		ns
$t_{SD}$	Data Set-up to Write End	25		30		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[7, 8]</sup>		20		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[7]</sup>	5		10		ns
$t_{BW}$	$\overline{BHE}$ / $\overline{BLE}$ LOW to End of Write	50		60		ns

**Notes:**

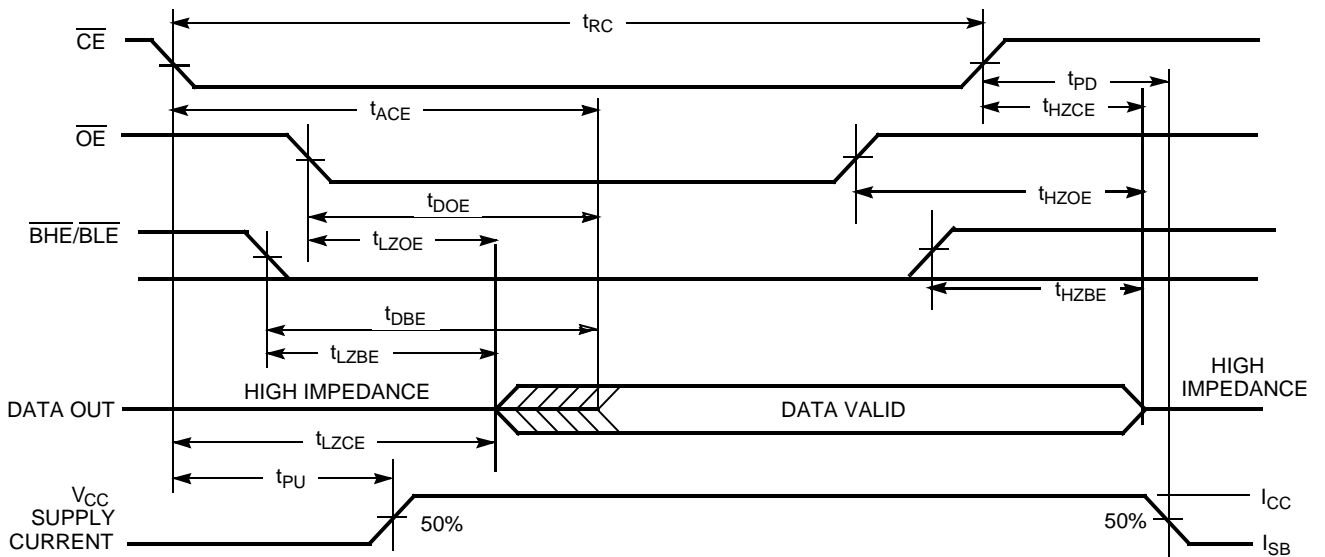
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to  $V_{CC}$  typ., and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
7. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
8.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
9. If both byte enables are toggled together this value is 10 ns.
10. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

### Switching Waveforms

#### Read Cycle No. 1<sup>[12, 13]</sup>



#### Read Cycle No. 2<sup>[13, 14]</sup>

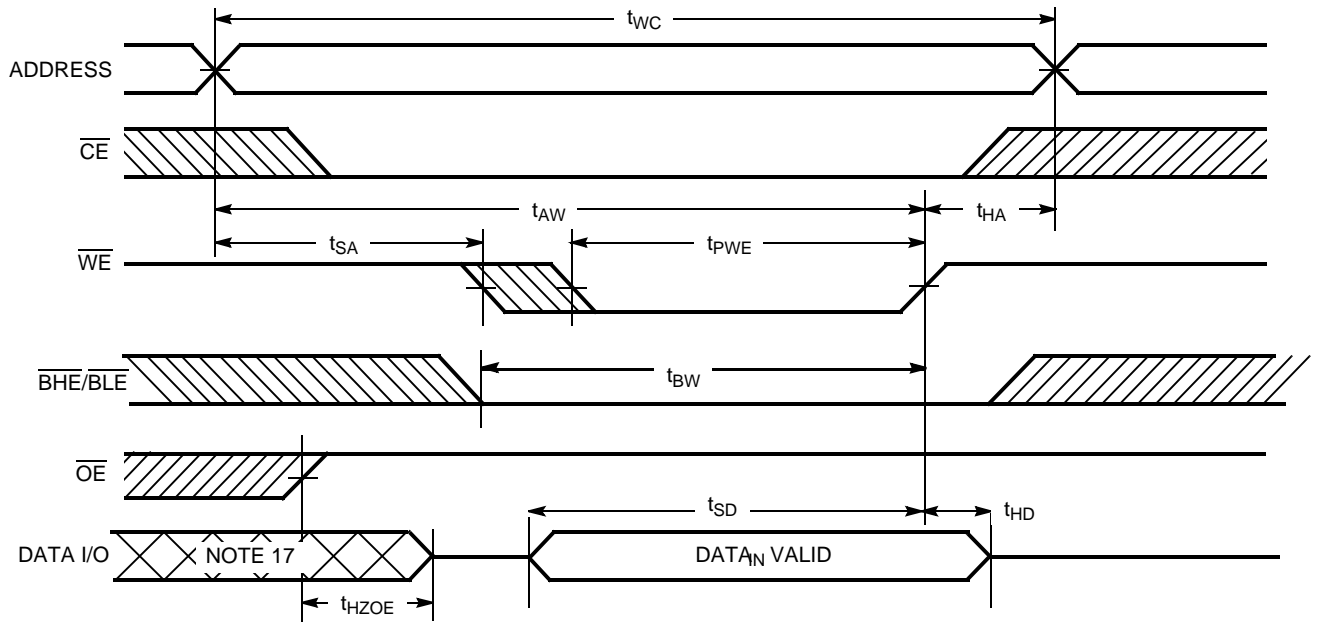


#### Notes:

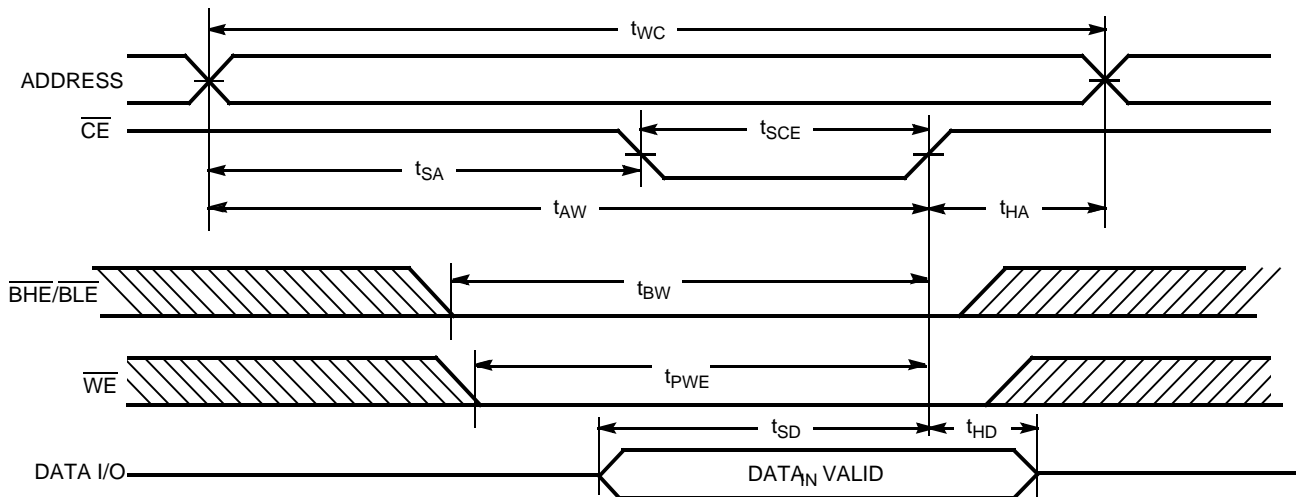
12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
13.  $\overline{WE}$  is HIGH for read cycle.
14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms** (continued)

**Write Cycle No. 1 (WE Controlled)**<sup>[10, 15, 16]</sup>



**Write Cycle No. 2 (CE Controlled)**<sup>[10, 15, 16]</sup>

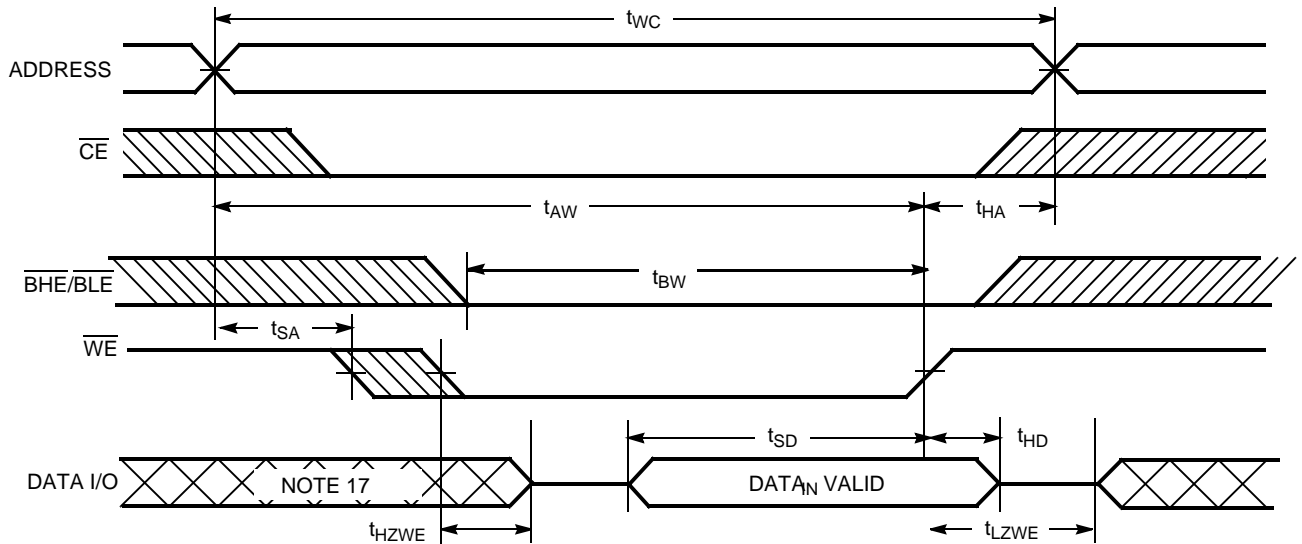


**Notes:**

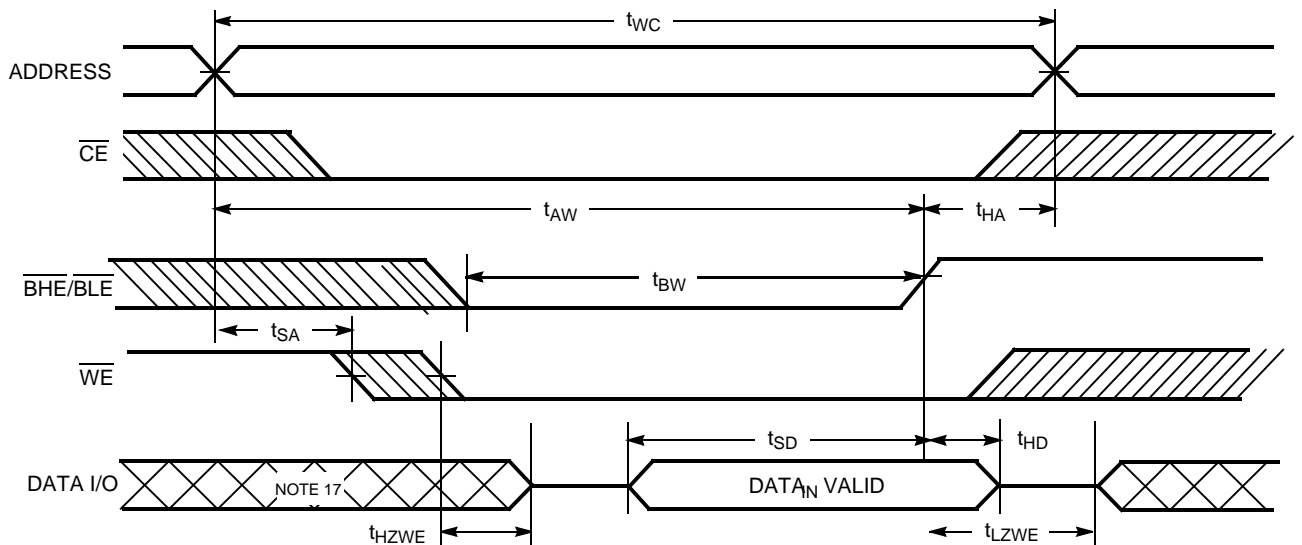
- 15. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
- 16. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
- 17. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms** (continued)

**Write Cycle No. 3 (WE Controlled, OE LOW)<sup>[11, 16]</sup>**

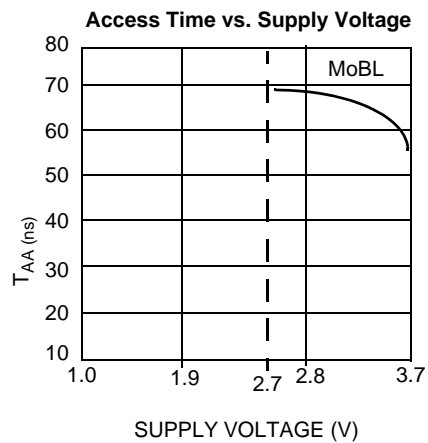
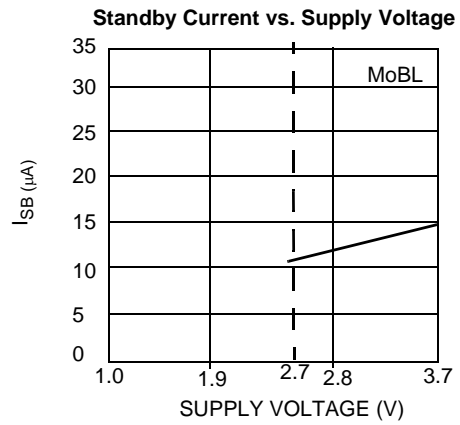
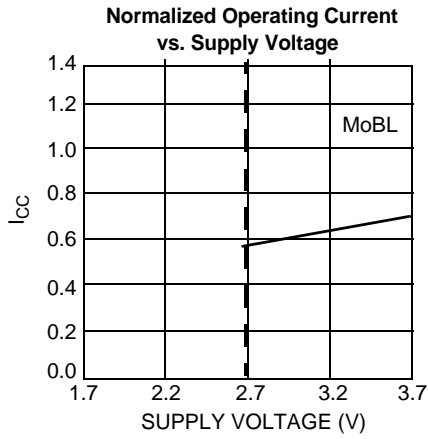


**Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW)<sup>[17]</sup>**





Typical DC and AC Characteristics



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	$I/O_8-I/O_{15}$	$I/O_0-I/O_7$	Mode	Power
H	X	X	X	X	High-Z	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X	X	X	H	H	High-Z	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out	Data Out	Read	Active ( $I_{CC}$ )
L	H	L	H	L	High-Z	Data Out	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out	High-Z	Read	Active ( $I_{CC}$ )
L	H	H	X	X	High-Z	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In	Data In	Write	Active ( $I_{CC}$ )
L	L	X	H	L	High-Z	Data In	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In	High-Z	Write	Active ( $I_{CC}$ )

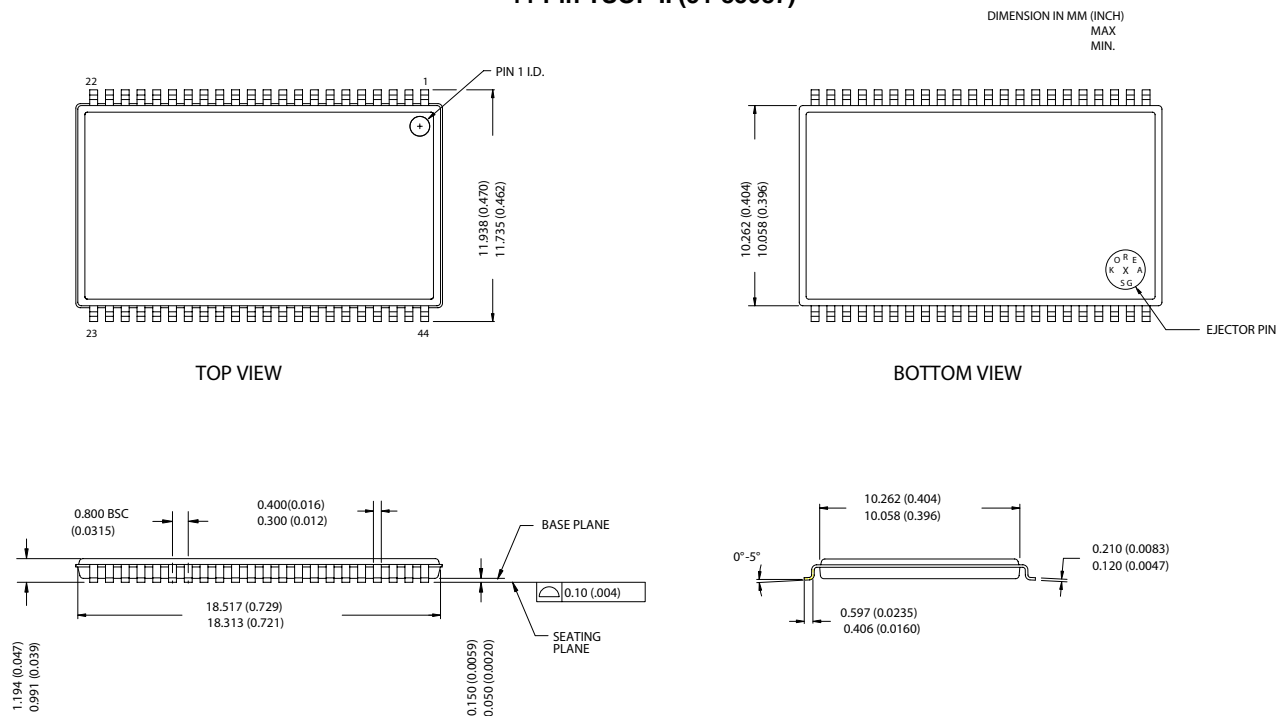
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62137VNLL-55ZXI	51-85087	44-pin TSOP II (Pb-free)	Industrial
70	CY62137VNLL-70ZXI		44-pin TSOP II (Pb-free)	Industrial
	CY62137VNLL-70ZSXA		44-pin TSOP II (Pb-free)	Automotive-A
	CY62137VNLL-70ZSXE		44-pin TSOP II (Pb-free)	Automotive-E

Please contact your local Cypress sales representative for availability of these parts

**Package Diagram**

**44-Pin TSOP II (51-85087)**



51-85087-A

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**Document History Page**

<b>Document Title: CY62137VN MoBL<sup>®</sup> 2-Mbit (128K x 16) Static RAM</b>				
<b>Document Number: 001-06497</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	426503	See ECN	NXR	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Updated Ordering Information table