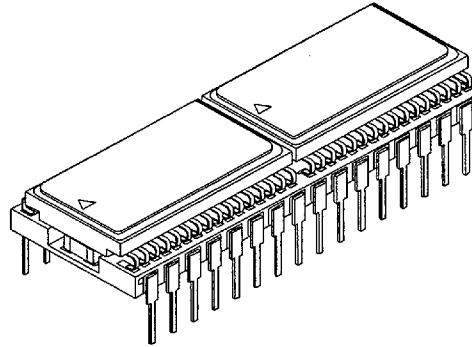


**DESCRIPTION:**

The DPS256S8BN is a high speed military 256K x 8 high-density, static RAM module comprised of two high speed ceramic 128K x 8 monolithic SRAM's, an advanced high-speed CMOS decoder and decoupling capacitors surface mounted on a co-fired ceramic substrate having side-brazed leads.

The DPS256S8BN is available in a 1.677 inch long, 600-mil-wide, 32-pin dual-in-line package that conforms to the same JEDEC standard pin configuration as the future four megabit monolithics.

The DPS256S8BN operates from a single +5V supply and all input and output pins are completely TTL-compatible.

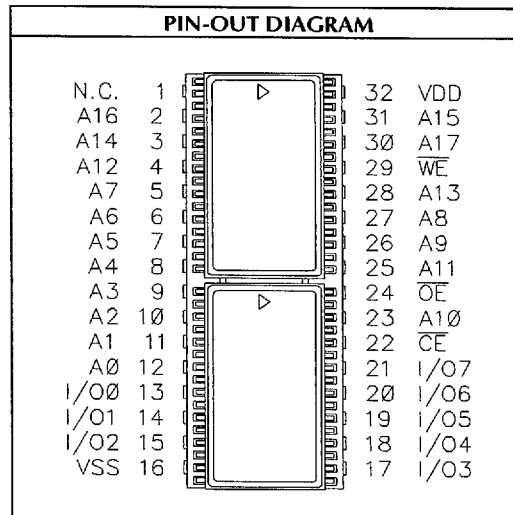
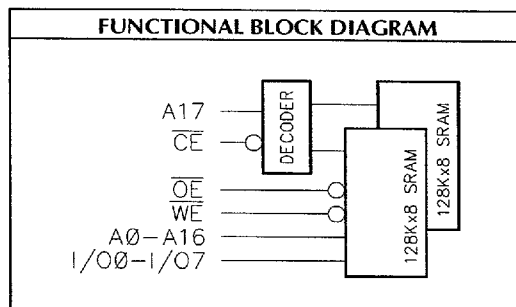


**FEATURES:**

- Organized Available: 256K x 8
- Access Times: 25\*, 35, 45, 55, 70, 85ns
- Fully Static Operation - No clock or refresh required
- All inputs and outputs are TTL-Compatible
- 600 mil, 32 - Pin JEDEC standard DIP pinout

PIN NAMES	
A0 - A17	Address Inputs
I/O0 - I/O7	Data In/Out
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V <sub>DD</sub>	Power (+5V)
V <sub>SS</sub>	Ground

\* Available in Commercial only.



RECOMMENDED OPERATING RANGE <sup>1</sup>						
Symbol	Characteristic	Min.	Typ.	Max.	Unit	
V <sub>DD</sub>	Supply Voltage	4.5	5.0	5.5	V	
V <sub>IH</sub>	Input HIGH Voltage	2.2		V <sub>DD</sub> +0.3	V	
V <sub>IL</sub>	Input LOW Voltage	-0.5 <sup>2</sup>		0.8	V	
T <sub>A</sub>	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	
		M/B	-55	+25	+125	

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
D <sub>OUT</sub> Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	D <sub>OUT</sub>	Active
Write	L	L	X	D <sub>IN</sub>	Active

H = HIGH                      L = LOW                      X = Don't Care

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V <sub>OH</sub>	HIGH Voltage	I <sub>OH</sub> = -4.0mA	2.4	-	V
V <sub>OL</sub>	LOW Voltage	I <sub>OL</sub> = 8.0mA		0.4	V

ABSOLUTE MAXIMUM RATINGS <sup>3</sup>			
Symbol	Parameter	Max.	Unit
T <sub>STC</sub>	Storage Temperature	-65 to +150	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
V <sub>DD</sub>	Supply Voltage <sup>1</sup>	-0.5 to +7.0	V
V <sub>I/O</sub>	Input/Output Voltage <sup>1</sup>	-0.5 to V <sub>DD</sub> +0.5	V

CAPACITANCE <sup>4</sup> : T <sub>A</sub> = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C <sub>ADR</sub>	Address Input	30	pF	V <sub>IN</sub> = 0V
C <sub>CE</sub>	Chip Enable	20		
C <sub>WE</sub>	Write Enable	30		
C <sub>OE</sub>	Output Enable	30		
C <sub>I/O</sub>	Data Input/Output	30		

DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to V <sub>DD</sub>	-10	+10	-10	+10	-10	+10	µA
I <sub>OUT</sub>	Output Leakage Current	V <sub>I/O</sub> = 0V to V <sub>DD</sub> , CE or OE = V <sub>IH</sub> , or WE = V <sub>IL</sub>	-20	+20	-20	+20	-20	+20	µA
I <sub>CC</sub>	Operating Supply Current	Cycle = min., Duty = 100%, I <sub>OUT</sub> = 0mA		160		165		185	mA
I <sub>SB1</sub>	Full Standby Supply Current (CMOS)	V <sub>IN</sub> ≥ V <sub>DD</sub> -0.2V or V <sub>IN</sub> ≤ V <sub>SS</sub> +0.2V, CE ≥ V <sub>DD</sub> -0.2V		10		10		20	mA
I <sub>SB2</sub>	Standby Current (TTL)	CE = V <sub>IH</sub>		40		50		50	mA
V <sub>OL</sub>	Output Low Voltage	I <sub>OUT</sub> = 8.0mA		0.4		0.4		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> = -4.0mA	2.4		2.4		2.4		V

DATA RETENTION CHARACTERISTICS									
Symbol	Parameter	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>D</sub> R	Data Retention Voltage	CE ≥ V <sub>D</sub> R -0.2V	2.0	5.5	2.0	5.5	2.0	5.5	V
I <sub>CCDR2</sub>	Data Retention Supply Current	V <sub>D</sub> R = 2.0V		0.5		0.8		3.6	mA
I <sub>CCDR3</sub>	Data Retention Supply Current	V <sub>D</sub> R = 3.0V		0.8		1.2		4.0	mA
t <sub>CDR</sub>	Chip Disable to Data Retention Time		0		0		0		ns
t <sub>R</sub>	Recovery Time	t <sub>RC</sub> = Read Cycle Timing	5		5		5		ms

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns *
Input and Output Timing Reference Levels	1.5V

Output Load		
Load	C <sub>L</sub>	Parameters Measured
1	30pF	except t <sub>CLZ</sub> , t <sub>OLZ</sub> , t <sub>CHZ</sub> , t <sub>OHZ</sub> , t <sub>WHZ</sub> , and t <sub>WLZ</sub>
2	5pF	t <sub>CLZ</sub> , t <sub>OLZ</sub> , t <sub>CHZ</sub> , t <sub>OHZ</sub> , t <sub>WHZ</sub> , and t <sub>WLZ</sub>

\* Transition measured between 0.8V and 2.2V.

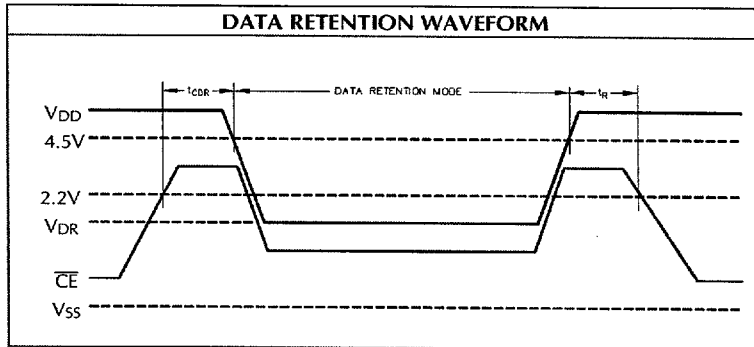
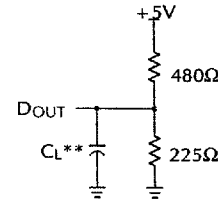


Figure 1. Output Load  
\*\* Including Probe and Jig Capacitance.

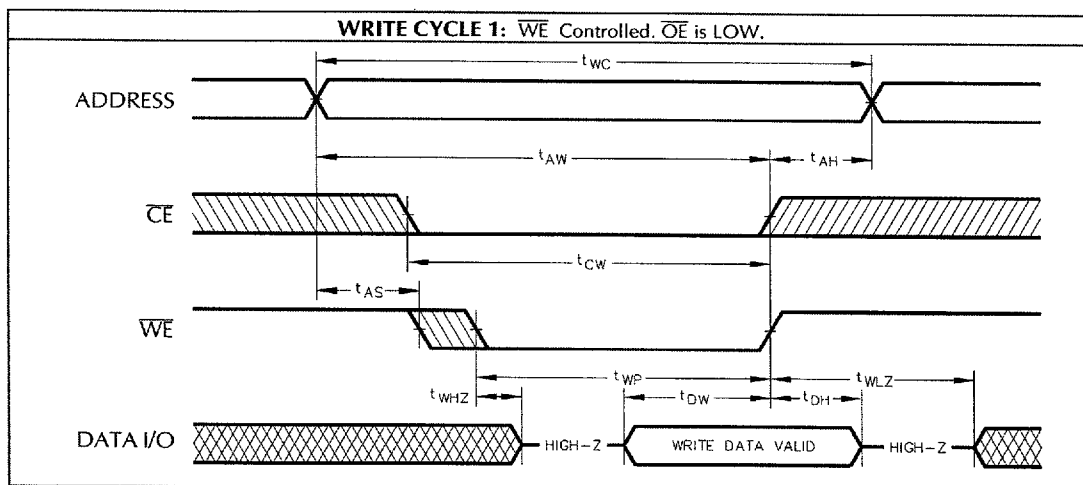
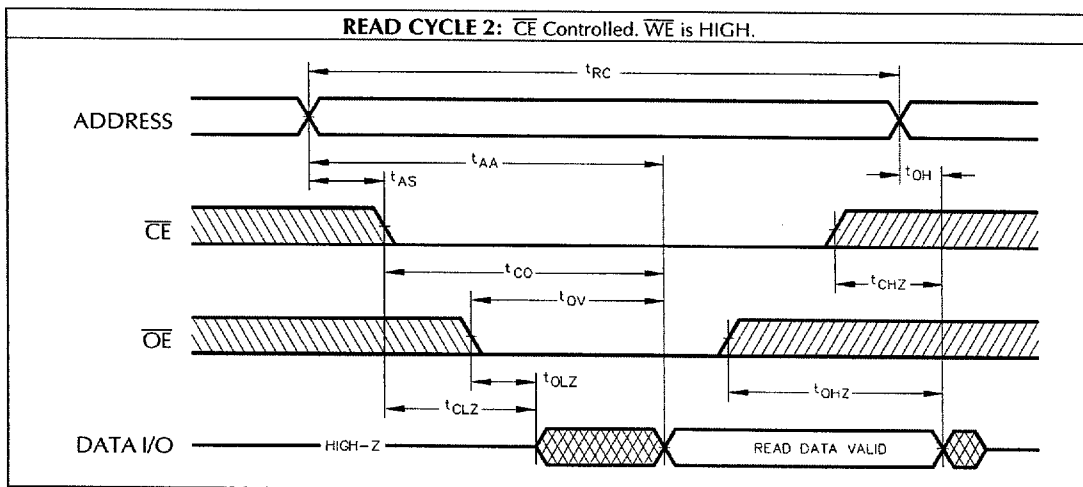
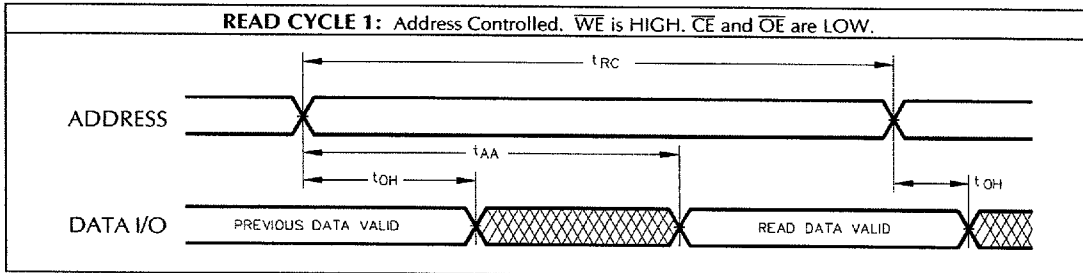


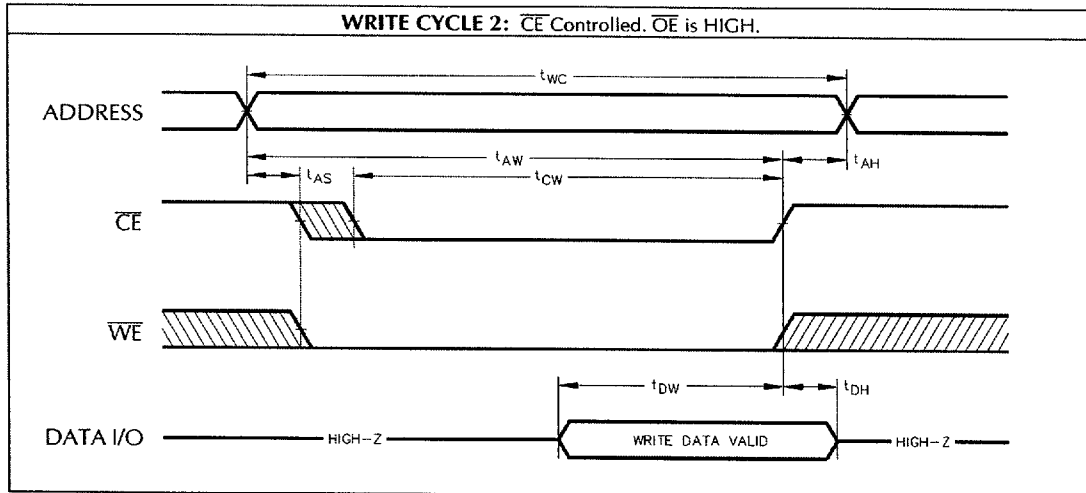
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	25ns †		35ns		45ns		55ns		70ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t <sub>RC</sub>	Read Cycle Time	25		35		45		55		70		ns
2	t <sub>AA</sub>	Address Access Time		25		35		45		55		70	ns
3	t <sub>CO</sub>	Chip Enable to Output Valid		25		35		45		55		70	ns
4	t <sub>OV</sub>	Output Enable to Output Valid		8		10		20		25		25	ns
5	t <sub>OH</sub>	Output Hold from Address Change	5		5		5		5		5		ns
6	t <sub>CLZ</sub>	Chip Enable to Output in LOW-Z <sup>4,6</sup>	5		5		5		5		5		ns
7	t <sub>OLZ</sub>	Output Enable to Output in LOW-Z <sup>4,6</sup>	0		0		0		0		0		ns
8	t <sub>CHZ</sub>	Chip Enable to Output in HIGH-Z <sup>4,6</sup>		20		25		30		30		35	ns
9	t <sub>OHZ</sub>	Output Enable to Output in HIGH-Z <sup>4,6</sup>		8		10		20		25		25	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges <sup>7</sup>													
No.	Symbol	Parameter	25ns †		35ns		45ns		55ns		70ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t <sub>WC</sub>	Write Cycle Time	25		35		45		55		70		ns
11	t <sub>AW</sub>	Address Valid to End of Write	20		30		40		50		65		ns
12	t <sub>CW</sub>	Chip Enable to End of Write	20		30		40		50		65		ns
13	t <sub>DW</sub>	Data to Write Time Overlap	12		15		15		20		25		ns
14	t <sub>DH</sub>	Data Hold Time from Write Time	0		0		0		0		0		ns
15	t <sub>WP</sub>	Write Pulse Width	17		20		25		30		35		ns
16	t <sub>AS</sub>	Address Set-up Time ***	0		0		0		0		0		ns
17	t <sub>AH</sub>	Address Hold Time	5		5		5		5		5		ns
18	t <sub>WHZ</sub>	Write Enable to Output in HIGH-Z <sup>4,6</sup>		8		10		15		20		25	ns
19	t <sub>WLZ</sub>	Write Enable to Output in LOW-Z <sup>4,6</sup>	0		0		0		0		0		ns

\*\*\* Valid for both Read and Write Cycles.  
† Available in commercial only.

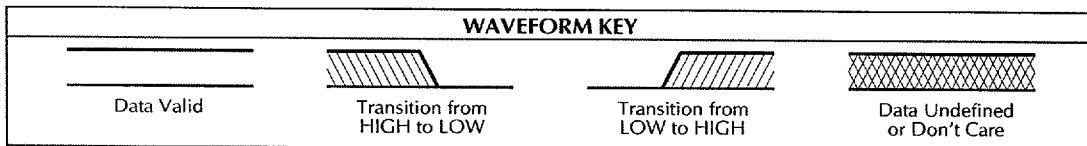


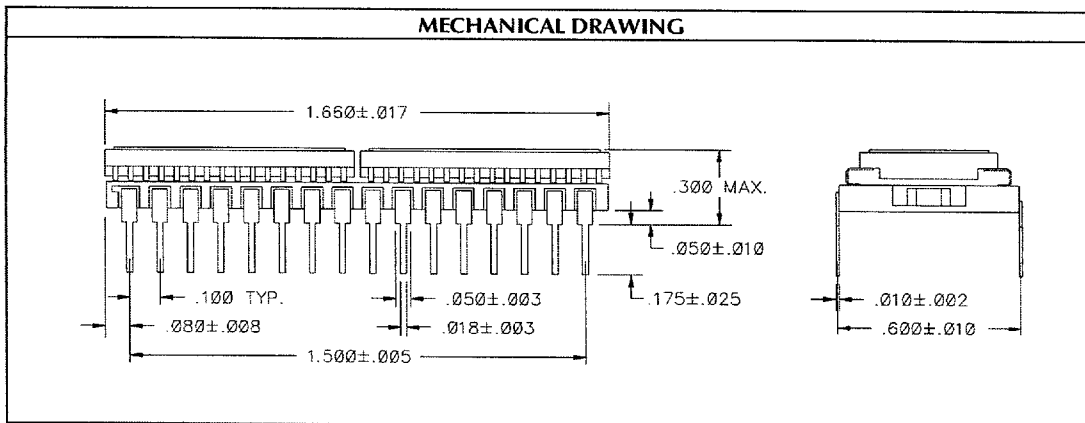
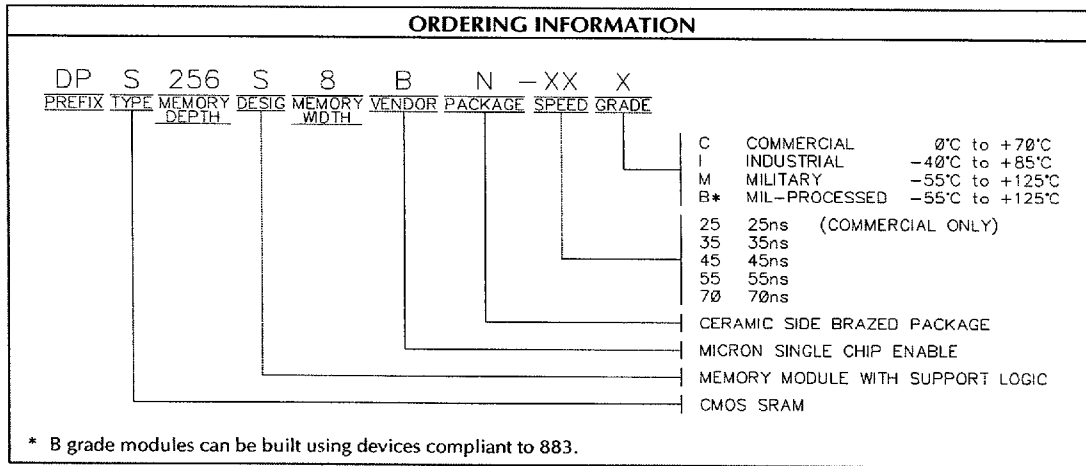




**NOTES:**

1. All voltages are with respect to  $V_{SS}$ .
2. -2.0V min. for pulse width less than 20ns ( $V_{IL}$  min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of  $\pm 500mV$  from steady state voltage.
6. When  $\overline{OE}$  and  $\overline{CE}$  are LOW and  $\overline{WE}$  is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when  $\overline{WE}$  is LOW.





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