DESCRIPTION

The HYM591000B is a 1M x 9-bit Fast page mode CMOS DRAM module consisting of two HY514400A and one HY531000A in 20/26 pin SOJ on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitor is mounted for each DRAM.
The HYM591000BM/BLM are Tin-Lead plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 1M byte memory.

FEATURES

- **Low power dissipation**
  Max. battery back-up 6.6mW (L-part)
  Max. CMOS standby 3.3mW (L-part)
  16.5mW
  Max. TTL standby 33.0mW
  Max. operating

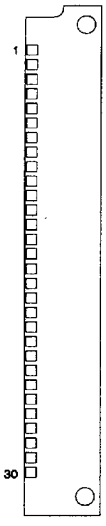
Speed	Power
60	1.73W
70	1.51W

- **Single power supply of 5V±10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

Speed	t_{RAC}	t_{CAC}	t_{PC}
60	60ns	15ns	40ns
70	70ns	20ns	45ns

- **Fast page mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh**
- **1024 refresh cycles / 128ms (L-part)**
  1024 refresh cycles / 16ms

PIN CONNECTION



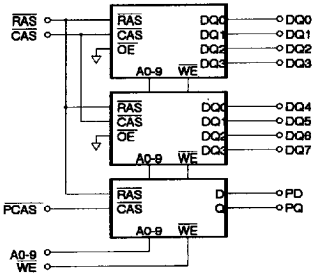
PIN DESCRIPTION

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{PCAS}$	$\overline{CAS}$ for Parity
$\overline{WE}$	Write Enable
A0-A9	Address Input
DQ0-DQ7	Data Input/Output
PD	Data In for Parity
PQ	Data Out for Parity
V_{CC}	Power (+5V)
V_{SS}	Ground

PIN NAME

#	NAME
1	VCC
2	$\overline{CAS}$
3	DQ0
4	A0
5	A1
6	DQ1
7	A2
8	A3
9	VSS
10	DQ2
11	A4
12	A5
13	DQ3
14	A6
15	A7
16	DQ4
17	A8
18	A9
19	NC
20	DQ5
21	$\overline{WE}$
22	VSS
23	DQ6
24	NC
25	DQ7
26	PQ
27	$\overline{RAS}$
28	$\overline{PCAS}$
29	PD
30	VCC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	−55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	2.4	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	−1.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V±10%, V_{SS} = 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pin)	$V_{SS} \le V_{IN} \le V_{CC}$ + 1.0, All other pins not under test = V_{SS}		-30	30	μA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	μA	
I_{CC1}	V_{CC} Supply Current, Operating	$t_{RC} = t_{RC}$ (min.)	60 70	- -	315 275	mA	1,2,3
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs ≥ V_{SS}		-	6	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	$t_{RC} = t_{RC}$ (min.)	60 70	- -	315 275	mA	1,3
I_{CC4}	V_{CC} Supply Current, Fast Page mode	$t_{PC} = t_{PC}$ (min.)	60 70	- -	210 175	mA	1,2,3
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ V_{CC}–0.2V	 L-part	- -	3 0.6	mA	 5
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	$t_{RC} = t_{RC}$ (min.)	60 70	- -	315 275	mA	1,3
I_{CC7}	V_{CC} Supply Current, Battery Back Up (L-part only)	t_{RC} = 125μs, $\overline{CAS}$ = CBR cycling or 0.2V, $\overline{WE}$ = V_{CC}–0.2V, A0-A9 = V_{CC}–0.2V or 0.2V, DQ0-DQ7 = V_{CC}–0.2V, 0.2V, or open	t_{RAS} ≤ 300ns t_{RAS} ≤ 1μs	- -	0.9 1.2	mA	1,4,5
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH} = –5mA		2.4	-	V	

NOTE :
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
4. Only t_{RAS}(max.) = 1μs is applied to refresh of battery backup but t_{RAS}(max.) = 10μs is applied to normal functional operation.
5. I_{CC5}(max.) = 0.6mA and I_{CC7} are applied to L-part only (HYM591000BLM).

AC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V±10%, V_{SS} = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM591000BM/BLM -60 MIN.	-60 MAX.	-70 MIN.	-70 MAX.	UNIT	NOTE
1	tRC	Random Read or Write Cycle Time	110	-	130	-	ns	
2	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	ns	
4	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	60	-	70	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	15	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	ns	4
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	20	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	40	-	50	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100K	70	100K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	15	-	20	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	60	-	70	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	15	10K	20	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	20	50	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	50	-	55	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	15	-	15	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	15	-	20	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	50	-	55	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	ms	
		L-part	-	128	-	128		11
40	tWCS	Write Command Set-up Time 0 -	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM591000BM/BLM				UNIT	NOTE
			-60		-70			
			MIN.	MAX.	MIN.	MAX.		
41	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	5	-	5	-	ns	
42	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	15	-	15	-	ns	
43	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	40	-	40	-	ns	
44	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	ns	
45	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time (CBR Cycle)	10	-	10	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initilization cycles instead of 8 $\overline{RAS}$-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Transition time is measured between V_{IH} and V_{IL} and assumed to be 5ns for all inputs.
3. Refer to the HY514400A and HY531000A data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. t_{REF}(max.) = 1024ms is applied to L-part only (HYM591000BLM).

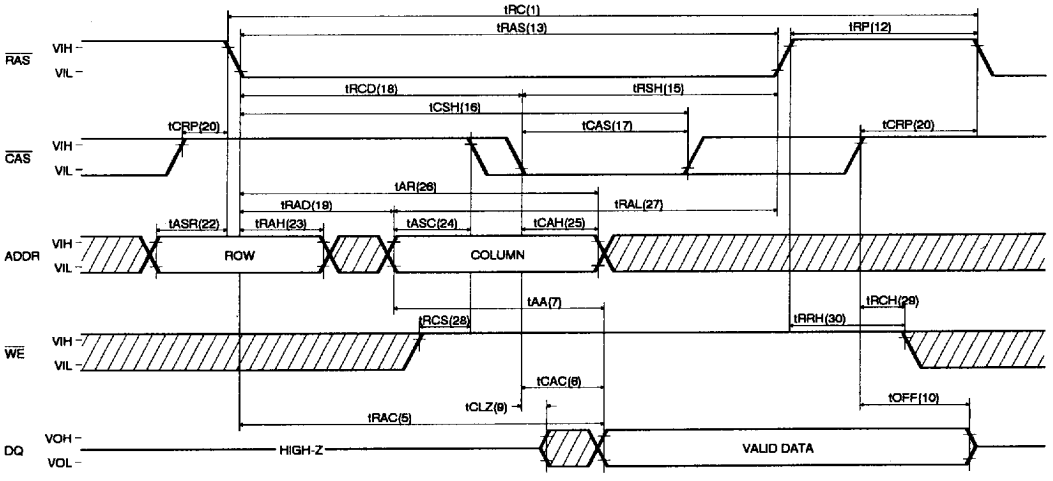
CAPACITANCE

(T_A = 25°C, V_{CC} = 5V±10%, V_{SS} = 0V, f = 1MHz, unless otherwise noted.)

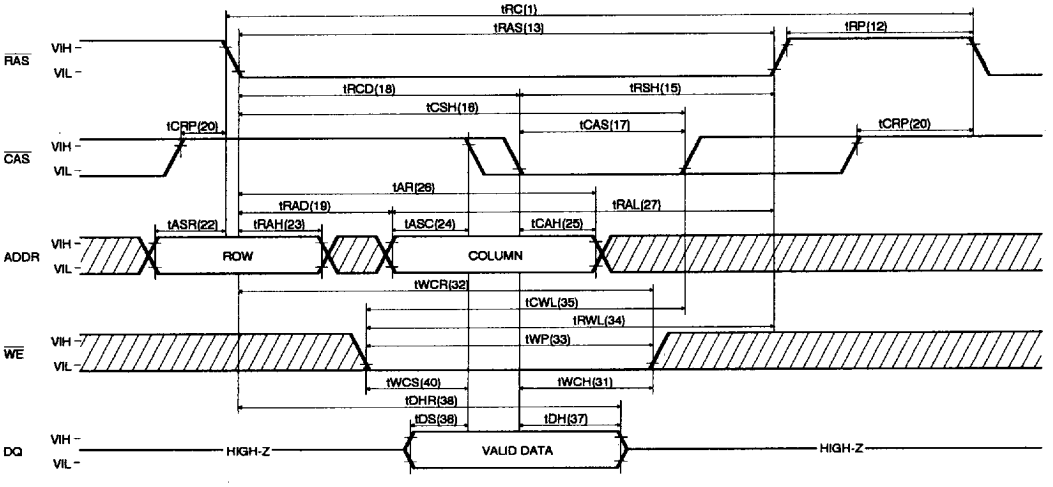
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A9, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	-	25	pF
C_{IN2}	Input Capacitance (PD, $\overline{PCAS}$)	-	10	pF
C_{DQ}	I/O Capacitance (DQ0-DQ7)	-	15	pF
C_{PQ}	Output Capacitance (PQ)	-	10	pF

TIMING DIAGRAM

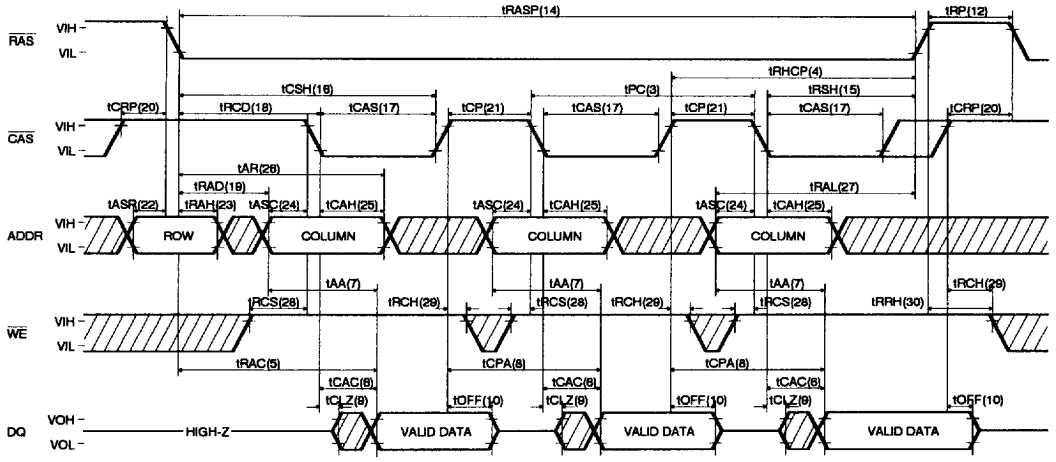
READ CYCLE



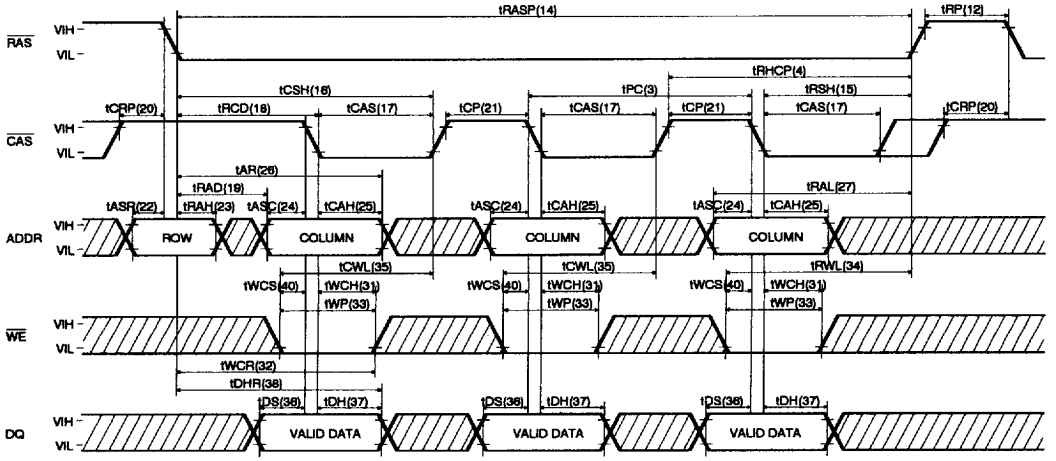
EARLY WRITE CYCLE



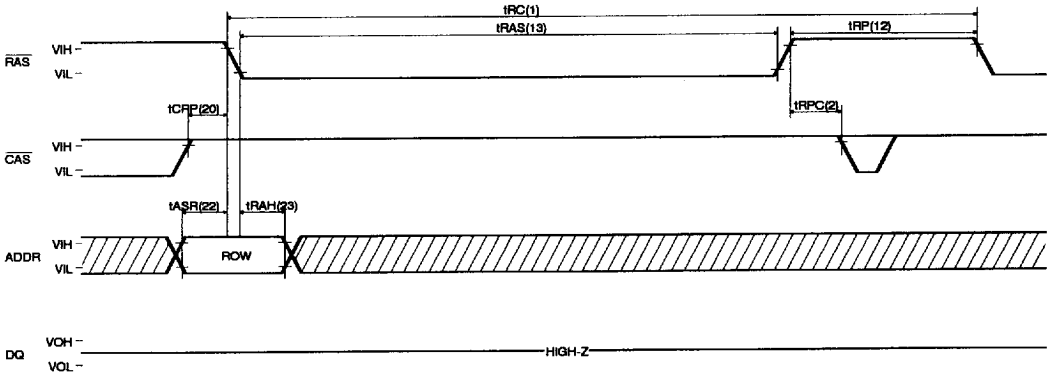
FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE

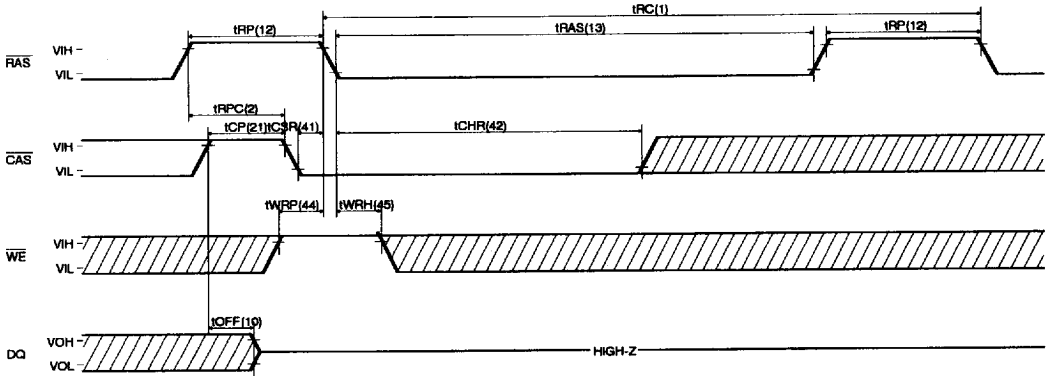


$\overline{RAS}$-ONLY REFRESH CYCLE



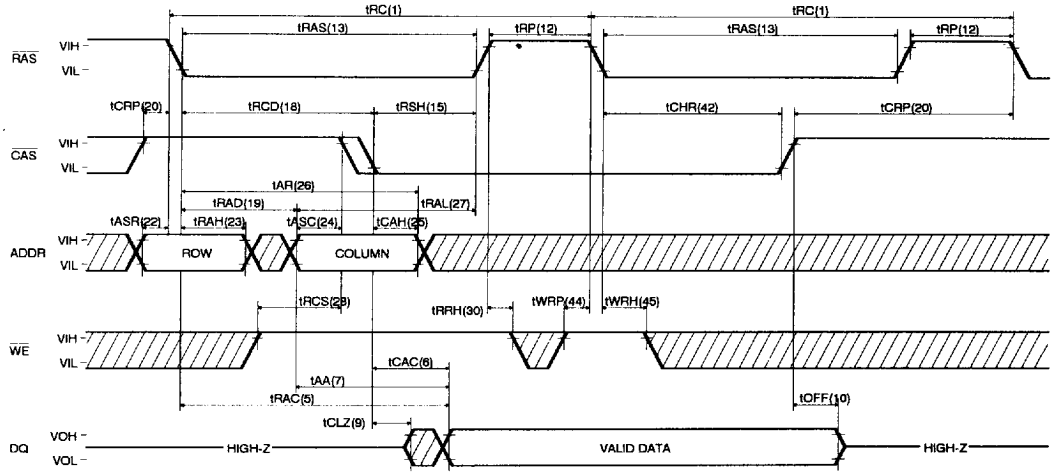
NOTE : $\overline{WE}$ = "H" or "L"

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

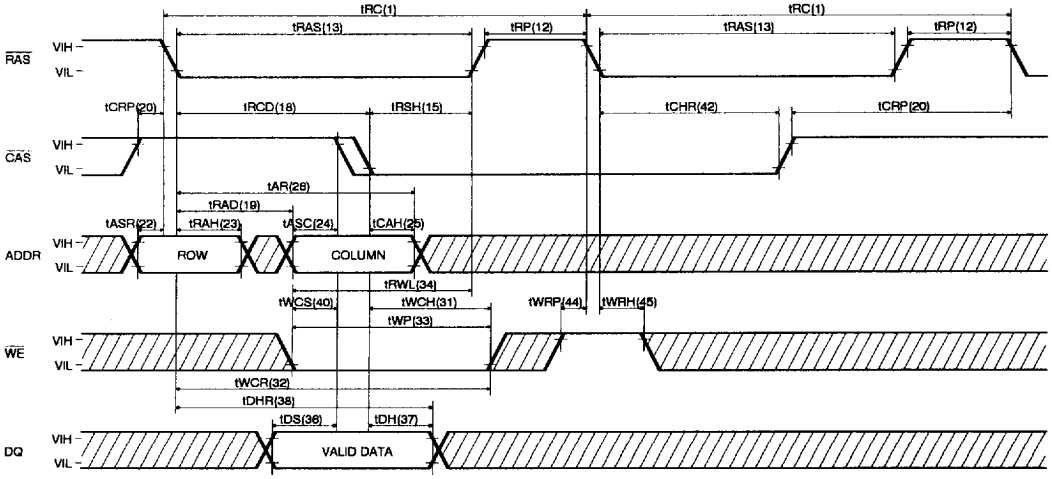


NOTE : ADDR = "H" or "L"

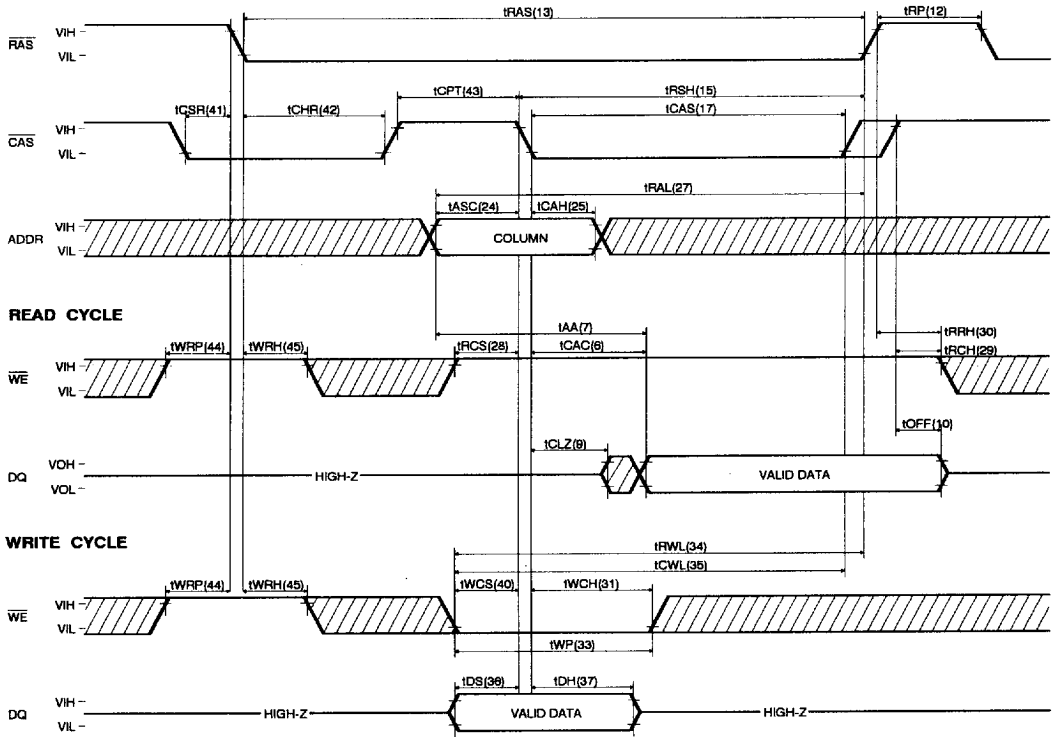
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



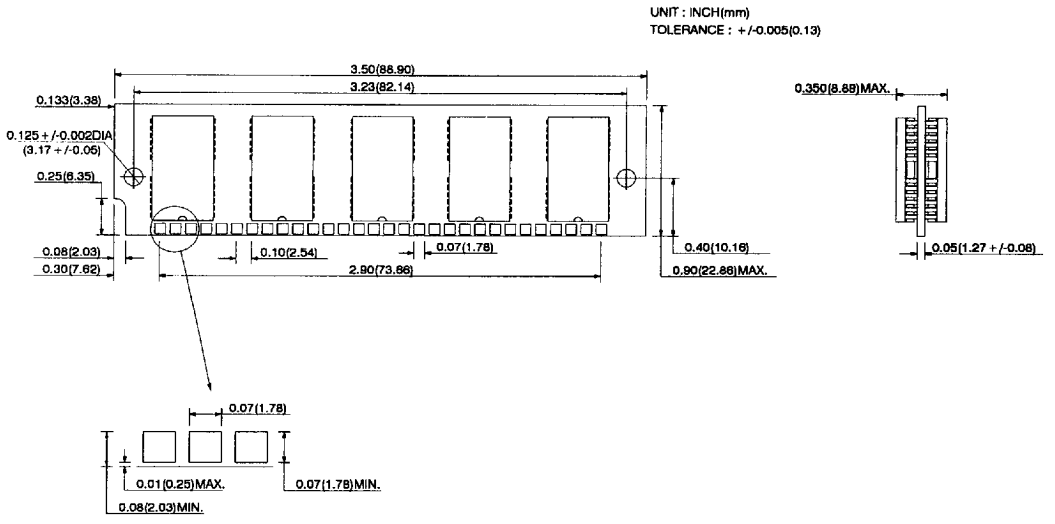
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



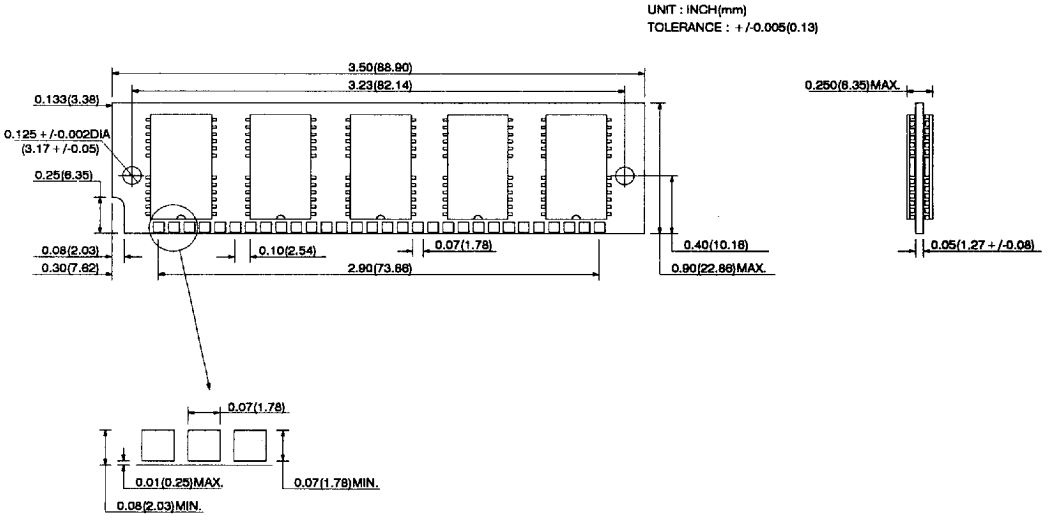
PACKAGE INFORMATION

30 pin Single In-line Memory Module (M ; Tin-Lead plated)

HYM591610M/LM (SOJ mounted)



HYM591610TM/LTM (TSOP-II mounted)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM591000BM	60/70		SIMM	Tin-Lead
HYM591000BLM	60/70	L-part	SIMM	Tin-Lead