PLESSEY Semiconductors

PRELIMINARY INFORMATION

T-75-27-07

MV8870-1

DTMF RECEIVER

The MV8870-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Plessey Semiconductors' double-poly CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code.

External component count is minimised by on-chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface.

FEATURES

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality

APPLICATIONS

- Receiver Systems for BT or CEPT Specifications
- Paging Systems
- Repeater Systems/Mobile Radio
- Credit Card Systems
- Remote Control

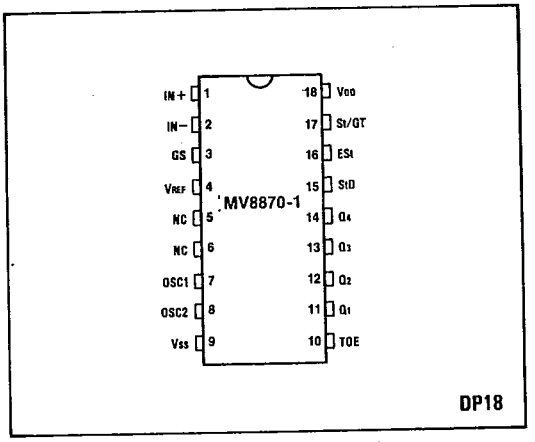


Fig.1 Pin connections - top view

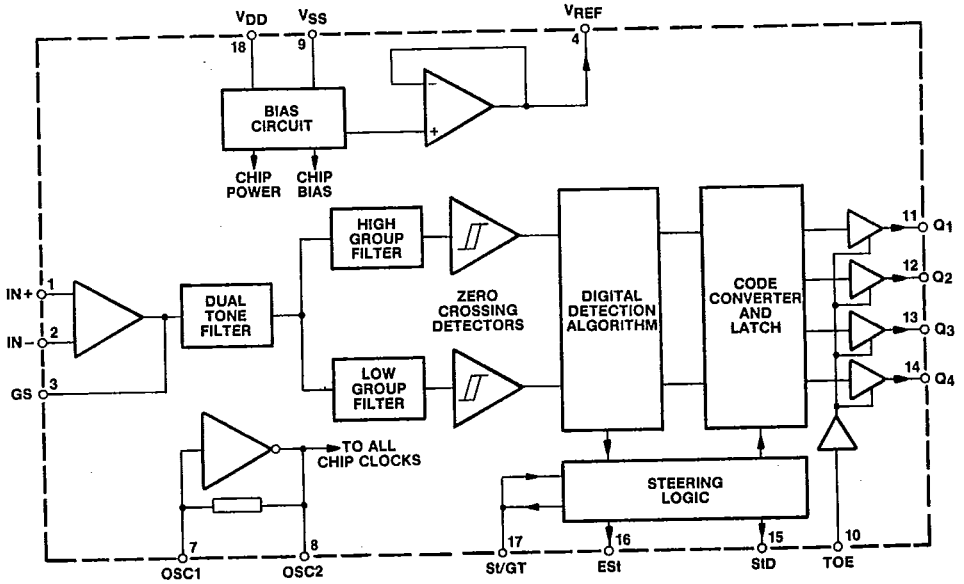


Fig.2 Functional block diagram

FUNCTIONAL DESCRIPTION

The MV8870-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low tone groups, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high-group frequencies. The filter section also incorporates notches at 350 and 440Hz for exceptional dial tone rejection (see Fig.3) Each filter is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full supply rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognises the presence of two valid tones (this is referred to as the 'Signal Condition' in some industry specifications) the 'Early Steering' output (ESt) will go to an active state. Any subsequent loss of signal condition will cause the ESt pin to go to its inactive state (see Fig.5).

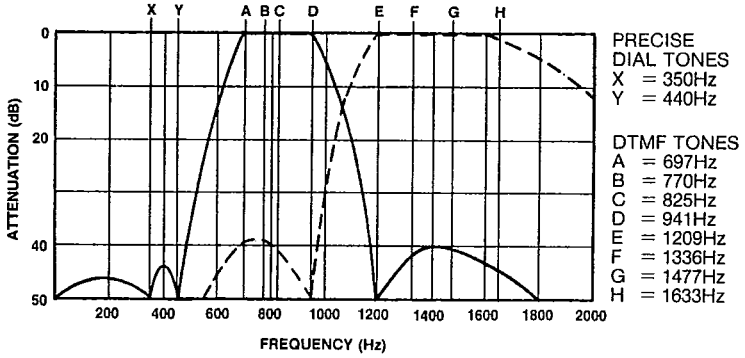


Fig.3 Filter response

Steering Circuit

Before registration of a decoded tone-pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes the voltage at the St/GT pin ($V_{St/GT}$) to rise as the capacitor discharges (see Figs.4 and 5).

Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), $V_{St\,GT}$ reaches the threshold (V_{TSt}) of the steering logic which allows it to register the tone pair and strobe the corresponding 4-bit code into the output latch (see Table 1). At this point the St/GT pin is activated as an output and drives $V_{St/GT}$ to V_{DD} (see Fig.5).

St/GT continues to drive high as long as ESt remains high. After a short delay to allow the output latch to settle, the delayed steering output pin (StD) goes high to indicate that the code for a new received tone-pair is available. The contents of the output latch are output onto the output bus (Q_1 to Q_4 pins) when the three-state output enable pin (TOE) is high.

The steering circuit works in reverse to validate the interdigit pause between signals. Thus as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop-out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

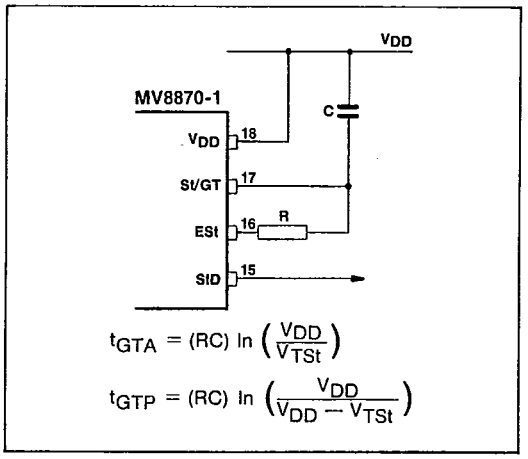
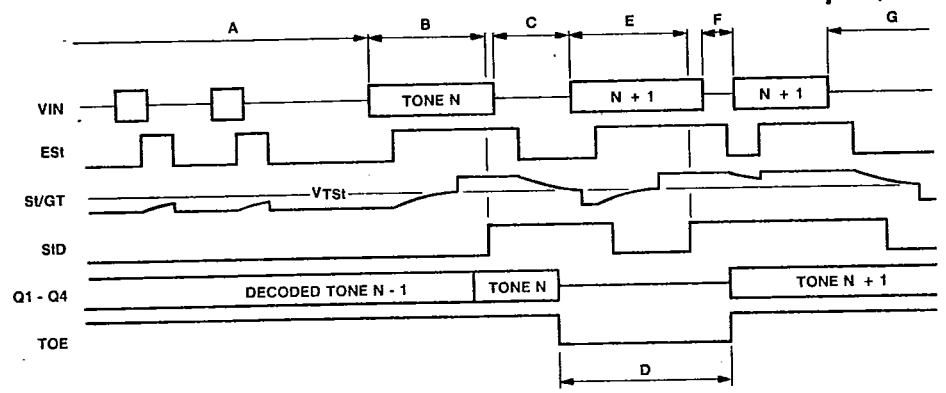


Fig.4 Basic steering circuit



Explanation of Events

A. Tone bursts detected, but tone duration invalid and output latch unchanged.
B. Tone N detected, tone duration valid, output latch updated and new data signalled by StD.
C. End of tone N detected, tone absent duration valid, but output latch not updated until next valid tone.
D. Outputs switched to high impedance.
E. Tone N + 1 detected, tone duration valid, tone decoded, output latch updated (although outputs are currently high impedance) and new data signalled by StD.
F. Acceptable dropout of tone N + 1, tone absent duration invalid, StD and output latch unchanged.
G. End of tone N + 1 detected, tone absent duration valid, StD goes low but output latch not updated until next valid tone.

Fig.5 Timing diagram

F_{LOW}	F_{HIGH}	KEY	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1209	0	H	1	0	1	0
941	1336	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	Any	L	Z	Z	Z	Z

Table 1 Functional decode

APPLICATIONS

A simple application circuit is shown in Fig.6. This has a symmetric guard time circuit, a single-ended analog input and a dedicated crystal oscillator.

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigit pause, the simple steering circuit shown in Fig.6 is applicable. Component values are chosen according to the formula (see Figs.4, 7 and 8):

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

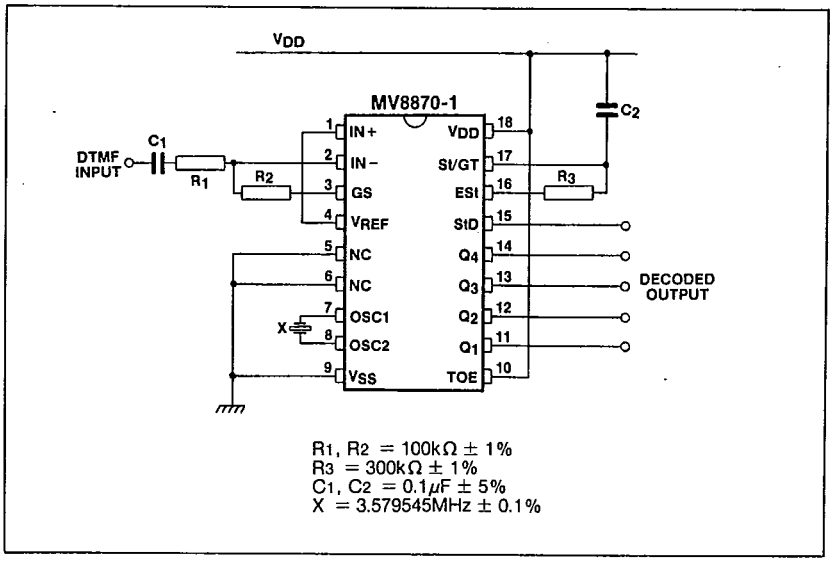
The value of t_{DP} is a device parameter (see Dynamic Characteristics) and t_{REC} is the minimum signal duration to be recognised by the receiver. Likewise t_{DA} is a device parameter and t_{ID} is the minimum time taken to recognise an interdigit pause. A value for C of 0.1μF is recommended for most applications, leaving R to be selected by the designer.

Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal conditions long enough to be registered. Alternatively a relatively short t_{REC} with a long t_{ID} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figs.7 and 8.

Differential Input Configuration

The input arrangement of the MV8870-1 provides a differential input op. amp. and a bias source (V_{REF}) to bias the inputs at mid-rail. The gain may be adjusted through a feedback resistor from the op. amp. output (GS). In a single-ended configuration the input pins are connected as shown in Fig.6 where the op. amp. is connected to give unity gain and the V_{REF} pin biases the input at $V_{DD}/2$.

Fig.9 shows the differential configuration. In this circuit gain is adjusted through the feedback resistor R5.



R1, R2 = 100kΩ ± 1%
R3 = 300kΩ ± 1%
C1, C2 = 0.1μF ± 5%
X = 3.579545MHz ± 0.1%

PLESSEY SEMICONDUCTORS

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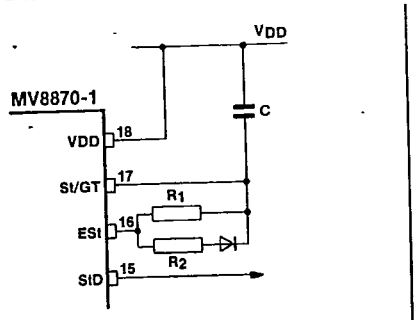
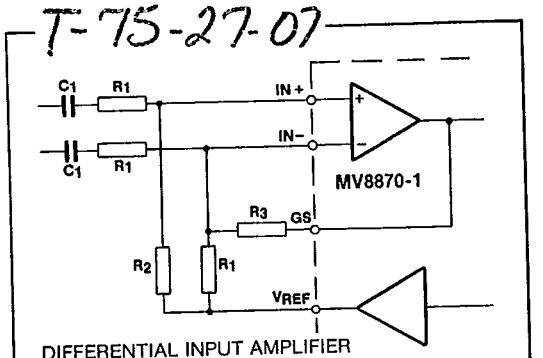


$$t_{GTA} = (Rp\,C)\ln\frac{V_{DD}}{V_{TSt}}$$

$$t_{GTP} = (R1\,C)\ln\frac{V_{DD}}{V_{DD}-V_{TSt}}$$

$$Rp = \frac{R1\,R2}{R1+R2}$$

Fig.7 Guard time adjustment ($t_{GTP} < t_{GTA}$)



DIFFERENTIAL INPUT AMPLIFIER

$C_1 = C_1 = 10nF$
$R_1 = R_4 = R_1 = 100k\Omega$
$R_2 = 60k\Omega$ $R_3 = 37.5k\Omega$

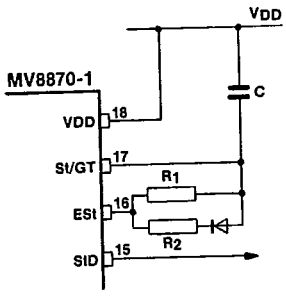
All resistors ±1 %
All capacitors ±5 %

$$R_3 = \left(\frac{R_2\,R_5}{R_2+R_5}\right)$$

$$\text{VOLTAGE GAIN (Av diff)} = \frac{R_5}{R_1}$$

$$\text{INPUT IMPEDANCE (ZIN diff)} = 2\sqrt{R1^2 + \left(\frac{1}{\omega C}\right)^2}$$

Fig.9 Differential input configuration



$$t_{GTA} = (R1\,C)\ln\frac{V_{DD}}{V_{TSt}}$$

$$t_{GTP} = (Rp\,C)\ln\frac{V_{DD}}{V_{DD}-V_{TSt}}$$

$$Rp = \frac{R2\,R1}{R2+R1}$$

Fig.8 Guard time adjustment ($t_{GTP} > t_{GTA}$)

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.78MHz crystal which is normally connected as shown in Fig.6. However, it is possible to configure several MV8870-1 devices to use only a single oscillator crystal. The devices are chained together with the oscillator output of the first device in the chain capacitively coupled to the oscillator input of the second device and so on down the chain. The details are shown in Fig.10. Precision balancing capacitors are not required as problems of unbalanced loading are not a concern.

Receiver System for British Telecom Specification POR 1151

The circuit shown in Fig.11 illustrates the use of the MV8870-1 in a typical receiver system. The BT specification defines the non-operate level as input signals below -34dBm. This is obtained by choosing R1 and R2 to give 3dB of attenuation so that an input of -34dBm corresponds to -37dBm at the op. amp. outpt pin (GS). The tolerances on R3 and C2 give a tolerance on guard time of 6%. For better performance the non-symmetric guard time circuit shown in Fig.12 is recommended.

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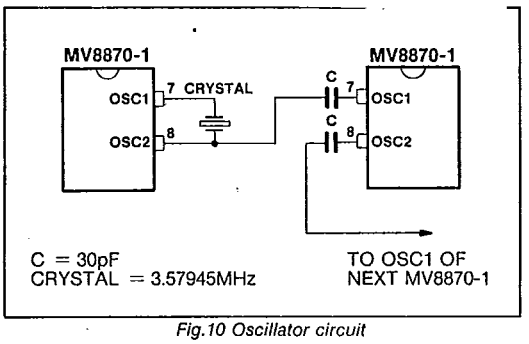

Fig.10 Oscillator circuit

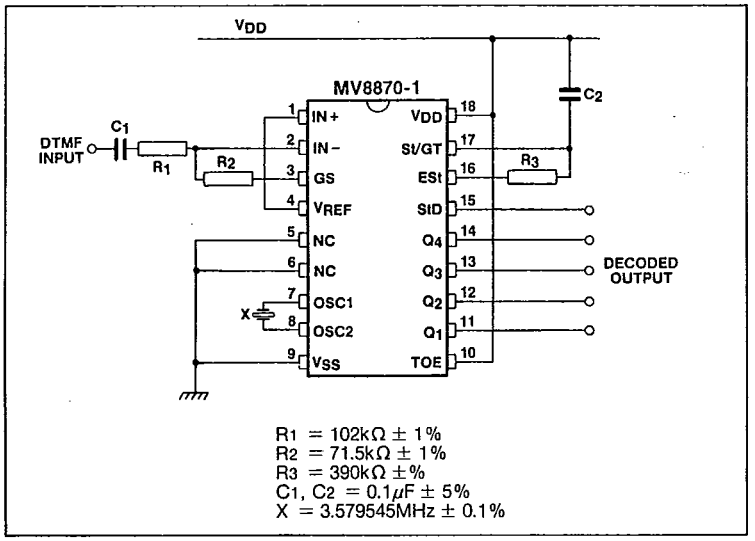

Fig.11 Single ended input configuration for BT or CEPT spec

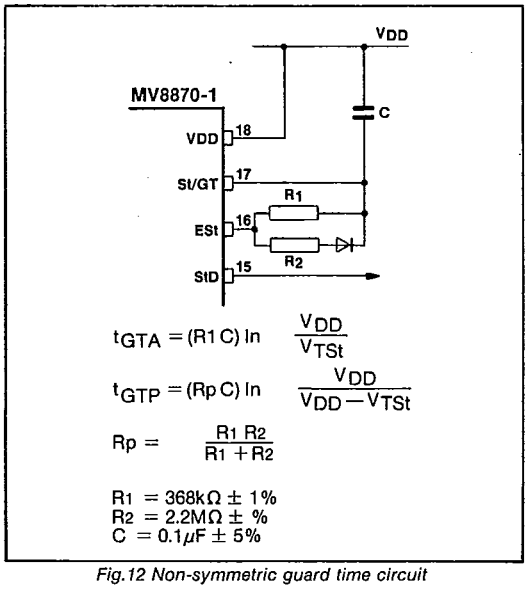

Fig.12 Non-symmetric guard time circuit

PIN DESCRIPTIONS

Symbol	Pin No.	Pin name and description
IN+, IN-	1,2	**In Plus and Minus (Voltage Inputs).** These are respectively the non-inverting and inverting inputs to the front-end op. amp. The DTMF input is applied to these pins in normal operation.
GS	3	**Gain Select (Voltage Output).** This pin is connected to the output of the front-end op. amp. A feedback resistor between this pin and the inverting input (IN-) controls the front-end gain.
V_{REF}	4	**Reference Voltage (Voltage Output).** This pin outputs a voltage which is half-way between the power supply voltages (V_{SS} and V_{DD}). It can be used to bias the input signal.
(IC)	5,6	**(Internal Connection).** These pins should be tied to the ground (V_{SS}).
OSC1	7	**Oscillator 1 (Digital Input).** This is the input to the inverter of the oscillator circuit. There is an internal biasing resistor between this pin and the inverter output (OSC2). A 3.579545MHz crystal is normally connected externally between the two pins to complete the oscillator circuit.
OSC2	8	**Oscillator 2 (Digital Output).** This is the output of the inverter of the oscillator circuit. There is an internal biasing resistor between this pin and the inverter input (OSC1). A 3.579545MHz crystal is normally connected externally between the two pins to complete the oscillator circuit.
V_{SS}	9	**Negative Supply (Power Input).** This is the negative power supply for the device. It is normally 0V.
TOE	10	**Three-State Output Enable (Digital Input with Pull-up).** If this pin is high then the decoder outputs (Q_1 to Q_4) are enabled. If it is low then the outputs go into their high impedance state. There is an internal pull-up at this pin.
Q_1 - Q_4	11 - 14	**Q_1 to Q_4 (Three-State Outputs).** When the TOE pin is high these pins output the code in the output latch which corresponds to the last valid tone-pair detected. They go into their high impedance state when the TOE pin is low.
StD	15	**Delayed Steering (Digital Output).** This pin follows the ESt and St/GT pins. It goes high to indicate that a new tone-pair has been detected and the corresponding code has been loaded into the output latch. It goes low to indicate that a new tone-pair is expected.
ESt	16	**Early Steering (Digital Output).** This pin goes high when the digital detection algorithm decides that there is a valid DTMF input. It goes low as soon as the algorithm decides that there is no valid DTMF input. In normal use this pin is used to drive an external guard time circuit which in turn drives the St/GT pin.
St/GT	17	**Steering/Guard Time (Voltage Input/Digital Output).** This pin follows the ESt pin. When ESt pin changes state this pin acts as an input and monitors the voltage developed here by the ESt pin acting through the external guard time circuit. When the voltage reaches the internally generated V_{TSI} level then this pin acts as an output and pulls itself fully to the state of the ESt pin. When this pin goes fully high a new code is loaded into the output latch and the StD pin goes high. When this pin goes fully low the device prepares itself for a new tone-pair and the StD pin goes low.
V_{DD}	18	**Positive Supply (Power Input).** This is the positive power supply for the device. It is normally 5V.

ELECTRICAL CHARACTERISTICS

Test Conditions (see Fig.13) - Voltages are with respect to ground (V_{SS})

Parameter	Symbol	Value			Units
		Min.	Typ. (1)	Max.	
Positive supply voltage (V_{DD} pin)	V_{DD}	4.75	5	5.25	V
Ambient temperature	T_{amb}	-40		+85	°C
Op. amp. output capacitive load (GS pin)	C_{OUT}			100	pF
Op. amp. output resistive load (GS pin)	R_{OUT}	50			kΩ
Input high voltage (OSC1 and TOE pins)	V_{IH}	3.5		V_{DD}	V
Input low voltage (OSC1 and TOE pins)	V_{IL}	0		1.5	V
Oscillator frequency (OSC1 and OSC2 pins)	fo	3.5759	3.579545	3.5831	MHz
Oscillator input rise time (OSC1 pin)	t_{OR}			110	ns
Oscillator input high time (OSC1 pin)	t_{OH}	110		170	ns
Oscillator input fall time (OSC1 pin)	t_{OF}			110	ns
Oscillator input low time (OSC1 pin)	t_{OL}	110		170	ns
Oscillator output load (OSC2 pin)	C_{LO}			30	pF

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

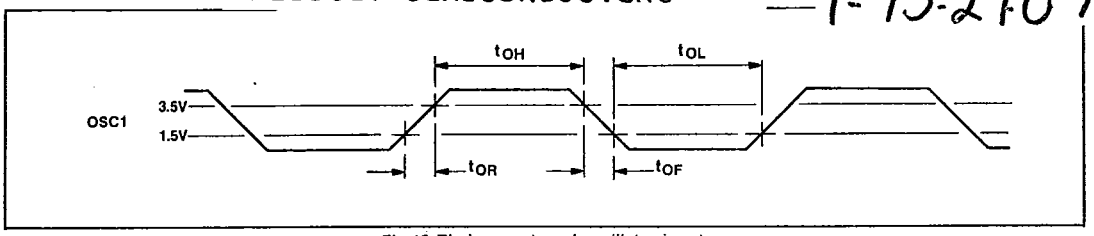

Fig.13 Timing - external oscillator input

Static Characteristics - Voltages are with respect to ground (Vss)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ. (1)	Max.		
Power dissipation	P_D		15	37	mW	
Supply current (V_{DD} pin)	I_{DD}		3.0	7.0	mA	
Reference voltage (V_{REF} pin)	V_{REF}	2.4		2.8	V	
Reference output resistance (V_{REF} pin)	R_{REF}		10		kΩ	
Input leakage current (OSC1, IN+ and IN- pins)	I_I		100		nA	$0 \leqslant V_{PIN} \leqslant V_{DD}$
Internal pull-up current (TOE pin)	I_{PU}		7.5	15	A	$0 \leqslant V_{PIN} \leqslant V_{DD}$
Output low sink current (OSC2, Q_1 - Q_4, StD, ESt and St/GT pins)	I_{OL}	1	2.5		mA	$0.4V \leqslant V_{PIN} \leqslant V_{DD}$
Output high source current (OSC2, Q_1 - Q_4, StD, ESt and St/GT pins)	I_{OH}	0.4	0.8		mA	$0V \leqslant V_{PIN} \leqslant 4.6V$
Steering threshold voltage (St/GT pin)	V_{TSt}	2.2		2.5	V	
Pin capacitance	C_P		7	15	pF	Pin to supplies

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Dynamic Characteristics: Input Op. Amp. - Voltages are with respect to ground (Vss)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ. (1)	Max.		
Input impedance (IN+ and IN- pins)	R_{IN}		10		MΩ	1kHz
Input offset voltage (IN+ and IN- pins)	V_{OS}		25		mV	
Power supply rejection	PSRR		60		dB	1kHz
Common mode range	V_{CM}		3.0		V p-p	No load
Common mode rejection	CMRR		60		dB	
DC open loop voltage gain	A_{VOL}		65		dB	
Open loop unit gain bandwidth	fc		1.5		MHz	
Output voltage swing (GS pin)	Vo		4.5		V p-p	R_{OUT} to V_{SS} $\geqslant$ 100kΩ

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

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Dynamic Characteristics: Detector - Voltages are with respect to ground (Vss)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ. (13)	Max.		
Valid input level (GS pin)	V_{VL}	61.7		2458	mV p-p	1,2,3,5,6,9
	P_{VL}	-31		1	dBm	
Invalid input level (GS pin)	V_{IL}			30.8	mV p-p	1,2,3,5,6,9
	P_{IL}			-37	dBm	
Acceptable positive twist	T_{AP}	6	10		dB	2,3,6,9
Acceptable negative twist	T_{AN}	6	10		dB	2,3,6,9
Acceptable frequency deviation	Δ_{FA}	-(1.5% +2Hz)		(1.5 % +2Hz)		2,3,5,9
Frequency deviation - rejected as too low	Δ_{FRL}		-5%	-3.5%		2,3,5,9
Frequency deviation - rejected as too high	Δ_{FRH}	3.5 %	5 %			2,3,5,9
Third tone tolerance	P_{TTT}	-18.5			dB	2,3,4,5,9,12
Noise tolerance	P_{NT}		-12		dB	2,3,4,5,7,9,10
Dial tone tolerance	P_{DTT}		22		dB	2,3,4,5,8,9,11
Tone present detect time	t_{DP}	5	11	14	ms	
Tone absent detect time	t_{DA}	0.5	4	8.5	ms	

NOTES
1. dBm = decibels above or below a reference power of 1mW into a 600 Ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration = 40ms. tone pause = 40ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tone in composite signal have equal amplitudes.
6. Tone pair is deviated by ± (1.5% + 2Hz).
7. Bandwidth limited (3kHz) Gaussian Noise.
8. The precise dial tone frequencies are (350Hz and 440Hz) ±2%.
9. For an error rate of better than 1 in 10.000.
10. Referenced to lowest frequency component in DTMF signal.
11. Referenced to the minimum valid input level.
12. Referenced to Fig.11. Input DTMF Tone Level at -25dBm (-28dBm at GS pin). Interference Frequency Range is 480 to 3400Hz.
13. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

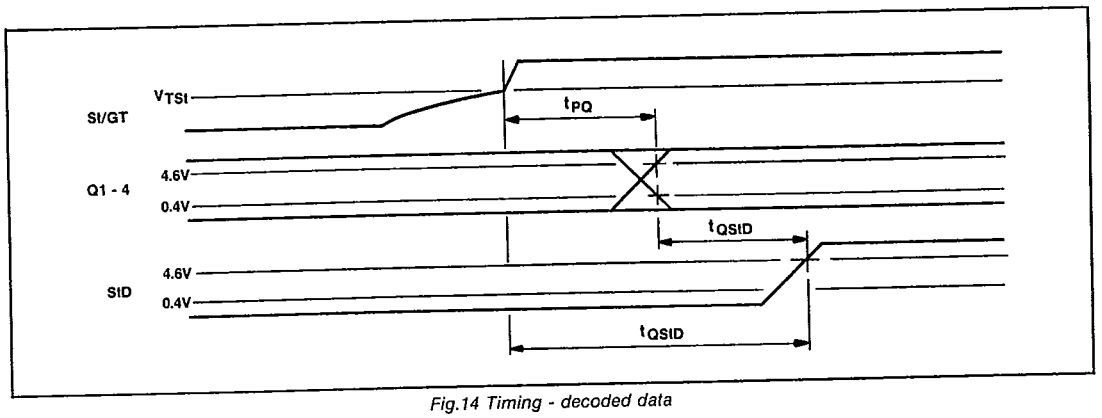

Fig.14 Timing - decoded data

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Dynamic Characteristics: Decoder (see Figs.14 and 15) - Voltages are with respect to ground V_{SS})

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ. (1)	Max.		
Propagation delay (St/GT to Q)	t_{PQ}		8	11	μs	TOE pin high
Propagation delay (St/GT to StD)	t_{PStD}		12		μs	
Output data set-up time (Q to StD)	t_{QStD}		3.4		μs	TOE pin high
Enable propagation delay (TOE to Q)	T_{PTE}		50		ns	R_L = 10kΩ (pulldown) C_L = 50pF
Disable propagation delay (TOE to Q)	t_{PTD}		300		ns	R_L = 10kΩ (pulldown) C_L = 50pF

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

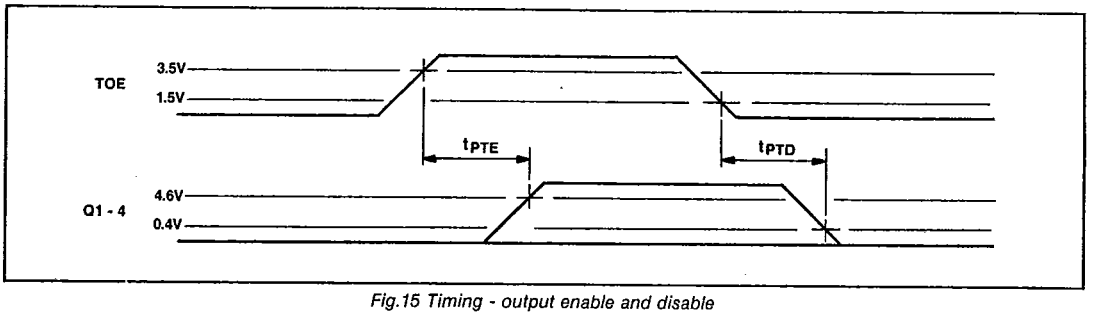

Fig.15 Timing - output enable and disable

ABSOLUTE MAXIMUM RATINGS

Voltages are with respect to the negative power supply (V_{SS})

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Positive supply voltage (pin 18), V_{DD}	6V
Voltage on any pin (other than supplies), V_{MAX}	-0.3V to V_{DD} +0.3V
Current at any pin (other than supplies), I_{MAX}	10mA
Storage temperature, T_{STG}	-65°C to +150°C
Package power dissipation, P_{DISS}	1000mW