MX27L2048

2M-BIT(256K x 8/ 128K x 16) CMOS EPROM

FEATURES

- 128K x 16 organization(MX27C2048, JEDEC pin out)
- +12.5V programming voltage
- Fast access time: 150/200/250 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 20mA @ 3.6V, 5MHz
- Standby current: 20μA
- Package type:
  - 40 pin ceramic DIP
  - 40 pin plastic DIP
  - 44 pin PLCC
  - 40 pin TSOP(I)

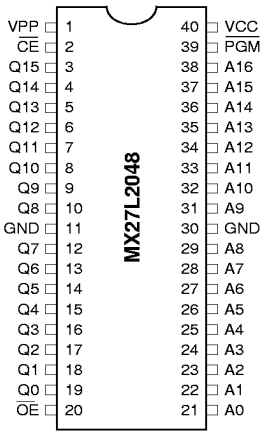
GENERAL DESCRIPTION

The MX27L2048 is a 3V only, 2M-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 128K words by 16 bits per word(MX27L2048), operates from a single + 3 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM programmers may be used. The MX27L2048 supports a intelligent quick pulse programming algorithm which can result in programming times of less than one minute.

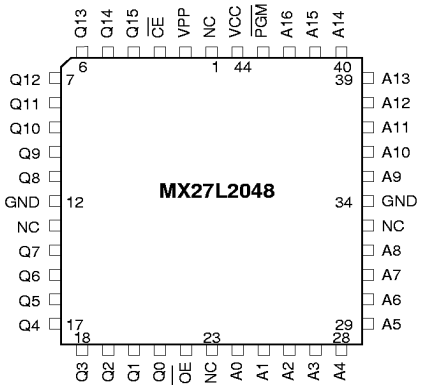
This EPROM is packaged in industry standard 40 pin dual-in-line ceramic packages or 40 pin plastic packages, 44-lead PLCC, 40-leaad TSOP(I).

PIN CONFIGURATIONS

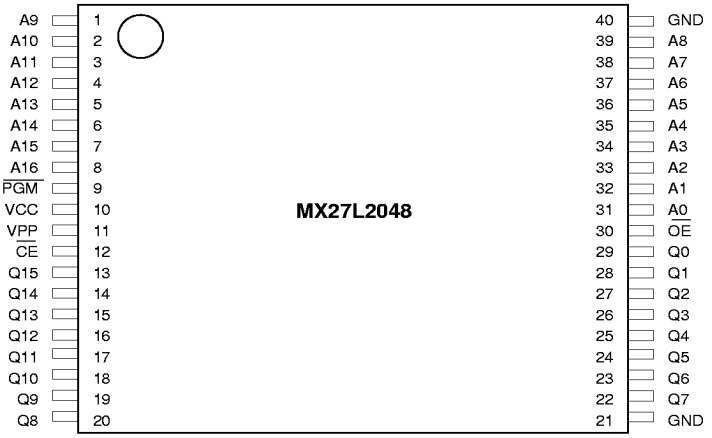
CDIP/PDIP



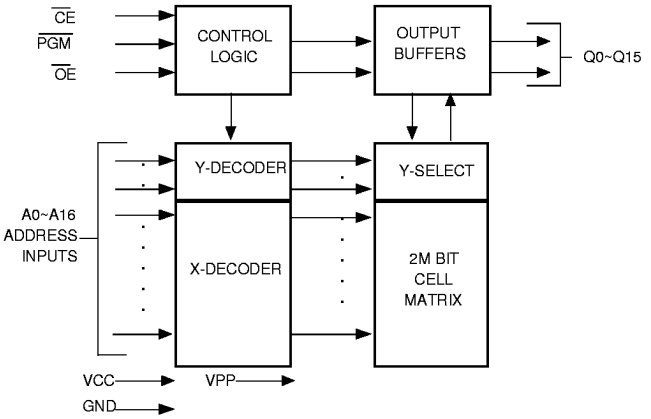
PLCC



10 x 40mm 40-TSOP(I)



BLOCK DIAGRAM



PIN DESCRIPTION(MX27C2048)

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q15	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Enable Input
VPP	Program Supply Voltage
VCC	Power Supply Pin (+5V)
GND	Ground Pin

FUNCTIONAL DESCRIPTION

THE ERASURE OF THE MX27L2048

The MX27L2048 is erased by exposing the chip to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase a MX27L2048. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm^2 for 15 to 20 minutes. The MX27L2048 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MX27L2048, and similar devices, will be cleared for all bits of their programmed states with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than that with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MX27L2048 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

THE PROGRAMMING OF THE MX27L2048

When the MX27L2048 is delivered, or it is erased, the chip has all 2M bits in the "ONE", or HIGH state. "ZEROs" are loaded into the MX27L2048 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.5V is applied to the VPP pin, $\overline{OE}$ is at VIH and $\overline{PGM}$ is at VIL.

For programming, the data to be programmed is applied with 16 bits in parallel to the data pins.

The flowchart in Figure 1 shows MXIC's interactive algorithm. Interactive algorithm reduces programming time by using short programming pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data is not verified, additional pulses are given until it is verified or the maximum is reached. This process is repeated while sequencing through each address of the MX27L2048. This part of the algorithm is done at VCC = 6.0V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the interactive programming is completed, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at VCC = 5V ± 10%.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage VPP = 12.75V is applied, with VCC = 6.25 V and $\overline{PGM}$ = VIH (Algorithm is shown in Figure 2). The programming is achieved by applying a single TTL low level 100μs pulse to the $\overline{PGM}$ input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = VPP = 5V ± 10%.

PROGRAM INHIBIT MODE

Programming of multiple MX27L2048's in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX27L2048 may be common. A TTL low-level program pulse applied to an MX27L2048 $\overline{CE}$ input with VPP = 12.5 ± 0.5 V will program the MX27L2048. A high-level $\overline{CE}$ input inhibits the other MX27L2048s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{OE}$ and $\overline{CE}$, at VIL, and VPP at its programming voltage.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the MX27L2048.

To activate this mode, the programming equipment must

force 12.0 ± 0.5 V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27L2048, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ15) defined as the parity bit.

READ MODE

The MX27L2048 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$'s, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - t OE.

WORD-WIDE MODE

With BYTE/VPP at VCC ± 0.2V outputs Q0-7 present data D0-7 and outputs Q8-15 present data D8-15, after $\overline{CE}$ and $\overline{OE}$ are appropriately enabled.

BYTE-WIDE MODE

With $\overline{BYTE}$/VPP at GND ± 0.2V, outputs Q8-15 are tri-stated. If Q15/A-1 = VIH, outputs Q0-7 present data bits D8-15. If Q15/A-1 = VIL, outputs Q0-7 present data bits D0-7.

STANDBY MODE

The MX27L2048 has a CMOS standby mode which reduces the maximum VCC current to 20 μA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.3 V. The MX27L2048 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between Vcc and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

	PINS						
MODE	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	VPP	OUTPUTS
Read	VIL	VIL	VIH	X	X	VCC	DOUT
Output Disable	VIL	VIH	VIH	X	X	VCC	High Z
Standby (TTL)	VIH	X	X	X	X	VCC	High Z
Standby (CMOS)	VCC±0.3V	X	X	X	X	VCC	High Z
Program	VIL	VIH	VIL	X	X	VPP	DIN
Program Verify	VIL	VIL	VIH	X	X	VPP	DOUT
Program Inhibit	VIH	X	X	X	X	VPP	High Z
Manufacturer Code	VIL	VIL	X	VIL	VH	VCC	00C2H
Device Code	VIL	VIL	X	VIH	VH	VCC	0122H

NOTES: 1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL(For auto select)
3. A1 - A8 = A10 - A16 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltage during programming.

FIGURE 1. INTERACTIVE PROGRAMMING FLOW CHART

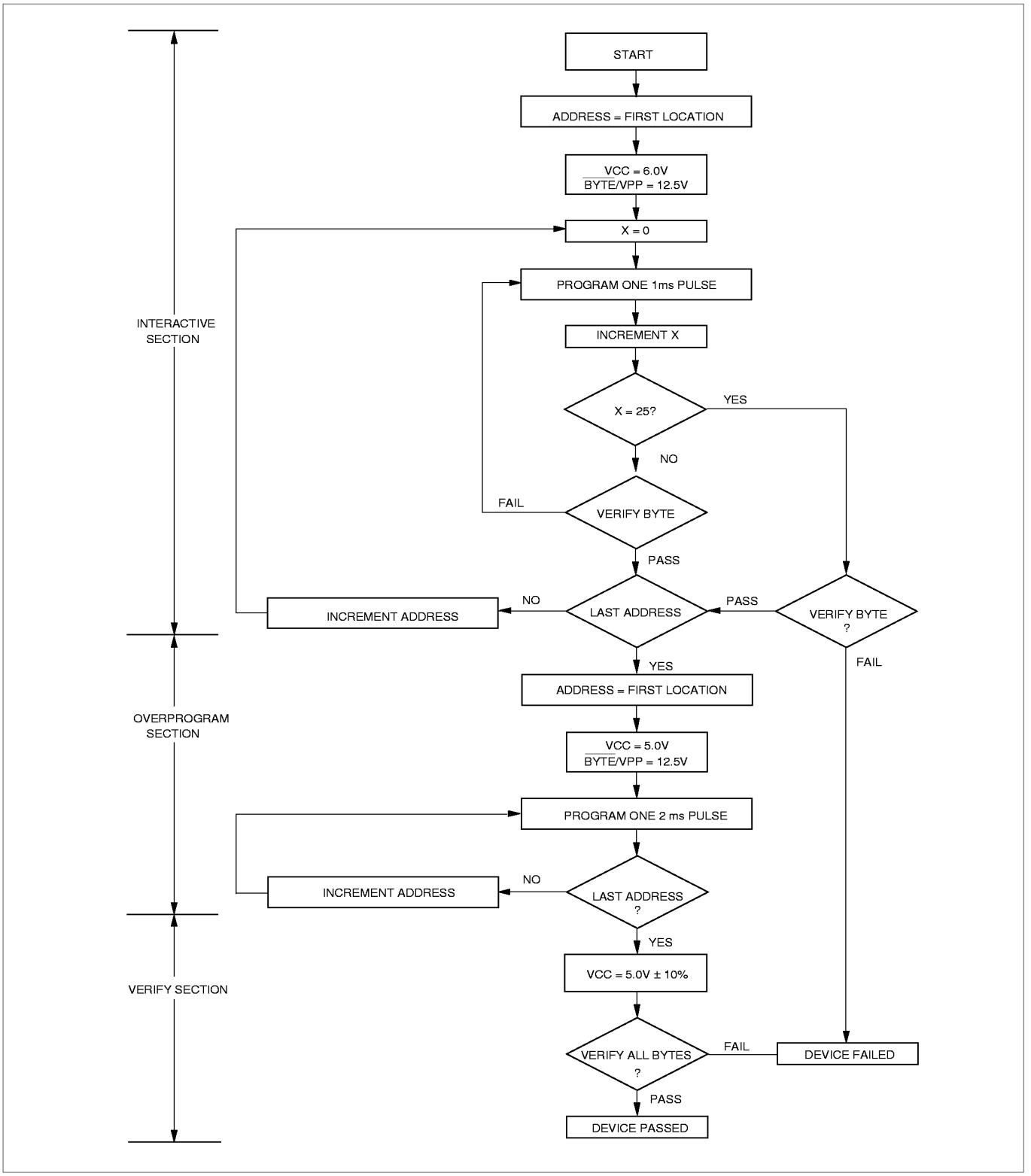
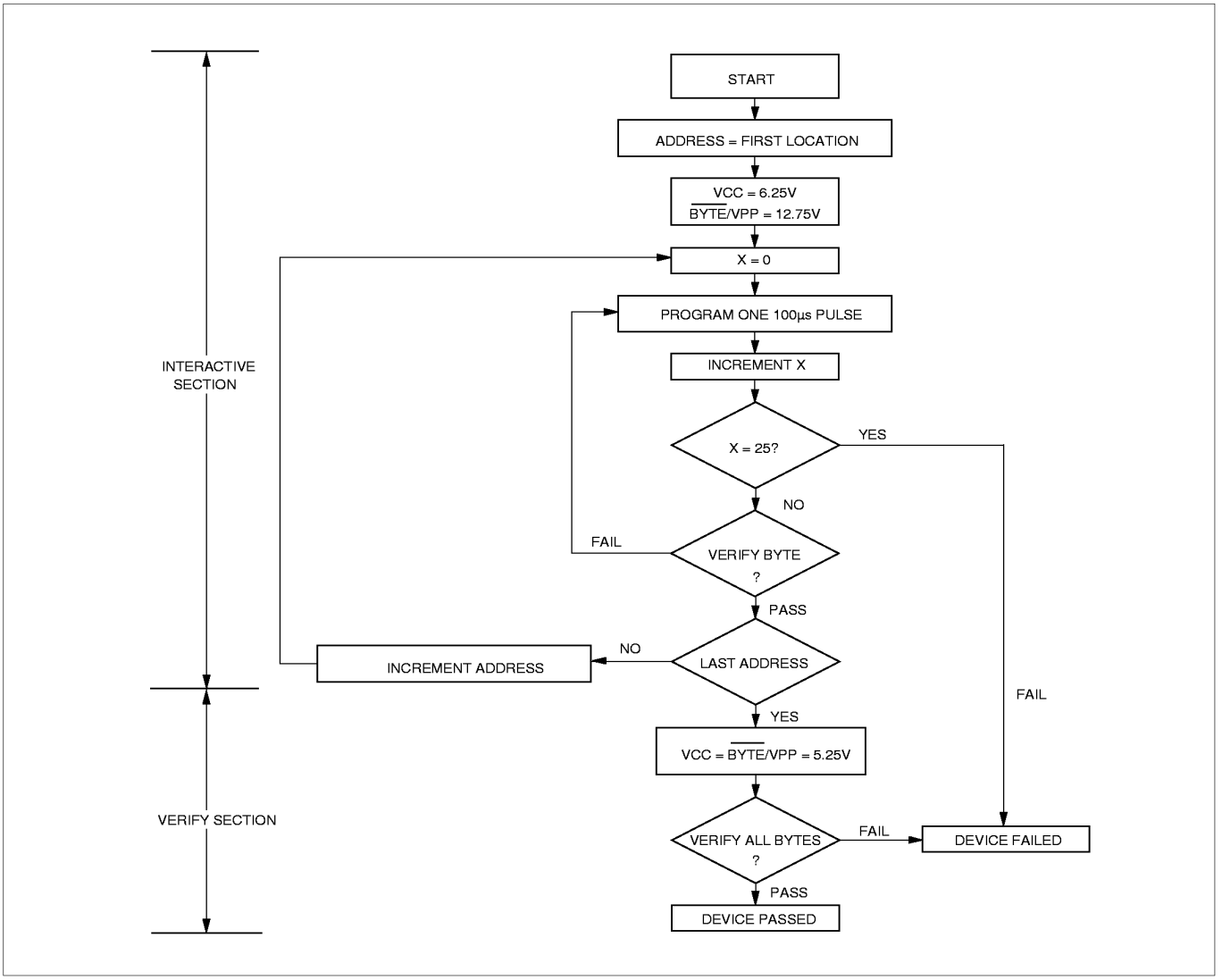
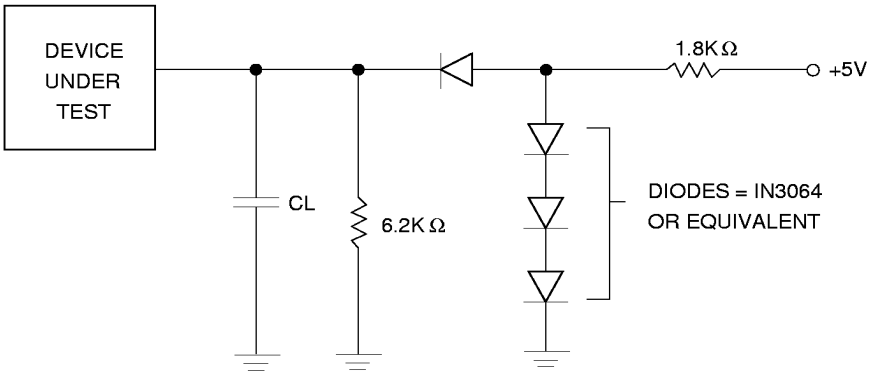


FIGURE 2. FAST PROGRAMMING FLOW CHART

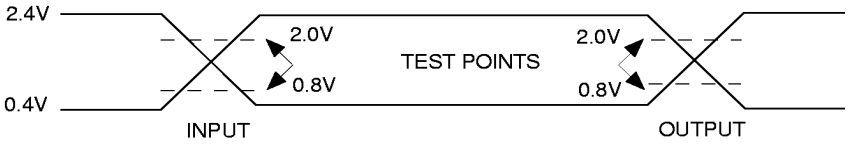


SWITCHING TEST CIRCUITS



CL = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0".
Input pulse rise and fall times are <20ns.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & Vpp	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC =2.7 ~ 3.6V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA, VCC=3.0V
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA, VCC=3.0V
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	2.7V < VCC < 3.6V
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 3.6V
ILO	Output Leakage Current	-10	10	µA	$\overline{VOUT}$ = 0 to 3.6V
ICC3	VCC Power-Down Current		20	µA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		0.25	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		20	mA	$\overline{CE}$ = VIL, f=5MHz, Iout = 0mA, VCC=3.6V
IPP	VPP Supply Current Read		100	µA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = VCC

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 2.7 ~ 3.6V

		27L2048-15		27L2048-20		27L2048-25			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		150		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		150		200		250	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		70		100		120	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	50	0	60	0	70	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		ns	

DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

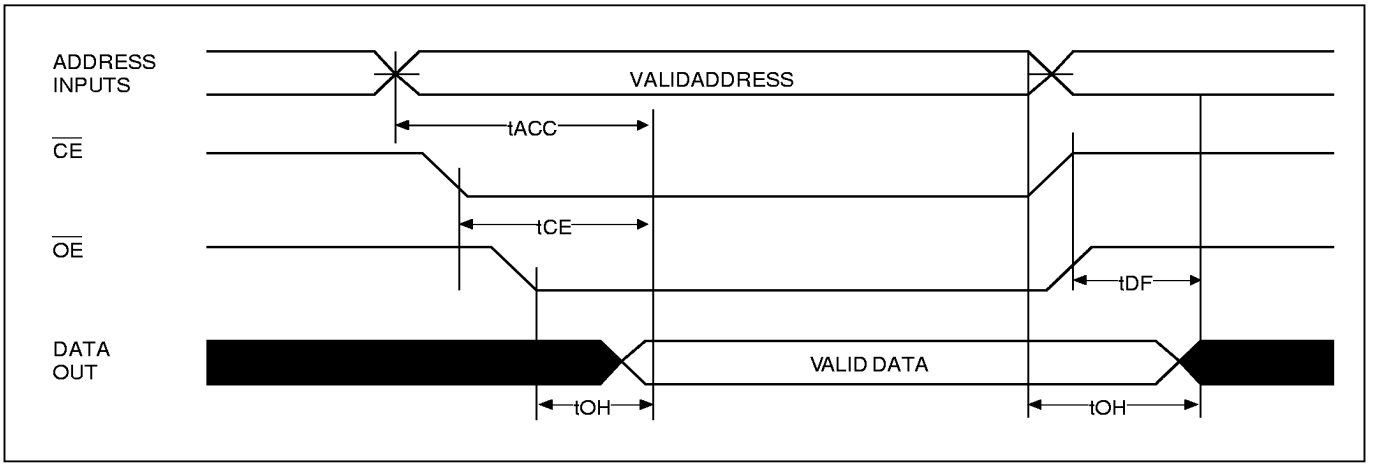
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 3.6V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program & Verify)		50	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH
VCC1	Interactive Supply Voltage	5.75	6.25	V	
VPP1	Interactive Programming Voltage	12.0	13.0	V	
VCC2	Fast Programming Supply Voltage	6.00	6.50	V	
VPP2	Fast Programming Voltage	12.5	13.0	V	

AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

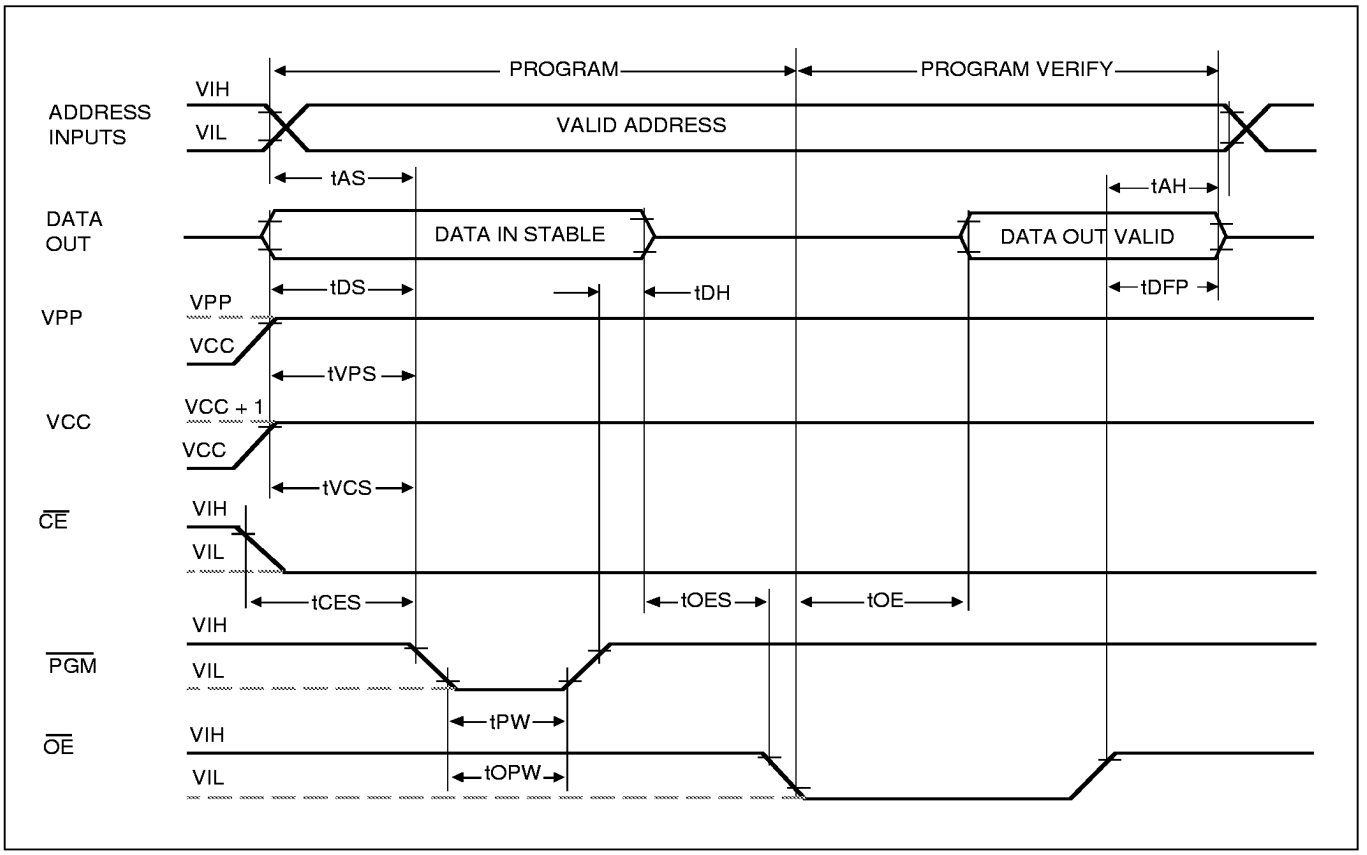
SYMBOL	PARAMETER		MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time		2.0		µS	
tOES	$\overline{OE}$ Setup Time		2.0		µS	
tDS	Data Setup Time		2.0		µS	
tAH	Address Hold Time		0		µS	
tDH	Data Hold Time		2.0		µS	
tDFP	$\overline{CE}$ to Output Float Delay		0	130	nS	
tVPS	VPP Setup Time		2.0		µS	
tPW	$\overline{CE}$ Program Pulse Width	*Fast*	95	105	µS	
		Interactive	0.95	1.05	mS	
tOPW	$\overline{CE}$ Overprogram Pulse(Interactive)		1.95	2.05	mS	
tVCS	VCC Setup Time		2.0		µS	
tDV	Data Valid from $\overline{CE}$			250	nS	
tCES	$\overline{CE}$ Setup Time		2.0		µS	
tOE	Data valid from $\overline{OE}$			150	nS	

WAVEFORMS(MX27C2048)

READ CYCLE

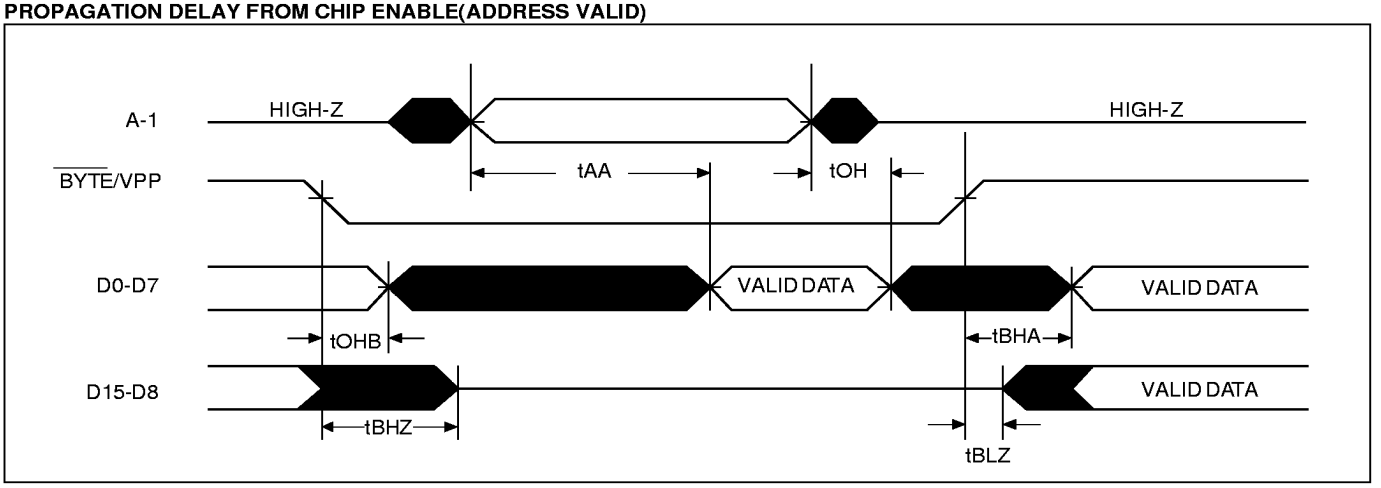


INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS

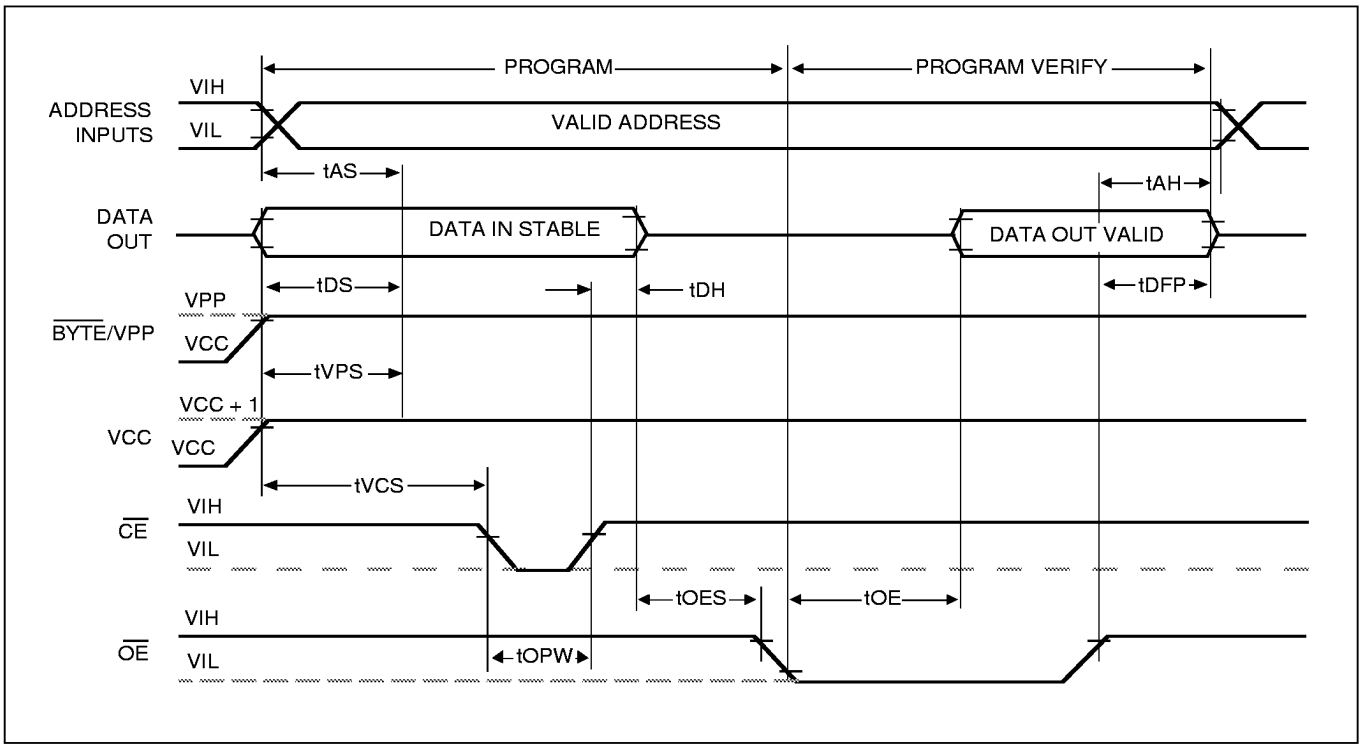


WAVEFORMS(MX27C2100)

PROPAGATION DELAY FROM CHIP ENABLE(ADDRESS VALID)



INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS



ORDERING INFORMATION

CERAMIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX27L2048DC-15	150	20	20	40 Pin DIP(JEDEC pin out)
MX27L2048DC-20	200	20	20	40 Pin DIP(JEDEC pin out)
MX27L2048DC-25	250	20	20	40 Pin DIP(JEDEC pin out)

PLASTIC PACKAGE

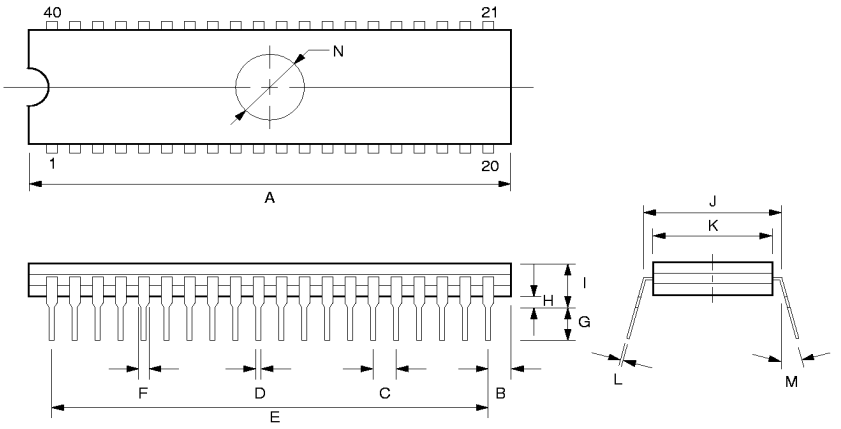
PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX27L2048PC-15	150	20	20	40 Pin DIP(JEDEC pin out)
MX27L2048PC-20	200	20	20	40 Pin DIP(JEDEC pin out)
MX27L2048PC-25	250	20	20	40 Pin DIP(JEDEC pin out)
MX27L2048QC-15	150	20	20	44 Pin PLCC
MX27L2048QC-20	2000	20	20	44 Pin PLCC
MX27L2048QC-25	250	20	20	44 Pin PLCC
MX27l2048TC-15	150	20	20	40 Pin TSOP(I)
MX27L2048TC-20	200	20	20	40 Pin TSOP(I)
MX27L2048TC-25	250	20	20	40 Pin TSOP(I)

PACKAGE INFORMATION

40-PIN CERDIP(MSI) WITH WINDOW(600 mil)

ITEM	MILLIMETERS	INCHES
A	53.34 max.	2.100 max.
B	1.85 ± .30	.073 ± .012
C	2.54 [TP]	.100 [TP]
D	.46 ± .05	.018 ± .002
E	48.22	1.900
F	1.40 ± .05	.055 ± .002
G	3.43 ± .38	.135 ± .015
H	.94 ± .41	.037 ± .016
I	5.00	.197
J	15.51 ± .08	.611 ± .003
K	14.82 ± .38	.584 ± .015
L	.25 ± .13	.010 ± .005
M	0~15°	0~15°
N	ϕ9.64	ϕ.380

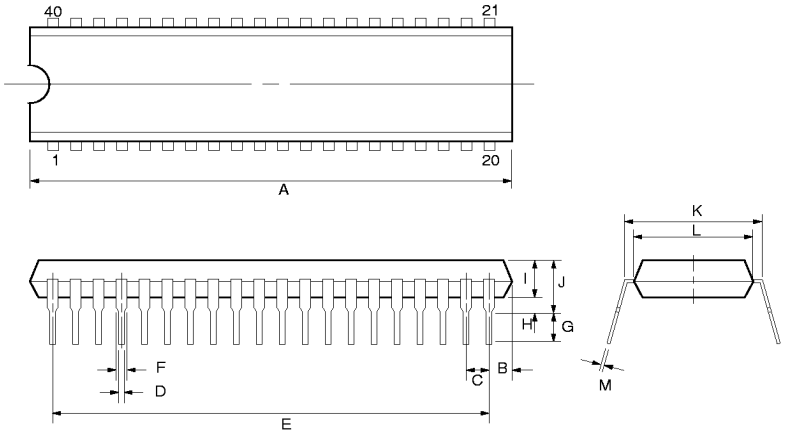
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



40-PIN PLASTIC DIP(600 mil)

ITEM	MILLIMETERS	INCHES
A	52.54 max.	2.070 max.
B	2.03 [REF]	.080 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	48.22	1.900
F	1.52 [Typ.]	.060 [Typ.]
G	3.30 ± .25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.91 ± .25	.154 ± .010
J	4.42 ± .25	.174 ± .010
K	15.22 ± .25	.600 ± .010
L	13.76 ± .25	.542 ± .010
M	.25 [Typ.]	.010 [Typ.]

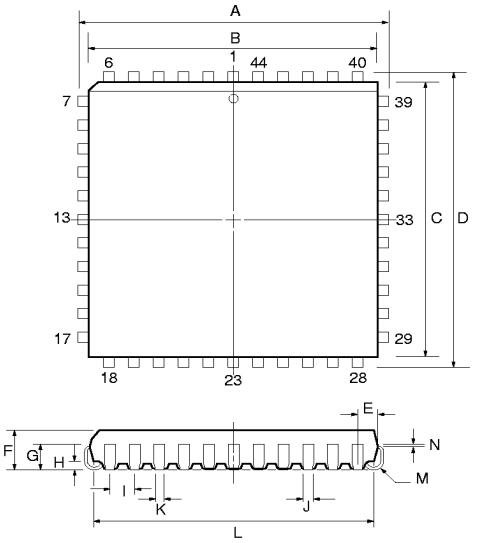
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



PACKAGE INFORMATION

44-PIN PLASTIC LEADED CHIP CARRIER(PLCC)

ITEM	MILLIMETERS	INCHES
A	17.53 ± .12	.690 ± .005
B	16.59 ± .12	.653 ± .005
C	16.59 ± .12	.653 ± .005
D	17.53 ± .12	.690 ± .005
E	1.95	.077
F	4.70 max.	.185 max
G	2.55 ± .25	.100 ± .010
H	.51 min.	.020 min.
I	1.27 [Typ.]	.050 [Typ.]
J	.71 ± .10	.028 ± .004
K	.46 ± .10	.018 ± .004
L	15.50 ± .51	.610 ± .020
M	.63 R	.025 R
N	.25 [Typ.]	.010 [Typ.]



40-PIN PLASTIC TSOP

ITEM	MILLIMETERS	INCHES
A	14.0 ± .20	0.551 ± .008
B	12.4 ± .10	0.488 ± .004
C	10.1 max.	0.398 max.
D	0.125 [Typ.]	0.005 [Typ.]
E	.80 [Typ.]	.031 [Typ.]
F	.20 ±.10	.008 ± .004
G	.30 ± .10	.012 ± .004
H	.50 [Typ.]	.020[Typ.]
I	.45 max.	0.18 max.
J	0 ~.20	0 ~ .008
K	1.00 ± .10	.039 ± .004
L	1.2 max.	0.047 max.
M	.50	.020
N	0 ~ 10°	0 ~ 10°

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.