STPC® VEGA

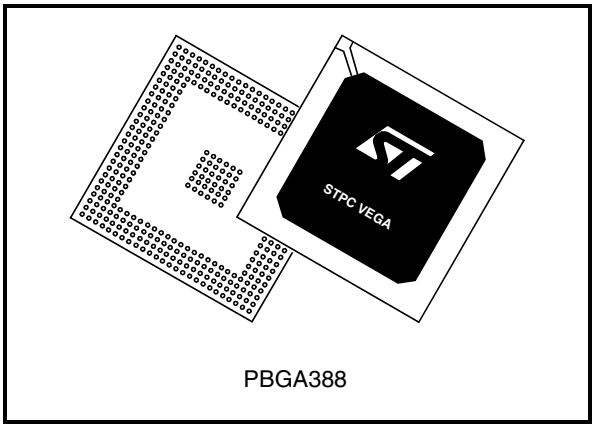
X86 CORE PC COMPATIBLE SOC with ETHERNET and USB

PRELIMINARY DATA

- PENTIUM® II CLASS PROCESSOR CORE
- 64-BIT SDRAM CONTROLLER RUNNING AT UP TO 100 MHZ
- PCI 2.1 COMPLIANT MASTER/SLAVE CONTROLLER
- ISA MASTER / SLAVE
- DUAL PORT USB HOST CONTROLLER (OHCI)
- 10/100 ETHERNET MAC [1)]
- INTEGRATED PERIPHERAL CONTROLLER WITH SUPPPORT FOR EXTERNAL RTC
- ULTRA DMA-66 IDE CONTROLLER
- POWER MANAGEMENT UNIT
- 16-BIT LOCAL BUS INTERFACE
- I2C BUS CONTROLLER
- UART (1 RxTx)
- IEEE 1149.1 JTAG INTERFACE
- 8 GENERAL PURPOSE IO
- PROGRAMMABLE CLOCKS
- 0.18 MICRON TECHNOLOGY
- 1.8 V CORE & 3.3 V I/Os
- LOW POWER CONSUMPTION DEVICE

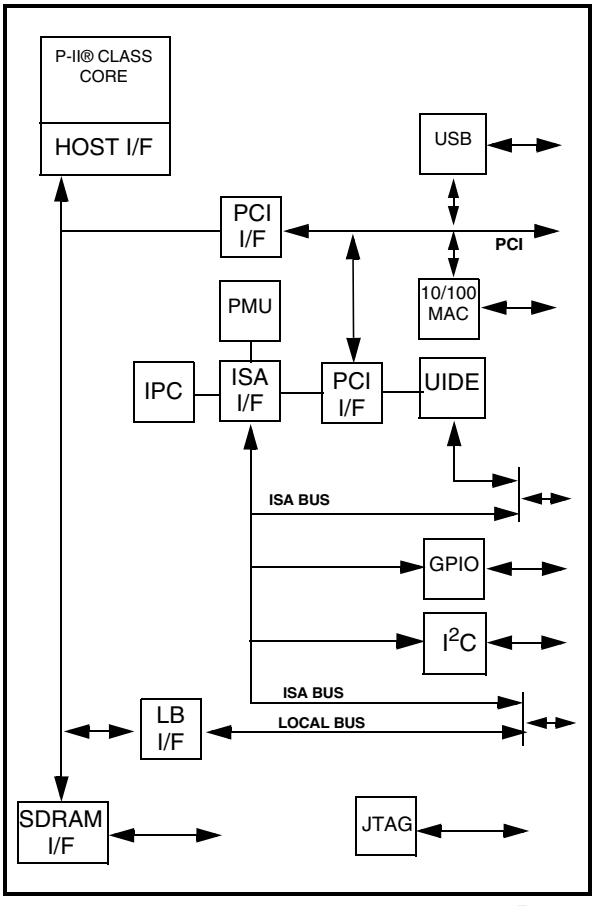
DESCRIPTION

The STPC VEGA integrates a fully static Pentium® II® Class processor, fully compatible with Industry Standards, and combines it with a powerful chipset to provide a general purpose PC compatible subsystem on a single device. The device is packaged in a 388 Ball Grid Array (PBGA).



PBGA388

Block Diagram



1- The usage of the internal MAC 10/100 is very restricted. For more information see 10/100 Ethernet Controller description.

Rev. 1

Table of Contents

Table of Contents

- **X86 Processor**
- x86 Pentium® II class processor running in X2 mode
  -3 Issue integer six-stage pipeline/clock
  -3 issue MMX®/clock
  -Pipelined FPU
- Bus clock with skew correction
- Internal core clocks generated as multiples of bus clock with multiplication factors of X2, X2.5, X3, X3.5

- **SDRAM Interface**
- 64-bit data bus
- 100 MHz maximum SDRAM clock
- 8 MByte to 256 MByte memory size (only the upper 128MByte cacheable)
- Supports 16 Mbit to 256 Mbit memories
- Support for -8 to -15 memory parts
- Supports buffered and non-buffered DIMMs
- Supports registered DIMMs
- Programmable latency

- **PCI Controller Master/Slave**
- Compatible with PCI Version 2.1 specification
- Integrated PCI arbitration interface. Up to three external masters can be directly connected
- Master/Slave Bridge to USB, LAN, UIDE & ISA cycles
- Support for burst read/write from PCI master
- 0.20X, 0.25X, 0.33X and 0.5X Host clock PCI clock. Automatically selected.

- **ISA Master/Slave**
- Generates the ISA clock from either 14.318 MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles
- Fast Gate A20 and Fast reset
- Supports Flash ROM
- Supports ISA hidden refresh
- Buffered DMA and ISA master cycles to reduce the bandwidth utilization of PCI and system bus

- **Local Bus**
- Multiplexed with ISA interface
- 16-bit bus data path with word steering capability
- Two cacheable banks of 32 Mbyte flash devices (boot block shadowed from 000C0000h to 000FFFFFh)
- Programmable timing with host clock granularity for flash accesses
- 32-bit flash burst support
- Two-level hardware key protection for flash boot block protection
- Up to eight IO devices (four Chipselects) supported with programmable start address & size
- IO device timing (setup & recovery time) programmable

- **Integrated Peripherals Controller**
- Interrupt Controller: 8259 compatible (two Interrupt controllers)
- DMA Controller: 8237 compatible (two DMA controllers)
- Page register
- Counter 0 and counter 1 gates are always on, counter 2 is controlled by writing to Port B
- Supports external RTC

- **Ultra DMA-66 IDE Controller**
- Supports IDE hard drives larger than 528 MBytes
- Support for two connectors to allow up to four drives
- Support for CD-ROM and tape peripherals
- Support for 11.1/16.6 Mbytes/second, I/O Channel Ready PIO data transfers
- Supports up to 66 Mbytes/second, UDMA data transfers
- Ultra DMA supports CRC-16 error checking protocol (no correction supported)
- PIO: 0 to 5, DMA: 0 to 2, UDMA: 0 to 4

- Backward compatibility with IDE (ATA-1)

- **8 GPIO**
- Individual pins programmable as either input or output
- Interrupt generation with selectable masking

■ **10/100 Ethernet Controller**

The usage of VEGA internal MAC is very restricted and tested only under Linux operating system with the specific configuration 100Mb/s Half and Full Duplex . Any other functional configuration is not guaranteed by STMicroelectronics.

Problem that maybe occur is a file transfer corruption , however the use of the internal MAC for browsing applications or http session does not causes problem.

- Compliant with IEEE 802.3, 802.3u specification
- Supports 10/100 Mb/s data transfer rates
- IEEE 802.3 compliant MII interface to talk to an external physical layer (PHY)
- VLAN support
- Supports both full-duplex and half-duplex operations
- Supports CSMA/CD Protocol for half-duplex
- Supports flow-control for full-duplex operation
- Collision detection and auto retransmission on collisions in half-duplex mode
- Management support using a variety of counters
- Preamble generation and removal
- Automatic 32-bit CRC generation and checking
- Optional insertion of PAD/CRC32 on transmit
- Options for Automatic Pad stripping on the receive packets
- Provides external and internal loop back capability on the MII Interface
- Contains a variety of flexible address filtering modes on the Ethernet side:
  - One 48-bit Perfect address
  - 64 hash-filtered multicast addresses
  - Pass all multicast addresses
  - Promiscuous Mode
  - Pass all incoming packets with a status report

■ **USB Host Controller**
- Open HCI Rev 1.1 compatible
- USB Rev 1.1 compatible
- Root hub with two down-stream ports with power switching control
- Support of both low & high speed USB devices
- Support of system management interupt (SMI)

■ **UART**
- One UART RxTx only
- Programmable word length, stop bits and parity
- Programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Scratch register
- Two 16-byte FIFOs

■ **Power Management Unit**
- Four power saving modes: On, Doze, Standby, Suspend
- Programmable system activity detector
- Supports STPCLK#

■ **I2C Bus Controller**
- One I2C compliant master/slave bus controller
- Slow and fast modes supported

■ **JTAG Function**
- Boundary Scan Chain function

1 INTRODUCTION

At the heart of the STPC Vega is an advanced processor block that includes a powerful PENTIUM® II CLASS processor core along with a 64-bit SDRAM controller, a high speed PCI local-bus controller and Industry standard PC chip set functions (Interrupt controller, U-DMA Controller, Interval timer and ISA bus) and U-IDE controller.

The processor bus runs at the speed of half the processor speed (x2 mode) or x3 or x3.5 modes.

The STMicroelectronics PENTIUM® II CLASS processor core is embedded with standard and application specific peripheral modules on the same silicon die. The core has all the functionality of the Intel™ standard PENTIUM® II CLASS processor products, including the low power System Management Mode (SMM).

System Management Mode (SMM) provides an additional interrupt and address space that can be used for system power management or software transparent emulation of peripherals. While running in isolated SMM address space, the SMM interrupt routine can execute without interfering with the operating system or application programs.

The 'standard' PC chipset functions (DMA, interrupt controller, timers, power management logic) are integrated with the PENTIUM® II CLASS processor core.

The PCI bus is the main data communication link to the STPC Vega chip. The STPC Vega translates appropriate host bus I/O and Memory cycles onto the PCI bus. It also supports generation of Configuration cycles on the PCI bus. The STPC Vega, as a PCI bus agent (host bridge class), fully complies with PCI specification 2.1. The chip-set also implements the PCI mandatory header registers in Type 0 PCI configuration space for easy porting of PCI aware system BIOS. The device contains a PCI arbitration function for three external PCI devices.

The STPC Vega integrates an ISA bus controller. Peripheral modules such as parallel and serial communications ports, keyboard controllers and additional ISA devices can be accessed by the STPC Vega chip set through this bus.

An industry standard U-IDE (ATA 2) controller is built in to the STPC Vega and connected internally via the PCI bus.

The General Purpose Input/Output (GPIO) interface provides an 8-bit I/O facility, using 8 dedicated device pins. It is organised using one 8-bit Register.
Each GPIO port can be configured as an input or an output simply by programming the associated port direction control register. All GPIO ports are configured as inputs at reset, which also latches the input levels into the Strap Registers. The input states of the ports are thus recorded automatically at reset, and this can be used as a strap register anywhere in the system.

1.1 MEMORY CONTROLLER

The STPC Vega handles the memory data (DATA) bus directly, controlling up to 256 MBytes. The SDRAM controller supports accesses to the Memory Banks to/from the CPU (via the host). Parity is not supported.

The SDRAM controller only supports 64 bit wide Memory Banks.

Four Memory Banks (if DIMMS are used; Single sided or two double-sided DIMMs) are supported in the following configurations (see Table 1-1.)

Table 1-1. Memory configurations

Memory Bank size	Number	Organisation	Device Size
1Mx64	4	1Mx16	16Mbits
2Mx64	8	2Mx8	
4Mx64	16	4Mx4	
4Mx64	4	2Mx16x2	64Mbits
8Mx64	8	4Mx8x2	
16Mx64	16	8Mx4x2	
2Mx64	2	500Kx32x4	
4Mx64	4	1Mx16x4	
8Mx64	8	2Mx8x4	
16Mx64	16	4Mx4x4	
4Mx64	2	1Mx32x4	128Mbits
8Mx64	4	2Mx16x4	
16Mx64	8	4Mx8x4	
32Mx64	16	8Mx4x4	
8Mx64	2	2Mx32x4	256MBits
16Mx64	4	2Mx16x4	
32Mx64	8	2Mx8x4	

The SDRAM Controller supports buffered or unbuffered SDRAM but not EDO or FPM modes. SDRAMs must support Full Page Mode Type access.

The STPC Memory Controller provides various programmable SDRAM parameters to allow the SDRAM interface to be optimized for different processor bus speeds, SDRAM speed grades and CAS Latency.

1.2 FEATURE MULTIPLEXING

The STPC Vega BGA package has 388 balls. This however is not sufficient for all of the integrated functions available; some features therefore share the same balls and cannot thus be used at the same time. The STPC Vega configuration is done by 'strap options'. This is a set of pull-up or pull-down resistors (see Section 3 for more details), checked on reset, which auto-configure the STPC Vega.

There are 2 multiplexed functions, these are the external ISA bus and the Local Bus interfaces.

1.3 POWER MANAGEMENT

The STPC Vega core is compliant with the Advanced Power Management (APM) specification to provide a standard method by which the BIOS can control the power used by personal computers. The Power Management Unit (PMU) module controls the power consumption, providing a comprehensive set of features that controls the power usage and supports compliance with the United States Environmental Protection Agency's Energy Star Computer Program. The PMU provides the following hardware structures to assist the software in managing the system power consumption:

– System Activity Detection

– 3 power-down timers detecting system inactivity:
  - Doze timer (short durations)
  - Stand-by timer (medium durations)
  - Suspend timer (long durations)

– House-keeping activity detection

– House-keeping timer to cope with short bursts of house-keeping activity while dozing or in stand-by state

– Peripheral activity detection

– Peripheral timer detecting peripheral inactivity

– SUSP# modulation to adjust the system performance in various power down states of the system including full power-on state

– Power control outputs to disable power from different planes of the board

Lack of system activity for progressively longer periods of time is detected by the three power down timers. These timers can generate SMI interrupts to CPU so that the SMM software can put the system in decreasing states of power consumption. Alternatively, system activity in a power down state can generate an SMI interrupt to allow the software to bring the system back up to full power-on state. The chip-set supports up to three power down states described above; these correspond to decreasing levels of power savings.

Power down puts the STPC Vega into suspend mode. The processor completes execution of the current instruction, any pending decoded instructions and associated bus cycles. During suspend mode, internal clocks are stopped. Removing power-down, the processor resumes instruction fetching and begins execution in the instruction stream at the point it had stopped. Because of the static nature of the core, no internal data is lost.

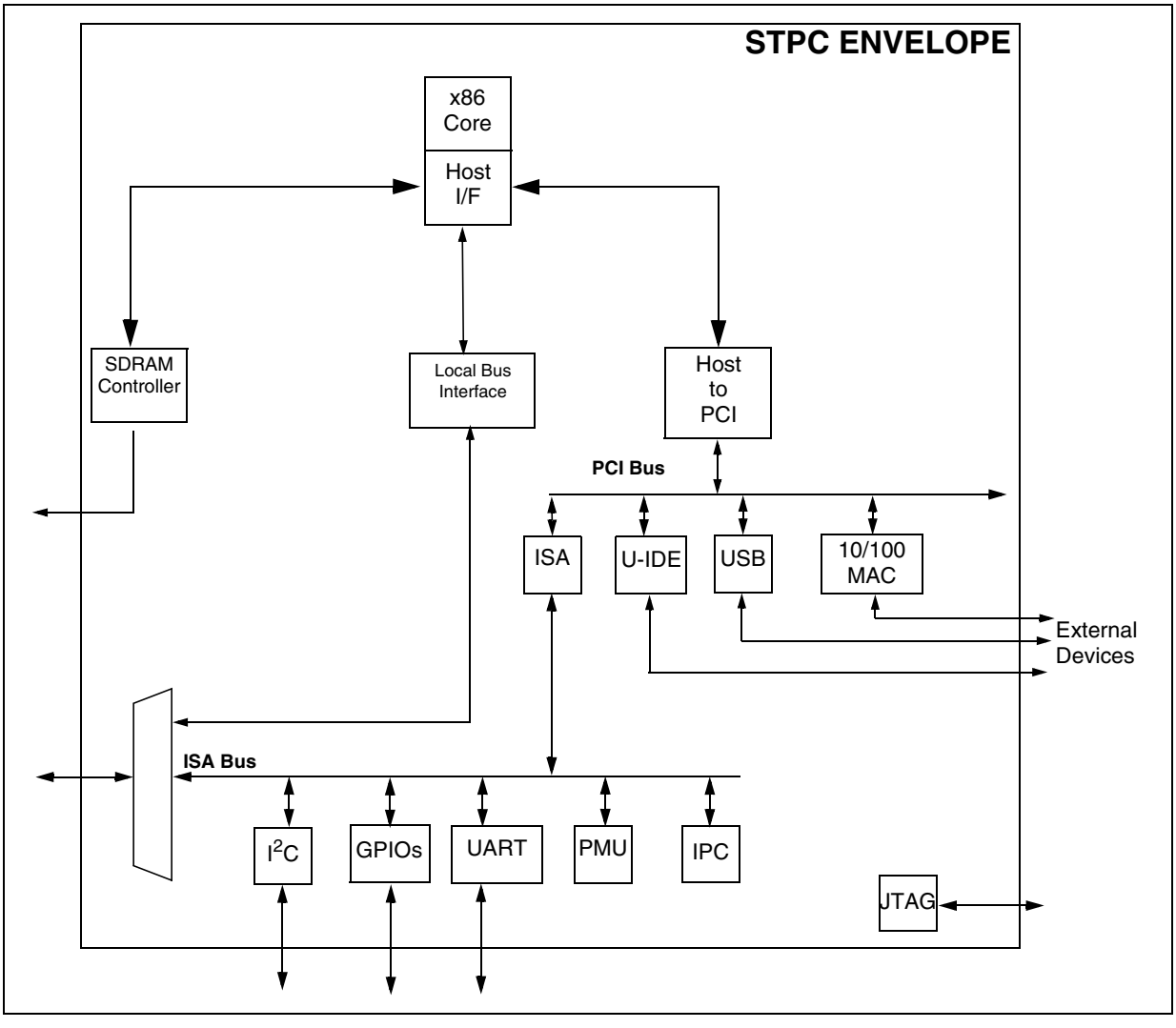
1.4 JTAG

JTAG stands for Joint Test Action Group and is the popular name for IEEE Std. 1149.1, Standard Test Access Port and Boundary-Scan Architecture. This built-in circuitry is used to assist in the test, maintenance and support of functional circuit blocks through Boundary Scan Chain.

1.5 I^2C

The I^2C (Inter-Integrated Circuit) Controller built into the STPC Vega provides a two-wire communication link between the STPC and external integrated circuits. Master and Slave modes are available in slow and fast modes.

Figure 1-1. Functional description



1.6 CLOCK TREE

The STPC Vega integrates many features and generates all its clocks from a single 14MHz oscillator. This results in multiple clock domains as described in Figure 1-2.

The speed of the PLLs is either fixed (DEVCLK), either programmable by strap option (HCLK) either programmable by software (GPCLK, MCLK). When in synchronized mode, MCLK speed is fixed to HCLKO speed and HCLKI is generated from MCLKI.

Figure 1-2. STPC Vega clock architecture

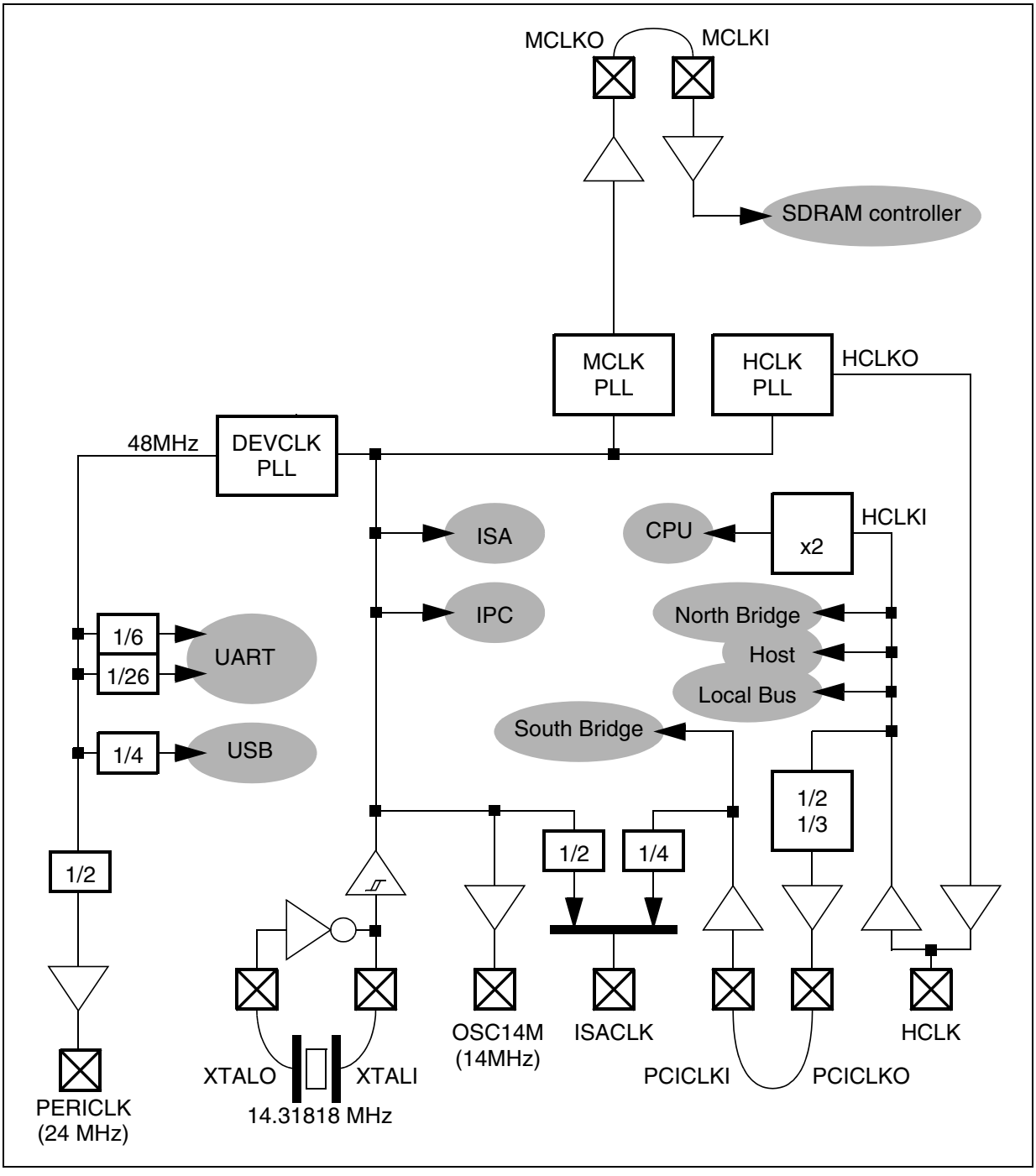
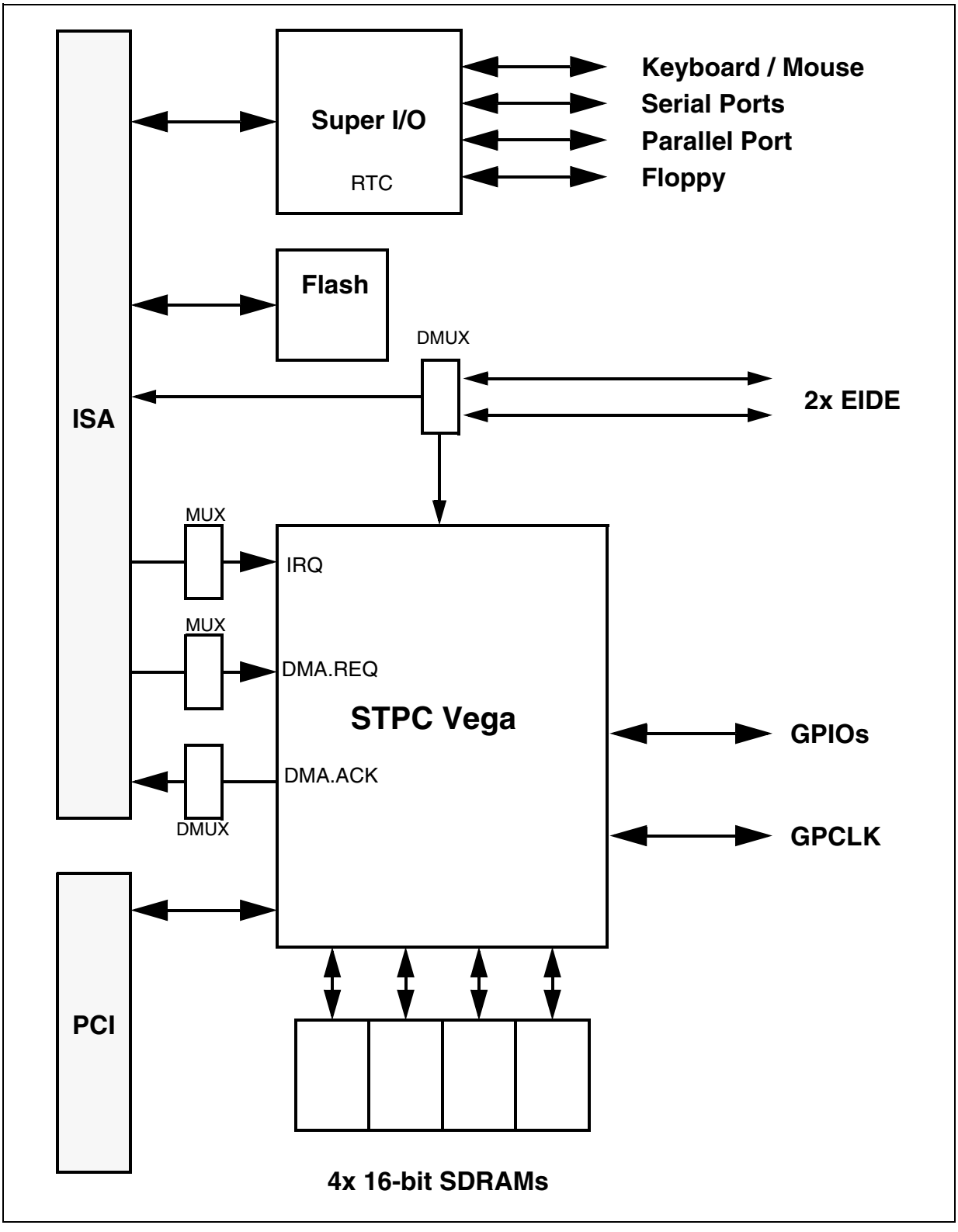


Figure 1-3. Typical ISA-based Application.



2 PIN DESCRIPTION

2.1 INTRODUCTION

The STPC Vega integrates most of the functionalities of the PC architecture. As a result, many of the traditional interconnections between the host PC microprocessor and the peripheral devices are totally internal to the STPC Vega. This offers improved performance due to the tight coupling of the processor core and these peripherals. As a result many of the external pin connections are made directly to the on-chip peripheral functions.

Table 2-1 describes the physical implementation listing signal type and functionality. Table 2-2 provides a full pin listing and pin descriptions. Table 2-6 provides a full listing of the STPC Vega package physical pin connections.

Note: Several interface pins are multiplexed with other functions. Refer to Table 2-4 and Table 2-5 for further details.

Table 2-1. Signal Description

Group name	Qty	
Basic Clocks, Reset & Xtal		8
Memory Interface		93
PCI Interface		57
ISA	65	86
UIDE	10	
Local Bus	50	
Analog (PLL) GND		4
Analog (PLL) V_{DD}		5
GPIO		8
Ethernet MAC (Media Access Controller)		17
USB		6
UART		2
I^2C		2
JTAG		4
V_{DD} 1.8 V		4
V_{DD} 3.3 V		12
GND		68
Unconnected		9
Misc		3
Total Pin Count		388

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[2]	Description	Qty
BASIC CLOCKS AND RESETS				
SYSRSETI#	I	SCHMITT_FT	System Power Good Input	1
SYSRSTO#	O	BT8TRP_TC	System Reset Output	1
XTALI	I	OSCI13B	14.318 MHz Crystal Input External Oscillator Input	1
XTALO	I/O		14.318 MHz Crystal Output	1
HCLK	I/O	BD4STRP_FT	Host Clock (Test)	1
DEV_CLK	O	BT8TRP_TC	Peripheral Clock	1
POWER SUPPLIES				
VDD			3.3V Power Supply for I/O Pads	12
VDD_CORE			1.8V Core Power Supply	4
VDD33_CPUCLK_PLL			3.3V Power Supply for CPU PLL Clock	1
VDD18_CPUCLK_PLL			1.8V Power Supply for CPU PLL Clock	1
V_{DD}_xxx_PLL			3.3V Power Supply for PLL Clocks	3
VSS_xxx_PLL			Ground Plane for PLL Clocks	4
GND			Digital Ground Plane	68
MEMORY INTERFACE				
MCLKI	I	TLCHT_TC	Memory Clock Input	1
MCLKO	O	BT8TRP_TC	Memory Clock Output	1
CS#[1:0]	O	DB8STRP_TC	Bank Chip Select	2
MA[10:0]	O	BD16STARUQP_TC	Memory Row & Column Address	1
MA[11]/CS#[2]	O	BD16STARUQP_TC	Bank Chip Select / Memory Address	1
MA[12]	O	BD16STARUQP_TC	Memory Row & Column Address	1
BA[0]	O	BD16STARUQP_TC	Bank Address	1
BA[1]/CS#[3]	O	BD16STARUQP_TC	Bank Address / Bank Chip Select	1
RAS#[1:0]	O	BD16STARUQP_TC	Row Address Strobe	2
CAS#[1:0]	O	BD16STARUQP_TC	Column Address Strobe	2
MWE#	O	BD16STARUQP_TC	Write Enable	1
DQM[7:0]	O	BT8TRP_TC	Data Input/Output Mask	8
MD[63:0]	I/O	BD8STRUQP_TC	Memory Data	64
PCI INTERFACE				
PCI_CLKI	I	TLCHT_FT	33 MHz PCI Input Clock	1
PCI_CLKO	O	BT8TRP_TC	33 MHz PCI Output Clock	1
AD[31:0]	I/O	BD8PCIARP_FT	PCI Address / Data	32
CBE[3:0]	I/O	BD8PCIARP_FT	Bus Commands / Byte Enables	4
FRAME#	I/O	BD8PCIARP_FT	Cycle Frame	1
IRDY#	I/O	BD8PCIARP_FT	Initiator Ready	1
TRDY#	I/O	BD8PCIARP_FT	Target Ready	1
LOCK#	I	TLCHT_FT	PCI Lock	1

Note[2]: See Table 2-3 for buffer type descriptions

Note[3]: These pins have a secondary role in that they are read by the device strap option registers during the rising edge of SYSRSTI#. See Section 3.1

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[2]	Description	Qty
DEVSEL#	I/O	BD8PCIARP_FT	Device Select	1
STOP#	I/O	BD8PCIARP_FT	Stop Transaction	1
PAR	I/O	BD8PCIARP_FT	Parity Signal Transactions	1
SERR#	O	BD8PCIARP_FT	System Error	1
PERR#	O	BD8PCIARP_FT	Parity Error	1
PCI_REQ#[2:0]	I	BD8PCIARP_FT	PCI Request	3
PCI_GNT#[2:0]	O	BD8PCIARP_FT	PCI Grant	3
PCI_INT#[3:0]	I	BD4STRUQP_FT	PCI Interrupt Request	4
ISA CONTROL				
ISA_CLK	O	BT8TRP_TC	ISA Clock Output Multiplexer Select Line For IPC	1
ISA_CLK2X	O	BT8TRP_TC	ISA Clock x2 Output Multiplexer Select Line For IPC	1
OSC14M	O	BT8TRP_TC	ISA bus synchronisation clock	1
LA[23:17]	O	BD8STRUQP_FT	Unlatched Address	7
SA[19:0]	I/O	BD8STRUQP_FT	Latched Address	20
SD[15:0]	I/O	BD8STRP_FT	Data Bus	16
ALE	O	BD4TRP_TC	Address Latch Enable	1
MEMR#, MEMW#	I/O	BD8STRUQP_FT	Memory Read and Memory Write	2
SMEMR#[3], SMEMW#[3]	O	BD8TRP_TC	System Memory Read and Write	2
IOR#, IOW#	I/O	BD8STRUQP_FT	I/O Read and Write	2
MCS16#, IOCS16#	I	BD4STRUQP_FT	Memory and I/O Chip Select 16	2
BHE#	O	BD8STRUQP_FT	System Bus High Enable	1
ZWS#	I	BD4STRP_FT	Zero Wait State (see Section 2.2.4)	1
REF#	O	BD8TRP_TC	Refresh Cycle.	1
MASTER#	I	BD4STRUQP_FT	Add On Card Owns Bus	1
AEN	O	BD8STRUQP_FT	Address Enable	1
IOCHCK#	I	BD4STRUQP_FT	I/O Channel Check.	1
IOCHRDY	I/O	BD8STRUQP_FT	I/O Channel Ready (ISA) Busy/Ready (IDE)	1
ISAOE#	O	BD4STRP_FT	ISA/IDE Selection	1
IRQ_MUX[3:0]	I	SCHMITT_FT	Time-Multiplexed Interrupt Request	4
DREQ_MUX[1:0]	I	BD4STRP_FT	Time-Multiplexed DMA Request	2
DACK_ENC[2:0][3]	O	BD4STRP_FT	Encoded DMA Acknowledge	3
TC[3]	O	BD4STRP_FT	ISA Terminal Count	1
RTCAS	O	BD4TRP_TC	Real Time Clock Address Strobe	1
RMRTCCS#	I/O	BD4STRP_FT	ROM/RTC Chip Select	1
KBCS#	I/O	BD4STRP_FT	Keyboard Chip Select	1
RTCRW#	I/O	BD4STRP_FT	RTC Read/Write	1
RTCDS	I/O	BD4STRP_FT	RTC Data Strobe	1

Note[2]: See Table 2-3 for buffer type descriptions

Note[3]: These pins have a secondary role in that they are read by the device strap option registers during the rising edge of SYSRSTI#. See Section 3.1

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[2]	Description	Qty
LOCAL BUS (Multiplexed Pins)				
PA[24:22][3]	O	BD4TRP_TC	Address Bus	3
PA[21:20], [8], [3:0]	O	BD4STRP_FT		7
PA[18:16], [14:12], [10], [7:4]	O	BD8STRUQP_FT		11
PA[15]	O	BD4TRP_TC		1
PA[11]	O	BD8TRP_TC		1
PA[9]	O	BD4TRP_TC		1
PD[15:0]	I/O	BD8STRP_FT	Data Bus	16
PBE#[1]	O	BD8STRP_FT	Upper Byte Enable (PD[15:8])	1
PBE#[0]	O	BD4STRUP_FT	Lower Byte Enable (PD[7:0])	1
PRD#	O	BD4STRUQP_FT	Peripheral Read Control	1
PWR#	O	BD8TRP_TC	Peripheral Write Control	1
PRDY#	I	BD8STRUQP_FT	Data Ready	1
FCS1#	O	BT8TRP_TC	Flash Chip Select	1
FCS0#	O	BD4TRP_TC		1
IOCS#[3]	O	BD4STRP_FT	I/O Chip Select	1
IOCS#[2:0]	O	BD8STRUQP_FT		3
IDE CONTROL				
DA[2:0]	O	BD8STRUQP_FT	Address Bus	3
DD[15:12]	I/O	BD4STRP_FT	Data Bus	4
DD[11:0]	I/O	BD8STRUQP_FT		12
PCS3#,PCS1#,SCS3#,SCS1#	O	BD8STRUQP_FT	Primary & Secondary Chip Selects	4
DIORDY	O	BD8STRUQP_FT	Data I/O Ready	1
PIRQ, SIRQ	I	SCHMITT_FT	Primary & Secondary Interrupt Request	2
PDRQ	I	SCHMITT_FT	Primary DMA Request	1
SDRQ	I	BD4STRP_FT	Secondary DMA Request	1
PDACK#, SDACK#	O	BD8STRP_TC	Primary & Secondary DMA Acknowledge	2
PDIOR#, SDIOR#	O	BD8STRP_TC	Primary & Secondary I/O Channel Read	2
PDIOW#, SDIOW#	O	BD8STRP_TC	Primary & Secondary I/O Channel Write	2
USB INTERFACE				
OC	I	TLCHTU_TC	Over Current Detect	1
USBDPLS[0], USBDMNS[0]	I/O	USBDS	Universal Serial Bus Port 0	2
USBDPLS[1], USBDMNS[1]	I/O	USBDS	Universal Serial Bus Port 1	2
POWERON	O	BT4CRP	USB power supply control	1
MAC ETHERNET INTERFACE (LAN)				
LAN_TXCLK	I	BD4STRP_FT	Transmit Clock	1
LAN_RXCLK	I	BD4STRP_FT	Receive Clock	1
LAN_CRS	I	BD4STRDQP_FT	Carrier Sense indication	1

Note[2]: See Table 2-3 for buffer type descriptions

Note[3]: These pins have a secondary role in that they are read by the device strap option registers during the rising edge of SYSRSTI#. See Section 3.1

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[2]	Description	Qty
LAN_COL	I	BD4STRDQP_FT	Collision indication	1
LAN_TX_EN[3]	O	BD4STRP_TC	Transmit Enable	1
LAN_TXD[3:0][3]	O	BD4STRP_TC	MII Transmit Data	4
LAN_RX_DV	I	BD4STRDQP_FT	Receive Data Valid	1
LAN_RX_ER	I	BD4STRDQP_FT	Receive Error	1
LAN_RXD[3:0]	I	BD4STRDQP_FT	MII Receive Data	4
LAN_MDC[3]	O	BD4STRP_TC	Management Data Clock	1
LAN_MDIO	I/O	BD4STRP_FT	Management Data I/O	1
JTAG				
TCLK	I	SCHMITT_FT	Test clock	1
TDI	I	SCHMITT_FT	Test Data Input	1
TMS	I	SCHMITT_FT	Test Mode input	1
TDO	O	BT4TRP_TC	Test Data Output	1
MISCELLANEOUS				
GPIO[7:0]	I/O	BD4STRP_FT	General Purpose I/Os	8
GPIO_R#[3]	O	BD4TRP_TC	GPIO Read Signal	1
GPIO_W#[3]	O	BD4TRP_TC	GPIO Write Signal	1
UART_RxD	I	TLCHT_FT	Serial Port Receive Line	1
UART_TxD[3]	O	BD4TRP_TC	Serial Port Transmit Line	1
SPKRD	O	BD4TRP_TC	Speaker Device Output	1
SCL	I/O	BD4STRUQP_FT	I²C Interface - Clock Can be used for VGA DDC[1] signal	1
SDA	I/O	BD4STRUQP_FT	I²C Interface - Data Can be used for VGA DDC[0] signal	1
SCAN_ENABLE	I	TLCHTD_TC	Reserved (Test pin)	1

Note[2]: See Table 2-3 for buffer type descriptions

Note[3]: These pins have a secondary role in that they are read by the device strap option registers during the rising edge of SYSRSTI#. See Section 3.1

Table 2-3. Buffer Type Descriptions

Buffer	Description
OSCI13B	Oscillator, 13 MHz, HCMOS
BT4CRP	LVTTL Output, 4 mA drive capability, Tri-State Control
BT4TRP_TC	LVTTL Output, 4 mA drive capability, Tri-State Control, Schmitt trigger
BT8TRP_TC	LVTTL Output, 8 mA drive capability, Tri-State Control, Schmitt trigger
BD4STRP_TC	LVTTL Bi-Directional, 4 mA drive capability, Schmitt trigger
BD4STRP_FT	LVTTL Bi-Directional, 4 mA drive capability, Schmitt trigger, 5V tolerant
BD4STRUP_FT	LVTTL Bi-Directional, 4 mA drive capability, Schmitt trigger, Pull-Up, 5V tolerant
BD4STRDQP_FT	LVTTL Bi-Directional, 4 mA drive capability, Schmitt Trigger, Pull-Down, 5V tolerant.
BD4STRUQP_FT	LVTTL Bi-Directional, 4 mA drive capability, Schmitt Trigger, Pull-Up, 5V tolerant.
BD8STRP_FT	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger, 5V tolerant
BD8STRUP_FT	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger, Pull-Up, 5V tolerant
BD8STRUQP_FT	LVTTL Bi-Directional, 8 mA drive capability, Schmitt Trigger, Pull-Up, 5V tolerant.
BD8PCIARP_FT	LVTTL Bi-Directional, 8 mA drive capability, PCI compatible, 5V tolerant
BD14STARP_FT	LVTTL Bi-Directional, 14 mA drive capability, Schmitt trigger, IEEE1284 compliant, 5V tolerant
BD16STARUQP_TC	LVTTL Bi-Directional, 16 mA drive capability, Schmitt trigger
SCHMITT_FT	LVTTL Input, Schmitt trigger, 5V tolerant
TLCHT_FT	LVTTL Input, 5V tolerant
TLCHTD_TC	LVTTL Input, Pull-Down
TLCHTU_TC	LVTTL Input, Pull-Up
USBDS	USB 1.1 compliant pad buffer
For details on Electrical Specifications of the pads see Table 4-3.	

2.2 SIGNAL DESCRIPTIONS

2.2.1 BASIC CLOCKS AND RESETS

SYSRSTI# *System Reset/Power good.* This input is low when the reset switch is depressed. Otherwise, it reflects the power supply power good signal. This input is asynchronous to all clocks, and acts as a negative active reset. The reset circuit initiates a hard reset on the rising edge of this signal. For more details please refer to Section 4.5.1

SYSRSTO# *Reset Output to System.* This is the system reset signal and is used to reset the rest of the components (not on Host bus) in the system. The ISA bus reset is an externally inverted buffered version of this output and the PCI bus reset is an externally buffered version of this output. For more details please refer to Section 4.5.1

XTALI *14.3 MHz Crystal Input*
XTALO *14.3 MHz Crystal Output.* These pins are connected to the 14.318 MHz crystal to provide the reference clock for the internal frequency synthesizer to generate all remaining clocks.
A 14.318 MHz series cut Quartz Crystal should be connected between these two pins. Balance capacitors of 15 pF should also be added. In the event of an external oscillator providing the master clock signal to the STPC Vega device, the TTL signal should be connected to XTALI.

HCLK *Host Clock.* This clock supplies the CPU and the host related blocks. This clock can be doubled inside the CPU and is intended to operate in the range 25 MHz to 133 MHz. This clock is generated internally from a Phase Locked Loop (PLL) but it can be driven directly from the external system.

DEV_CLK *Peripheral Clock.* 24 MHz general purpose peripheral clock. Also known as PERI_CLK in the schematics. It is provided for convenience for the integration of a Floppy Disk driver function in an external chip. This clock signal is not available in Local Bus mode.

2.2.2 MEMORY INTERFACE

MCLKI *Memory Clock Input.* This clock is used to drive the SDRAM controller. This input should be a buffered version of the MCLKO signal with the track lengths between the buffer and the pin matched with the track lengths between the buffer and the DIMMs.

MCLKO *Memory Clock Output.* This clock is used to drive the DIMMs on the board and is generated from an internal PLL. The default value is 66 MHz.

MA[12:0] *Memory Address.* Multiplexed row and column address lines. **MA[11]** becomes **CS2#** *Chip Select* where 16 Mbit devices are used.

BA[1:0] *Memory Bank Address.* **BA[1]** becomes **CS3#** *Chip Select* where 16 Mbit devices are used.

CS#[1:0] *Chip Select.* These signals are used to disable or enable device operation by masking or enabling all SDRAM inputs except MCLK, CKE and DQM.

MD[63:0] *Memory Data.* This is the 64-bit memory data bus.

RAS#[1:0] *Row Address Strobe.* There are two active-low row address strobe output signals. The RAS# signals drive the memory devices directly without any external buffering.This is one signal that is routed to two buffers.

CAS#[1:0] *Column Address Strobe.* There are two active-low column address strobe output signals. The CAS# signals drive the memory devices directly without any external buffering. This is one signal that is routed to two buffers.

MWE# *Write Enable.* Write enable specifies whether the memory access is a read (MWE# = H) or a write (MWE# = L).

DQM#[7:0] *Data Mask.* Makes data output Hi-Z after the clock and masks the SDRAM outputs. Blocks SDRAM data input when DQM active. This has a granularity of 1 byte on the MD lines.

2.2.3 PCI INTERFACE

PCI_CLKI *33 MHz PCI Input Clock.* This signal is the PCI bus clock input and should be driven from the PCI_CLKO pin.

PCI_CLKO *33 MHz PCI Output Clock.* This is the master PCI bus clock output.

AD[31:0] *PCI Address/Data.* This is the 32-bit multiplexed address and data bus of the PCI. This bus is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions.

CBE#[3:0] *Bus Commands / Byte Enables.* These are the multiplexed command and byte enable signals of the PCI bus. During the address phase they define the command and during the data phase they carry the byte enable information. These pins are inputs when a PCI master other than the STPC Vega owns the bus and outputs when the STPC Vega owns the bus.

FRAME# *Cycle Frame.* This is the frame signal of the PCI bus. It is an input when a PCI master owns the bus and is an output when STPC Vega owns the PCI bus.

IRDY# *Initiator Ready.* This is the initiator ready signal of the PCI bus. It is used as an output when the STPC Vega initiates a bus cycle on the PCI bus. It is used as an input during the PCI cycles targeted to the STPC Vega to determine when the current PCI master is ready to complete the current transaction.

TRDY# *Target Ready.* This is the target ready signal of the PCI bus. It is driven as an output when the STPC Vega is the target of the current bus transaction. It is used as an input when STPC Vega initiates a cycle on the PCI bus.

LOCK# *PCI Lock.* This is the lock signal of the PCI bus and is used to implement the exclusive bus operations when acting as a PCI target agent.

DEVSEL# *I/O Device Select.* This signal is used as an input when the STPC Vega initiates a bus cycle on the PCI bus to determine if a PCI slave device has decoded itself to be the target of the current transaction. It is asserted as an output either when the STPC Vega is the target of the current PCI transaction or when no other device asserts DEVSEL# prior to the subtractive decode phase of the current PCI transaction.

STOP# *Stop Transaction.* Stop is used to implement the disconnect, retry and abort protocol of the PCI bus. It is used as an input for bus cycles initiated by the STPC Vega and is used as an output when a PCI master cycle is targeted to the STPC Vega.

PAR *Parity Signal Transactions*. This is the parity signal of the PCI bus. This signal is used to guarantee even parity across AD[31:0], CBE#[3:0], and PAR. This signal is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions. Its assertion is identical to that of the AD bus delayed by one PCI clock cycle.

SERR# *System Error.* This is the system error signal of the PCI bus. It may, if enabled, be asserted for one PCI clock cycle if target aborts a STPC Vega initiated PCI transaction. Its assertion by either the STPC Vega or by another PCI bus agent will trigger the assertion of NMI to the host CPU. This is an open drain output.

PERR# *Parity Error.* A sustained tri-state signal used to denote the detection of a parity error related to a data phase.

PCI_REQ#[2:0] *PCI Request.* These pins are the three external PCI master request pins. They indicate to the PCI arbiter that external agents desire the use of the bus.

PCI_GNT#[2:0] *PCI Grant.* These pins indicate that the PCI bus has been granted to the master requesting it via PCIREQ#.

PCI_INT#[3:0] *PCI Interrupt Request.* These are the PCI bus interrupt signals.

2.2.4 ISA INTERFACE

ISA_CLK, ISA_CLKX2 *ISA Clock x1, x2.* These pins generate the Clock signal for the ISA bus and a Doubled Clock signal. They are also used as the multiplexer control lines for the Interrupt Controller Interrupt input lines. ISA_CLK is generated from either PCICLK/4 or OSC14M/ 2.

OSC14M *ISA Bus Synchronisation Clock Output.* This is the buffered 14.318 MHz clock for the ISA bus.

LA[23:17] *Unlatched Address.* When the ISA bus is active, these pins are ISA Bus unlatched address lines for 16-bit devices. When the ISA bus is accessed by any cycle initiated from the PCI bus, these pins are in output mode. When an ISA bus master owns the bus, these pins are in input mode.

SA[19:0] *ISA Address Bus.* System address bus of ISA on 8-bit slot. These pins are used as an input when an ISA bus master owns the bus and are outputs at all other times.

SD[15:0] *I/O Data Bus.* These pins are the external data bus to the ISA bus.

ALE *Address Latch Enable.* This is the address latch enable output of the ISA bus and is asserted by STPC Vega to indicate that LA23-17, SA19-0, AEN and SBHE# signals are valid. The ALE is driven high during refresh, DMA master or an ISA master cycles by the STPC Vega. ALE is driven low after reset.

MEMR# *Memory Read.* This is the memory read command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.
The MEMR# signal is active during refresh.

MEMW# *Memory Write.* This is the memory write command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.

SMEMR# *System Memory Read.* The STPC Vega generates the ISA bus SMEMR# signal only when the address is below one megabyte or the cycle is a refresh cycle.

SMEMW# *System Memory Write.* The STPC Vega generates the ISA bus SMEMW# signal only when the address is below one megabyte.

IOR# *I/O Read.* This is the ISA bus IO read command signal. It is an input when an ISA master owns the bus and is an output at all other times.

IOW# *I/O Write.* This is the ISA bus IO write command signal. It is an input when an ISA master owns the bus and is an output at all other times.

MCS16# *Memory Chip Select16.* This is the decode of the ISA LA23-17 address bus pins without any qualification of the command signal lines.
MCS16# is always an input. The STPC Vega ignores this signal during IO and refresh cycles.

IOCS16# *IO Chip Select16.* This signal is the decode of the ISA SA15-0 address bus pins without any qualification of the command signals. The STPC Vega does not drive IOCS16# (similar to PC-AT design). An ISA master access to an internal register of the STPC Vega is executed as an extended 8-bit IO cycle.

BHE# *System Bus High Enable.* This signal, when asserted, indicates that a data byte is being transferred on the SD15-8 lines. It is used as an input when an ISA master owns the bus and is an output at all other times.

ZWS# *Zero Wait State.* This signal is inactif and hardwired to 1.

REF# *Refresh Cycle.* This is the refresh command signal of the ISA bus. It is driven as an output when the STPC Vega performs a refresh cycle on the ISA bus. It is used as an input when an ISA master owns the bus and is used to trigger a refresh cycle.
The STPC Vega performs a pseudo hidden refresh. It requests the host bus for two host clocks to drive the refresh address and capture it in external buffers. The host bus is then relinquished while the refresh cycle continues on the ISA bus.

MASTER# *Add On Card Owns Bus.* This signal is active when an ISA device has been granted bus ownership.

AEN *Address Enable.* Address Enable is enabled when the DMA controller is the bus owner to indicate that a DMA transfer will occur. The enabling of the signal indicates to IO devices to ignore the IOR#/IOW# signal during DMA transfers.

IOCHCK# *IO Channel Check.* IO Channel Check is enabled by any ISA device to signal an error condition that cannot be corrected. NMI signal becomes active upon seeing IOCHCK# active if the corresponding bit in Port B is enabled.

IOCHRDY *Channel Ready.* IOCHRDY is the IO channel ready signal of the ISA bus and is driven as an output in response to an ISA master cycle targeted to the host bus or an internal register of the STPC Vega. The STPC Vega monitors this signal as an input when performing an ISA cycle on behalf of the host CPU, DMA master or refresh. ISA masters which do not monitor IOCHRDY are not guaranteed to work with the STPC Vega since the access to the system memory can be considerably delayed due to the UMA architecture.

ISAOE# ISA *OE Control.* This signal controls the $\overline{OE}$ signal of the external transceiver that connects the IDE DD bus and ISA SA bus. Set high selects the IDE bus and low selects the ISA bus.

IRQ_MUX[3:0] *Multiplexed Interrupt Request.* These are the ISA bus interrupt signals. They have to be encoded before connection to the STPC Vega using ISACLK and ISACLKX2 as the input selection strobes.
Note that IRQ8B, which by convention is connected to the RTC, is inverted before being sent to the interrupt controller, so that it may be connected directly to the $\overline{IRQ}$ pin of the RTC.

DREQ_MUX[1:0] *ISA Bus Multiplexed DMA Request.* These are the ISA bus DMA request signals. They are to be encoded before connection to the STPC Vega using ISACLK and ISACLKX2 as the input selection strobes.

DACK_ENC[2:0] *DMA Acknowledge.* These are the ISA bus DMA acknowledge signals. They are encoded by the STPC Vega before output and should be decoded externally using ISACLK and ISACLKX2 as the control strobes.

TC *ISA Terminal Count.* This is the terminal count output of the DMA controller and is connected to the TC line of the ISA bus. It is asserted during the last DMA transfer, when the byte count expires.

2.2.5 X-BUS INTERFACE

RTCAS# *Real Time Clock Address Strobe.* This signal is asserted for any I/O write to port 70H.

RMRTCCS# *ROM/Real Time Clock Chip Select.* This signal is asserted if a ROM access is decoded during a memory cycle. It should be

combined with MEMR# or MEMW# signals to properly access the ROM. During an IO cycle, this signal is asserted if access to the Real Time Clock (RTC) is decoded. It should be combined with IOR or IOW# signals to properly access the real time clock.

KBCS# *Keyboard Chip Select.* This signal is asserted if a keyboard access is decoded during an I/O cycle.

RTCRW# *Real Time Clock R$\overline{W}$.* This pin is a multi-function pin. When ISAOE# is active, this signal is used as RTCRW#. This signal is asserted for any I/O write to port 71H.

RTCDS# *Real Time Clock DS*. This pin is a multi-function pin. When ISAOE# is active, this signal is used as RTCDS. This signal is asserted for any I/O read to port 71H.

Note: The RMRTCCS#, KBCS#, RTCRW# and RTCDS# signals must be ORed externally with ISAOE# and then connected to the external device. An LS244 or equivalent function can be used if OE# is connected to ISAOE# and the output is provided with a weak pull-up resistor as shown in Figure 6-13.

2.2.6 LOCAL BUS

PA[23:0] *Address Bus Output.*

PD[15:0] *Data Bus.* This is the 16-bit data bus. PD[7:0] is the LSB and PD[15:8] is the MSB.

PRD# *Read Control output.*

PWR# *Write Control output.*

PRDY# *Data Ready input.* This signal is used to create wait states on the bus. When low, it completes the current cycle.

FCS#[1:0] *Flash Chip Select output.* These are the Programmable Chip Select signals for up to two banks of Flash memory. FCS0# is used for the boot process

IOCS#[3:0] *I/O Chip Select output.* These are the Programmable Chip Select signals for up to eight external I/O devices. This is possible through external logic and enabling bit 11 of the Local Bus Control Register Section 11.7. of the Programming Manual.

PBE#[1:0] *Byte Enable.* These are the Byte enables that identifies on which databus the date is valid. PBE#[0] corresponds to PD[7:0] and PBE#[1] corresponds to PD[15:8]. These are normally used when 8 bit transfers are transferred across the 16 bit bus.

2.2.7 IDE INTERFACE

DA[2:0] *Address.* These signals are connected to DA[2:0] of IDE devices directly or through a buffer. If the toggling of signals are to be masked during ISA bus cycles, they can be externally ORed with ISAOE# before being connected to the IDE devices.

DD[15:0] *Data bus.* When the IDE bus is active, they serve as IDE signals DD[11:0]. IDE devices are connected to SA[19:8] directly and the ISA bus is connected to these pins through two LS245 transceivers as described in Figure 6-13.

PCS1#, PCS3# *Primary Chip Select.* These signals are used as the active high primary master & slave IDE chip select signals. These signals must be externally ANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when the ISA bus is idle.

SCS1#, SCS3# *Secondary Chip Select.* These signals are used as the active high secondary master & slave IDE chip select signals. These signals must be externally ANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when the ISA bus is idle.

DIORDY *Busy/Ready.* This pin serves as the IDE signal DIORDY.

PIRQ *Primary Interrupt Request.*
SIRQ *Secondary Interrupt Request.*
Interrupt request from IDE channels.

PDRQ *Primary DMA Request.*
SDRQ *Secondary DMA Request.*
DMA request from IDE channels.

PDACK# *Primary DMA Acknowledge.*
SDACK# *Secondary DMA Acknowledge.*
DMA acknowledge to IDE channels.

PDIOR#, PDIOW# *Primary I/O Read & Write.*
SDIOR#, SDIOW# *Secondary I/O Read & Write*.
Primary & Secondary channel read & write.

2.2.8 USB INTERFACE

OC *OVER CURRENT DETECT* This signal is used to monitor the status of the USB power supply lines of both devices. USB port are disabled when OC signal is asserted.

USBDPLS0, USBDMNS0 *UNIVERSAL SERIAL BUS DATA 0* This signal pair comprises the differential data signal for USB port 0.

USBDPLS1, USBDMNS1 *UNIVERSAL SERIAL BUS PORT 1* This signal pair comprises the differential data signal for USB port 1.

POWERON *USB power supply lines*

2.2.9 MEDIA ACCESS CONTROLLER (MAC) ETHERNET INTERFACE (LAN)

LAN_RXCLK *Receive Clock.* This input provides the timing reference for the transfer of the receive data into the device.

LAN_RXD[3:0] *Receive Data.* MII (Media Independent Interface) receive data. Data is sampled on every rising edge of LAN_RXCLK.

LAN_CRS *Carrier Sense* shall be asserted by the Physical Layer (PHY) when either the transmit or receive medium is non idle. LAN_CRS shall be de-asserted by the PHY when both the transmit and receive media are idle. The PHY shall ensure that LAN_CRS remains asserted throughout the duration of a collision condition. LAN_CRS is not required to transition synchronously with respect to either the LAN_TXCLK or the LAN_RXCLK.

LAN_COL Asserted by the PHY upon detection of a collision on the medium, and shall remain asserted while the collision condition persists. LAN_COL is not required to transition synchronously with respect to either the LAN_TXCLK or the LAN_RXCLK.

LAN_TXCLK *Transmit Clock*. This input provides the timing reference for the transfer of the transmit data into the device.

LAN_TXD[3:0] *Transmit Data.* MII transmit data bus. Valid data is generated on LAN_TXD[3:0] on every rising edge of LAN_TXCLK while LAN_TX_EN is asserted. While LAN_TX_EN is deserted, LAN_TXD[3:0] values are driven to 0. LAN_TXD[3:0] transitions are synchronous to rising edges of LAN_TXCLK.

LAN_TX_EN *Transmit Enable*. Indicates when the device is presenting valid transmit data on the bus. While LAN_TX_EN is asserted, the device generates LAN_TXD[3:0]. LAN_TX_EN is asserted with the first data of preamble and remains asserted throughout the duration of the packet until it is deserted prior to the first LAN_TXCLK following the final data of the frame. LAN_TX_EN transitions are synchronous to LAN_TXCLK.

LAN_RX_DV *Receive Data Valid* is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on the LAN_RXD[3:0] bundle and that the data on LAN_RXD[3:0] is synchronous to LAN_RXCLK. LAN_RX_DV transitions synchronously with respect to the LAN_RXCLK. LAN_RX_DV remains asserted continuously from the first recovered nibble of the frame through the final recovered nibble and is negated prior to the first LAN_RXCLK that follows the final nibble.

LAN_RX_ER *Receive Error* is driven by the PHY. It shall be asserted for one or more LAN_RXCLK periods to indicate to the Reconciliation sublayer that an error (e.g. a coding error, or any error that the PHY is capable of detecting, and that may otherwise be undetectable at the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY to the Reconciliation sublayer. LAN_RX_ER shall transition synchronously with respect to LAN_RXCLK. While LAN_RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the LAN_RX_ER signal for at least one cycle of the LAN_RXCLK while driving the appropriate value onto LAN_RXD[3:0].

LAN_MDC *Management Data Clock.* Non-continuous clock output that provides a timing reference for bits on the LAN_MDIO pin. During MII management port operations, LAN_MDC minimum high and low time is 160 ns each and the minimum period for LAN_MDC is 400 ns. When no management operations are in progress, LAN_MDC is driven LOW.

LAN_MDIO *Management Data I/O.* Bi-directional MII management port data pin. LAN_MDIO is an output during the header portion of the management frame transfers and during the data portion of write operations. LAN_MDIO is an input during the data portion of read operations.

2.2.10 I^2C

SCL *Serial Clock*

SDA *Serial Data*

2.2.11 JTAG INTERFACE

TCLK *Test clock*

TDI *Test data input*

TMS *Test mode input*

TDO *Test data output*

TRST Test reset input

2.2.12 MISCELLANEOUS

GPIO[7:0] *General Purpose I/Os*

GPIO_R# *GPIO Read*

GPIO_W# *GPIO Write*

UART_RxD, UART_TxD *Single UART.* This RxTx only UART Serial Port has programmable word length, stop bits and parity and a programmable Baud Rate Generator. It also includes an Interrupt Generator, a Scratch Register and two 16-byte FIFO Registers.

SPKRD *Speaker Drive.* This the output to the speaker and is the AND of the counter 2 output with bit 1 of Port 61, and drives an external speaker driver. This output should be connected to a 7407-type high voltage driver.

SCAN_ENABLE *Reserved*. This pin is reserved for Test and Miscellaneous functions.

VDD_CORE *1.8 V ±0.15 V Core Power Supply.* These power pins are necessary to supply the core with 1.8 V.

VDD_CORE *3.3 V ±0.3 V Core Power Supply.* These power pins are necessary to supply the core with 3.3 V.

2.3 SIGNAL DETAIL

The muxing between ISA and LOCAL BUS is performed by external strap options.

The resulting interface is then dynamically muxed with the IDE Interface. .

Table 2-4. ISA / IDE Dynamic Multiplexing

ISA BUS (ISAOE# = 0)	IDE (ISAOE# = 1)
RMRTCCS#	DD[15]
KBCS#	DD[14]
RTCRW#	DD[13]
RTCDS	DD[12]
SA[19:8]	DD[11:0]
LA[23]	SCS3#
LA[22]	SCS1#
LA[21]	PCS3#
LA[20]	PCS1#
LA[19:17]	DA[2:0]
IOCHRDY	IORDY

.

Table 2-5. ISA / Local Bus Pin Sharing

ISA / IPC	LOCAL BUS
SD[15:0]	PD[15:0]
DREQ_MUX[1:0]	PA[21:20]
SMEMR#	PA[19]
MEMW#	PA[18]
BHE#	PA[17]
AEN	PA[16]
ALE	PA[15]
MEMR#	PA[14]
IOR#	PA[13]
IOW#	PA[12]
REF#	PA[11]
IOCHCK#	PA[10]
GPIO_RX	PA[9]
ZWS#	PA[8]
SA[7:1]	PA[7:1]
SA[0]	PRDY#
TC	PA[0]
DACK_ENC[2:0]	IOCSx#[2:0]
MASTER#	PRD#
MCS16#	PWR#
ISAOE#	IOCSx#[3]
DEV_CLK, RTCAS#	FCS#[1:0]
IOCS16#	PBE#0
SMEMW#	PBE#1

Table 2-6. Pinout

Pin #	Pin name
B5	SYSRSETI#
C5	SYSRSETO#
B4	XTALI
A4	XTALO
AC25	HCLK
F25	DEV_CLK/FCS#[1]
AE17	MCLKI
AD16	MCLKO
AF21	MA[0]
AD20	MA[1]
AE21	MA[2]
AC20	MA[3]
AF22	MA[4]
AD21	MA[5]
AE22	MA[6]
AF23	MA[7]
AC21	MA[8]
AD22	MA[9]
AE23	MA[10]
AC22	BA[0]
AD23	MA[12]
AD18	CS#[0]
AE19	CS#[1]
AD19	MA[11]/CS#[2]
AF20	CS#[3]/BA[1]
AC19	RAS#[0]
AE20	RAS#[1]
AD17	CAS#[0]
AE18	CAS#[1]
AE14	DQM#[0]
AF14	DQM#[1]
AD15	DQM#[2]
AE15	DQM#[3]
AF15	DQM#[4]
AC15	DQM#[5]
AE16	DQM#[6]
AC16	DQM#[7]
AC17	MWE#
U4	MD[0]
V1	MD[1]
V2	MD[2]
V3	MD[3]
W2	MD[4]
For Note definition see Table 2-2 Definition of Signal Pins	

Table 2-6. Pinout

Pin #	Pin name
W3	MD[5]
Y1	MD[6]
Y2	MD[7]
W4	MD[8]
AA1	MD[9]
Y3	MD[10]
AA2	MD[11]
Y4	MD[12]
AB1	MD[13]
AA3	MD[14]
AB2	MD[15]
AA4	MD[16]
AC1	MD[17]
AB3	MD[18]
AC2	MD[19]
AB4	MD[20]
AC3	MD[21]
AD2	MD[22]
AE1	MD[23]
AC5	MD[24]
AD4	MD[25]
AE3	MD[26]
AF2	MD[27]
AC6	MD[28]
AD5	MD[29]
AE4	MD[30]
AF4	MD[31]
AE5	MD[32]
AD6	MD[33]
AC7	MD[34]
AF5	MD[35]
AE6	MD[36]
AD7	MD[37]
AC8	MD[38]
AF6	MD[39]
AE7	MD[40]
AD8	MD[41]
AF7	MD[42]
AE8	MD[43]
AD9	MD[44]
AC10	MD[45]
AE9	MD[46]
AD10	MD[47]
AF9	MD[48]
AE10	MD[49]
For Note definition see Table 2-2 Definition of Signal Pins	

Table 2-6. Pinout

Pin #	Pin name
AC11	MD[50]
AD11	MD[51]
AE11	MD[52]
AC12	MD[53]
AF11	MD[54]
AD12	MD[55]
AE12	MD[56]
AF12	MD[57]
AC13	MD[58]
AD13	MD[59]
AE13	MD[60]
AF13	MD[61]
AC14	MD[62]
AD14	MD[63]
AA23	PCI_CLKI
AB25	PCI_CLKO
AA24	AD[0]
Y23	AD[1]
AB24	AD[2]
AA25	AD[3]
Y24	AD[4]
W23	AD[5]
AA26	AD[6]
Y25	AD[7]
W24	AD[8]
Y26	AD[9]
W25	AD[10]
V24	AD[11]
V25	AD[12]
U23	AD[13]
V26	AD[14]
U24	AD[15]
U25	AD[16]
T23	AD[17]
T24	AD[18]
T25	AD[19]
T26	AD[20]
R23	AD[21]
R24	AD[22]
R25	AD[23]
R26	AD[24]
P23	AD[25]
P24	AD[26]
P25	AD[27]
P26	AD[28]
For Note definition see Table 2-2 Definition of Signal Pins	

Table 2-6. Pinout

Pin #	Pin name
N23	AD[29]
N24	AD[30]
N25	AD[31]
N26	CBE[0]
M23	CBE[1]
M24	CBE[2]
M25	CBE[3]
M26	FRAME#
L26	TRDY#
L25	IRDY#
L24	STOP#
L23	DEVSEL#
K24	PAR
K23	SERR#
J26	PERR#
K25	LOCK#
J25	POWERON
J24	OC
H25	USBDMNS[0]
H24	USBDPLS[0]
H23	USBDMNS[1]
G25	USBDPLS[1]
AD25	PCI_REQ#[0]
AC24	PCI_REQ#[1]
AE26	PCI_REQ#[2]
AE24	PCI_GNT#[0]
AF25	PCI_GNT#[1]
AB23	PCI_GNT#[2]
D6	PCI_INT[0]
D5	PCI_INT[1]
C4	PCI_INT[2]
B3	PCI_INT[3]
B23	LA[17]/DA[0]
C22	LA[18]/DA[1]
D21	LA[19]/DA[2]
A23	LA[20]/PCS1#
B22	LA[21]/PCS3#
C21	LA[22]/SCS1#
D20	LA[23]/SCS3#
D17	SA[0]/PRDY#
A18	SA[1]/PA[1]
C17	SA[2]/PA[2]
B17	SA[3]/PA[3]
D16	SA[4]/PA[4]
C16	SA[5]/PA[5]
For Note definition see Table 2-2 Definition of Signal Pins	

Table 2-6. Pinout

Pin #	Pin name
B16	SA[6]/PA[6]
A16	SA[7]/PA[7]
E24	SA[8]/DD[0]
D25	SA[9]/DD[1]
E23	SA[10]/DD[2]
D24	SA[11]/DD[3]
C25	SA[12]/DD[4]
B26	SA[13]/DD[5]
A25	SA[14]/DD[6]
B24	SA[15]/DD[7]
C23	SA[16]/DD[8]
D22	SA[17]/DD[9]
F23	SA[18]/DD[10]
D26	SA[19]/DD[11]
D15	SD[0]/PD[0]
C15	SD[1]/PD[1]
B15	SD[2]/PD[2]
A15	SD[3]/PD[3]
D14	SD[4]/PD[4]
C14	SD[5]/PD[5]
B14	SD[6]/PD[6]
A14	SD[7]/PD[7]
D13	SD[8]/PD[8]
C13	SD[9]/PD[9]
B13	SD[10]/PD[10]
A13	SD[11]/PD[11]
A12	SD[12]/PD[12]
B12	SD[13]/PD[13]
C12	SD[14]/PD[14]
D12	SD[15]/PD[15]
D1	ISA_CLK
F3	ISA_CLK2X
E1	OSC14M
E2	LAN_TXCLK
F2	LAN_RXCLK
G3	LAN_CRS
F1	LAN_COL
H4	LAN_TX_EN
G2	LAN_TXD[0]
H3	LAN_TXD[1]
J2	LAN_TXD[2]
H2	LAN_TXD[3]
J3	LAN_RX_DV
K4	LAN_RX_ER
K2	LAN_RXD[0]
For Note definition see Table 2-2 Definition of Signal Pins	

Table 2-6. Pinout

Pin #	Pin name
L4	LAN_RXD[1]
L3	LAN_RXD[2]
L2	LAN_RXD[3]
K3	LAN_MDC
M4	LAN_MDIO
C11	ALE/PA[15]
C7	ZWS#/PA[8]
A11	BHE#/PA[17]
B10	MEMR#/PA[14]
C10	MEMW#/PA[18]
D10	SMEMR#/PA[19]
A9	SMEMW#/PBE#1
C9	IOR#/PA[13]
B8	IOW#/PA[12]
A7	MCS16#/PWR#
B7	IOCS16#/PBE#0
C8	MASTER#/PRD#
D8	REF#/PA[11]
D11	AEN/PA[16]
A6	IOCHCK#/PA[10]
A22	IOCHRDY/IORDY
E26	ISAOE#/IOCSx#[3]
B6	RTCAS#/FCS#[0]
G24	RTCDS#/DD[12]
E25	RTCRW#/DD[13]
G23	RMRTCCS#/DD[15]
D7	LB_PA[22]
A5	LB_PA[23]
C6	LB_PA[24]
B21	PIRQ
C20	SIRQ
A21	PDRQ
D19	SDRQ
B20	PDACK#
C19	SDACK#
A20	PDIOR#
B19	PDIOW#
C18	SDIOR#
B18	SDIOW#
A2	IRQ_MUX[0]
B9	IRQ_MUX[1]
B11	IRQ_MUX[2]
B1	IRQ_MUX[3]
C2	DREQ_MUX[0]/PA[20]
D3	DREQ_MUX[1]/PA[21]
For Note definition see Table 2-2 Definition of Signal Pins	

Table 2-6. Pinout

Pin #	Pin name
E4	DACK_ENC[0]/IOCSx#[0]
D2	DACK_ENC[1]/IOCSx#[1]
E3	DACK_ENC[2]/IOCSx#[2]
F4	TC/PA[0]
F24	KBCS#/DD[14]
P4	GPIO[0]
P3	GPIO[1]
P2	GPIO[2]
P1	GPIO[3]
R1	GPIO[4]
R2	GPIO[5]
R3	GPIO[6]
R4	GPIO[7]
T1	GPIO_R#/PA[9]
T2	GPIO_W#
G4	SPKRD
U3	SCL
T3	SDA
N4	SCAN_ENABLE
N1	TCLK
M1	TMS
M3	TDI
M2	TDO
N3	UART_RxD
N2	UART_TxD
J1	VDD33_CPUCLK_PLL
L1	VDD18_CPUCLK_PLL
G26	VDD_DEV_CLK_PLL[1]
AF18	VDD_MCLK_PLL[1]
AB26	VDD_PCICLKO_PLL[1]
C1	VDD_CORE
AD1	VDD_CORE
C26	VDD_CORE
AD26	VDD_CORE
K1	VDD
H26	VDD
W1	VDD
W26	VDD
A3	VDD
A10	VDD
A17	VDD
A24	VDD
AF3	VDD
AF10	VDD
AF17	VDD
For Note definition see Table 2-2 Definition of Signal Pins	

Table 2-6. Pinout

Pin #	Pin name
AF24	VDD
F26	VSS_DEV_CLK_PLL
G1	VSS_CPUCLK_PLL
AC26	VSS_PCICLKO_PLL
AF16	VSS_MCLK_PLL
J4	GND
V4	GND
J23	GND
V23	GND
D9	GND
D18	GND
AC9	GND
AC18	GND
H1	GND
U1	GND
K26	GND
U26	GND
A8	GND
A19	GND
AF8	GND
AF19	GND
A1	GND
A26	GND
B2	GND
B25	GND
C3	GND
C24	GND
D4	GND
D23	GND
AC4	GND
AC23	GND
AD3	GND
AD24	GND
AE2	GND
AE25	GND
AF1	GND
AF26	GND
L[11:16]	GND
M[11:16]	GND
N[11:16]	GND
P[11:16]	GND
R[11:16]	GND
T[11:16]	GND
T4	*Unconnected*
U2	*Unconnected*
For Note definition see Table 2-2 Definition of Signal Pins	

3 STRAP OPTIONS

This chapter defines the Vega Strap Options and their locations. The logic levels on the following dual-function pins are sampled on the rising edge of the last CLK in which reset is active (when SYSRSETIx is low). All bits are read-only.

Table 3-1. Strap Options

Pin	Location	Setting	Reference
LAN_TXD[0]	Index 4A, bit 0	User defined	see Section 3.1.1
LAN_TXD[1]	Index 4A, bit 1		
LAN_TXD[2]	Index 4A, bit 2		
LAN_TXD[3]	Index 4A, bit 3		
LAN_TX_EN	Index 4A, bit 4		
GPIO_Wx	Index 4A, bit 5	Pull Down	
GPIO_Rx	Index 4A, bit 6	Pull Down	
DACK_ENC[1]	Index 4A, bit 7	Pull Up	
LB_PA22	Index 4B, bit 0	Pull Down	see Section 3.1.2
LB_PA23	Index 4B, bit 1	Pull Up	
LB_PA24	Index 4B, bit 2	Pull Down	
LAN_MDC	Index 4B, bit 3	Pull Down	
UART_TXD	Index 4B, bit 4	Pull Down	
TC	Index 4B, bit 5	Pull Up	
DACK_ENC[0]	Index 4B, bit 6	Pull Up	
SMEMRx	Index 4B, bit 7	Pull Down	
SMEMWx	Index 4C, bit 0	Pull Down	see Section 3.1.3
DACK_ENC[2]	Index 4C, bit 1	Pull Up	
Note that all strap options must be implemented including those that are user defined			

3.1 POWER ON STRAP REGISTER DESCRIPTIONS

3.1.1 ADPC Strap Register 0 Configuration

ADPC0 Access = 0022h/0023h Regoffset = 04Ah

7	6	5	4	3	2	1	0
DACK_ENC[1]	**GPIO_Rx**	**GPIO_Wx**	**LAN_TX_EN**	**LAN_TXD[3]**	**LAN_TXD[2]**	**LAN_TXD[1]**	**LAN_TXD[0]**
This register defaults to the values sampled on above dual-function pins after reset							

Bit Nb Sampled	Mnemonic	Description
Bit 7	**DACK_ENC[1]**	Reflects the value sampled on DACK_ENC[1] pin to control the enabling of the LOCAL bus or the ISA bus: 1: ISA bus functionality of the device is enabled, the local bus is disabled. 0: Local bus functionality of the device is enabled, the ISA bus is disabled. Default: strapped to logic 1.
Bit 6	**GPIO_Rx**	Reflects the value sampled on GPIO_Rx pin to control the source of HCLK and MCLKO. 1: External clock source is driving the HCLK pin, MCLKO pin is tristated and MCLKO source is external. 0: MCLKO and HCLK pins are both outputs and are connected to their respective internal frequency synthesizer outputs. Default: strapped to logic 0.
Bit 5	**GPIO_Rx**	Reflects the value sampled on GPIO_Wx pin to control the clock relationship between MCLK and HCLK. 1: MCLK and HCLK have the same frequency; will improve system performance. 0: MCLK and HCLK have different frequencies. Default: strapped to logic 0.
Bits 4-0	**LAN_TX_EN**: **LAN_TXD[0]**	Reflect the values sampled on LAN_TX_EN and LAN_TXD[3:0] pins to control HCLK and PCI_CLK frequencies. 00000: HCLK = 24.928974 MHz; PCI_CLK = 12.46 MHz; 00001: HCLK = 49.857948 MHz; PCI_CLK = 24.93 MHz; 00010: HCLK = 66.634607 MHz; PCI_CLK = 33.32 MHz; 00011: HCLK = 72.485786 MHz; PCI_CLK = 24.16 MHz; 00100: HCLK = 74.895095 MHz; PCI_CLK = 24.97 MHz; 00101: HCLK = 77.448337 MHz; PCI_CLK = 25.82 MHz; 00110: HCLK = 79.943172 MHz; PCI_CLK = 26.65 MHz; 00111: HCLK = 82.329535 MHz; PCI_CLK = 27.44 MHz; 01000: HCLK = 87.499989 MHz; PCI_CLK = 29.17 MHz; 01001: HCLK = 89.999989 MHz; PCI_CLK = 30.00 MHz; 01010: HCLK = 92.471579 MHz; PCI_CLK = 30.82 MHz; 01011: HCLK = 97.473764 MHz; PCI_CLK = 32.49 MHz; 01100: HCLK = 99.715896 MHz; PCI_CLK = 33.24 MHz; 01101: HCLK = 102.430057 MHz; PCI_CLK = 25.61 MHz; 01110: HCLK = 104.999987 MHz; PCI_CLK = 26.25 MHz; 01111: HCLK = 107.386350 MHz; PCI_CLK = 26.85 MHz; 10000: HCLK = 109.989655 MHz; PCI_CLK = 27.50 MHz; 10001: HCLK = 112.499986 MHz; PCI_CLK = 28.12 MHz; 10010: HCLK = 114.545440 MHz; PCI_CLK = 28.64 MHz; 10011: HCLK = 117.409076 MHz; PCI_CLK = 29.35 MHz; 10100: HCLK = 119.914757 MHz; PCI_CLK = 29.98 MHz; 10101: HCLK = 122.499984 MHz; PCI_CLK = 30.62 MHz; 10110: HCLK = 124.958662 MHz; PCI_CLK = 31.24 MHz; 10111: HCLK = 127.431802 MHz; PCI_CLK = 31.86 MHz; 11000: HCLK = 129.965018 MHz; PCI_CLK = 32.49 MHz; 11001: HCLK = 133.269214 MHz; PCI_CLK = 33.32 MHz;

3.1.2 ADPC Strap Register 1 Configuration

ADPC1 Access = 0022h/0023h Regoffset = 04Bh

7	6	5	4	3	2	1	0
SMEMRx	**DACK_ENC[0]**	**TC**	**UART_TXD**	**LAN_MDC**	**LB_PA24**	**LB_PA23**	**LB_PA22**
This register defaults to the values sampled on the above dual-function pins after reset							

Bit Nb Sampled	Mnemonic	Description
Bit 7	**SMEMRx**	Reserved Default: strapped to logic 0
Bit 6	**DACK_ENC[0]**	Reserved Default: strapped to logic 1.
Bit 5	**TC**	Reserved, Default: strapped to logic 1.
Bits 4-3	**UART_TXD: LAN_MDC**	Reflect the values sampled on UART_TXD and LAN_MDC pins to control the uide clock in conjunction with hclko_strap[4:0] (bits 4-0 of index register 4a - para Section 3.1.1) Details are given in Table 3.1.3.
Bits 2-0	**LB_PA24: LB_PA22**	Reflect the values sampled on LB_PA24, LB_PA23 and LB_PA22 pins to control the bus to core clock multiplication factor of CP250C. 000: ratio of 2.5x 010: ratio of 2x 001: ratio of 3x 011: ratio of 3.5x 1xx: Reserved Default: strapped to logic 010.

Table 3-2. HCLK, PCICLK and UIDECLK Frequencies (MHz)

HCLK		PCICLK		UIDECLK					
HLCK Strap Settings Bits [4:0]	Freq	Freq	Div Factor	UIDECLK33 (uideclk_strap=10)		UIDECLK66 (uideclk_strap=00)		UIDECLK100 (uideclk_strap=11)	
				Freq	Div Factor	Freq	Div Factor	Freq	Div Factor
00h	24.93	12.46	2.0	16.62 *	1.5	16.62 *	1.5	24.93 *	1.0
01h	49.86	24.93	2.0	33.24	1.5	33.24 *	1.5	49.86 *	1.0
02h	66.63	33.32	2.0	33.32	2.0	66.63	1.0	66.63 *	1.0
03h	72.49	24.16	3.0	28.99	2.5	48.32	1.5	72.49	1.0
04h	74.90	24.97	3.0	29.96	2.5	49.93	1.5	74.90	1.0
05h	77.45	25.82	3.0	30.98	2.5	51.63	1.5	77.45	1.0
06h	79.94	26.65	3.0	31.98	2.5	53.30	1.5	79.94	1.0
07h	82.33	27.44	3.0	32.93	2.5	54.89	1.5	82.33	1.0
08h	87.50	29.17	3.0	29.17	3.0	58.33	1.5	87.50	1.0
09h	90.00	30.00	3.0	30.00	3.0	60.00	1.5	90.00	1.0
0Ah	92.47	30.82	3.0	30.82	3.0	61.65	1.5	92.47	1.0
0Bh	97.47	32.49	3.0	32.49	3.0	64.98	1.5	97.47	1.0
0Ch	99.72	33.24	3.0	33.24	3.0	66.48	1.5	99.72	1.0
0Dh	102.43	25.61	4.0	25.61	4.0	51.22	2.0	68.29	1.5
0Eh	105.00	26.25	4.0	26.25	4.0	52.50	2.0	70.00	1.5
0Fh	107.39	26.85	4.0	26.85	4.0	53.69	2.0	71.59	1.5
10h	109.99	27.50	4.0	27.50	4.0	54.99	2.0	73.33	1.5
11h	112.50	28.12	4.0	28.12	4.0	56.25	2.0	75.00	1.5
12h	114.55	28.64	4.0	28.64	4.0	57.27	2.0	76.37	1.5
13h	117.41	29.35	4.0	29.35	4.0	58.70	2.0	78.27	1.5
14h	119.91	29.98	4.0	29.98	4.0	59.96	2.0	79.94	1.5
15h	122.50	30.62	4.0	30.62	4.0	61.25	2.0	81.67	1.5
16h	124.96	31.24	4.0	31.24	4.0	62.48	2.0	83.31	1.5
17h	127.43	31.86	4.0	31.86	4.0	63.72	2.0	84.95	1.5
18h	129.97	32.49	4.0	32.49	4.0	64.98	2.0	86.65	1.5
19h	133.27	33.32	4.0	33.32	4.0	66.63	2.0	88.85	1.5

3.1.3 ADPC Strap Register 2 Configuration

ADPC2 Access = 0022h/0023h Regoffset = 04Ch

7	6	5	4	3	2	1	0
Rsv						**DACK_ENC[2]**	**SMEMWx**
This register defaults to the values sampled on the above dual-function pins after reset							

Bit Number Sampled	Mnemonic	Description
Bits 7-2	**Rsv**	Reserved
Bit 1	**DACK_ENC[2]**	Reflects the value sampled on DACK_ENC[2] pin to control he LOCAL bus 8/16 bit boot flash width(localbus_bk0_width). 0: 8-bit width 1: 16-bit width.
Bit 0	**SMEMWx**	Reflects the value sampled on SMEMWx pin to control the enabling of MCLKI PLL. 1: the MCLKI PLL is bypassed. 0: the MCLKI PLL is enabled. Default: strapped to logic 0.

4 ELECTRICAL SPECIFICATIONS

4.1 Introduction

The electrical specifications in this chapter are valid for the STPC Vega.

4.2 Electrical Connections

4.2.1 POWER/GROUND CONNECTIONS/ DECOUPLING

Due to the high frequency of operation of the STPC Vega, it is necessary to install and test this device using standard high frequency techniques. The high clock frequencies used in the STPC Vega and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the VSS and VDD pins.

4.2.2 UNUSED INPUT PINS

All inputs not used by the designer and not listed in the table of pin connections in Chapter 3 should be connected either to VDD or to VSS. Connect active-high inputs to VDD through a 20 kΩ (±10%) pull-up resistor and active-low inputs to VSS and connect active-low inputs to VCC through a 20 kΩ (±10%) pull-down resistor to prevent spurious operation.

4.2.3 RESERVED DESIGNATED PINS

Pins designated reserved should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor or an active signal could cause unexpected results and possible circuit malfunctions.

4.3 Absolute Maximum Ratings

The following table lists the absolute maximum ratings for the STPC Vega device. Stresses beyond those listed under Table 4-1 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those specified in section 14.4 “Operating Conditions”. Exposure to conditions beyond Table 4-1 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings (Table 4-1) may also result in reduced useful life and reliability.

Table 4-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
V_{DDx}	DC Supply Voltage	-0.3	4.0	V
V_{CORE}	DC Supply Voltage for Core	-0.3	1.95	V
V_I, V_O	Digital Input and Output Voltage	-0.3	VDD + 0.5	V
V_{5T}	5 Volt Tolerance	-0.3	5.5	V
V_{ESD}	ESD Capacity (Human body mode)		2000	V
T_{STG}	Storage Temperature	-40	+150	°C
T_{OPER}	Operating Temperature (Tcase) See Note 1.	-40	+105°	°C
P_{TOT}	Total Power Dissipation of the Package		5	W

Note 1: The figures specified apply to an STPC device that is soldered to a board, as detailed in the Board Layout Section.

4.4 DC CHARACTERISTICS

Table 4-2. DC Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	3.3V Operating Voltage		3.0	3.3	3.6	V
V_{CORE}	1.8V Operating Voltage		1.65	1.8	1.95	V
P_{DD}	3.3V Supply Power	$3.0V < V_{DD} < 3.6V$				W
P_{CORE}	1.8V Supply Power					W
V_{IL}	Input Low Voltage	Except XTALI	-0.3		0.8	V
		XTALI	-0.3		0.8	V
V_{IH}	Input High Voltage	Except XTALI	2.1		V_{DD}+0.3	V
		XTALI	2.35		V_{DD}+0.3	V
I_{LK}	Input Leakage Current	Input, I/O	-5		5	µA
	Integrated Pull up/down			50		KΩ

Table 4-3. PAD buffers DC Characteristics

Buffer Type	I/O count	IO TYPE	V_{IH} min (V)	V_{IL} max (V)	V_{OH} min (V)	V_{OL} max (V)	I_{OL} min (mA)	I_{OH} max (mA)	C_{load} max (pF)	Derating (ps/pF)[1]	C_{IN} (pF)
ANA	1	I	-	-	-	-	-	-	-	-	-
BD4STRDQP_FT	8	I/O	1,4	1,4	2,64	0,06	-	-	-	-	-
BD4STRP_FT	23	I/O	1,1	1,34	2,65	0,06	-	-	-	-	-
BD4STRP_TC	9	I/O	1,06	1,31	2,65	0,06	-	-	-	-	-
BD4STRUQP_FT	10	I/O	1,1	1,27	2,64	0,06	-	-	-	-	-
BD4TRP_TC	9	I/O	1,35	1,68	2,64	0,06	-	-	-	-	-
BD8PCIARP_FT	50	I/O	0,96	1,12	2,64	0,06	-	-	-	-	-
BD8STRP_FT	16	I/O	1,25	1,31	2,64	0,06	-	-	-	-	-
BD8STRP_TC	8	I/O	1,18	1,32	2,64	0,06	-	-	-	-	-
BD8STRUQP_FT	33	I/O	1,12	1,27	2,64	0,06	-	-	-	-	-
BD8STRUQP_TC	65	I/O	1,18	1,26	2,64	0,06	-	-	-	-	-
BD8TRP_TC	3	I/O	1,29	1,7	2,64	0,06	-	-	-	-	-
BD16STARUQP_TC	20	I/O	1,17	1,29	2,64	0,06	-	-	-	-	-
BT4CRP	1	O	-	-	-	-	-	-	-	-	-
BT4TR_TC	1	O	-	-	2,64	0,06	-	-	-	-	-
BT8TRP_TC	15	O	-	-	2,64	0,06	-	-	-	-	-
OSCI13B	1	O	-	-	-	-	-	-	-	-	-
SHMITT_FT	10	I	1,4	1,29	-	-	-	-	-	-	-
TLCHT_FT	3	I	1,29	1,66	-	-	-	-	-	-	-
TLCHT_TC	1	I	1,29	1,71	-	-	-	-	-	-	-
TLCHTD_TC	1	I	-	-	-	-	-	-	-	-	-
TLCHTU_TC	1	I	1,29	1,64	-	-	-	-	-	-	-
USBDS	4	I	1,01	1,28	2,64	0,06	-	-	-	-	-

Note 1: time to output variation depending on the capacitive load.

Table 4-4. 1.8V Power Consumption

HCLK (MHz)	CPUCLK (MHz)	MCLK (MHz)	Mode	P_{Max} (mW)	
				P_{typ}	P_{max}
66	133 (x2)	66	SYNC	1.31	1.87
90	180 (X2)	90	SYNC	1.64	2.34
66	200 (X3)	100	ASYNC	1.77	2.51
100	200 (X2)	100	SYNC	1.77	2.52

4.5 AC Characteristics

Table 4-5 through Table 4-12 list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1. and Figure 4-2. The rising clock edge reference level VREF and other reference levels are shown in Table 4-5 for the STPC Vega. Input or output signals must cross these levels during testing.

Figure 4-1. shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

Table 4-5. Drive Level and Measurement Points for Switching Characteristics

Symbol	Value	Units
V_{REF}	1.5	V
V_{IHD}	3.0	V
V_{ILD}	0.0	V

Note: Refer to Figure 4-1.

Figure 4-1. Drive Level and Measurement Points for Switching Characteristics

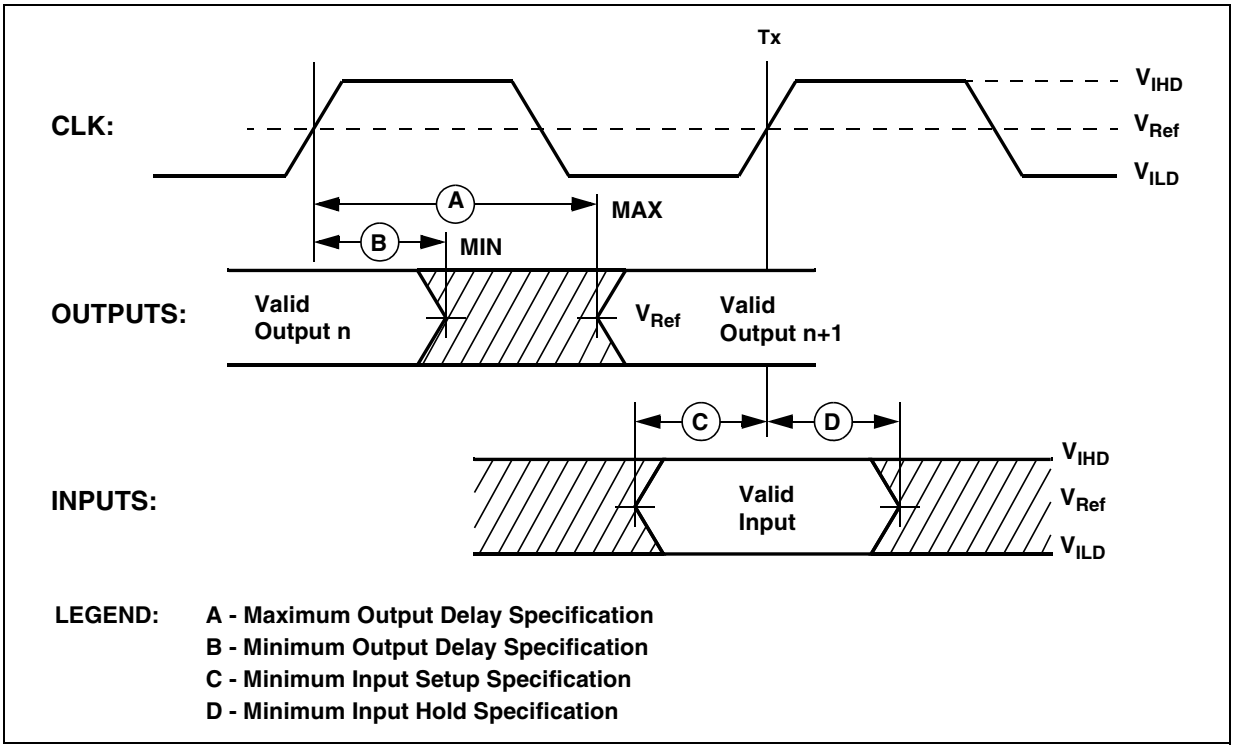
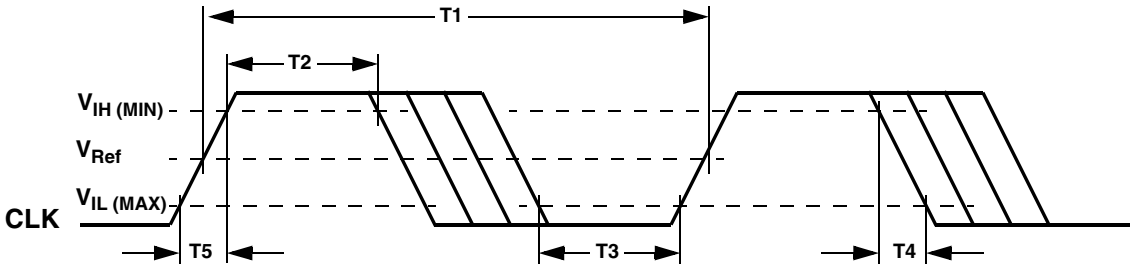


Figure 4-2. CLK Timing Measurement Points



LEGEND:
T1 - One Clock Cycle
T2 - Minimum Time at V_{IH}
T3 - Minimum Time at V_{IL}
T4 - Clock Fall Time
T5 - Clock Rise Time

NOTE: All sIgnals are sampled on the rising edge of the CLK.

4.5.1 POWER ON SEQUENCE

Figure 4-3 describes the power-on sequence of the STPC, also called cold reset.

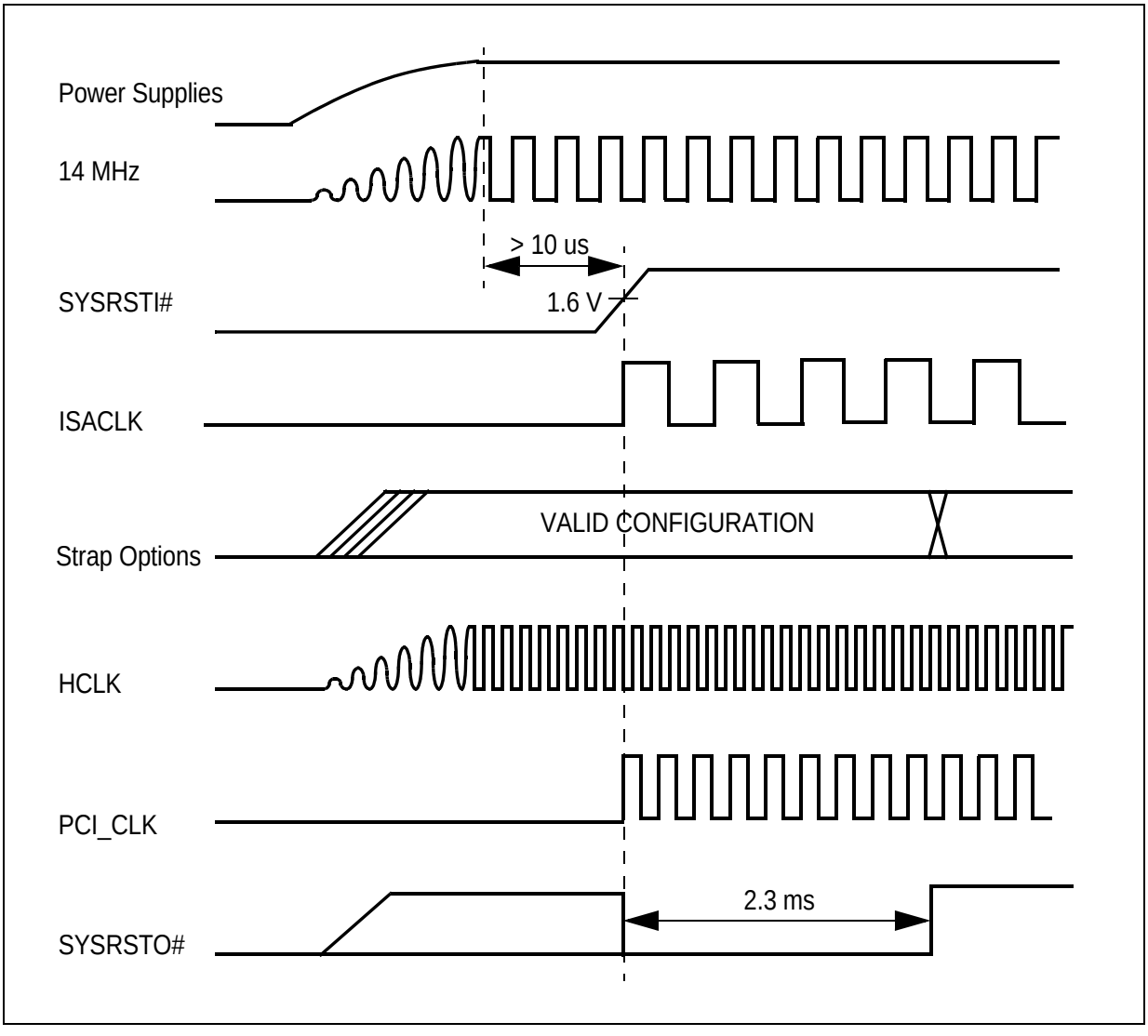
There is no dependency between the different power supplies and there is no constraint on their rising time.

SYSRSTI# has no constraint on its rising edge but must stay active until power supplies are all within specifications, a margin of 10µs is even recommended to let the STPC PLLs and strap options stabilize.

Strap Options are continuously sampled during SYSRSTI# low and must remain stable. Once SYSRSTI# is high, they MUST NOT CHANGE until SYSRSTO# goes high.

Bus activity starts only few clock cycles after the release of SYSRSTO#. The toggling signals depend on the STPC configuration.
In ISA mode, activity is visible on PCI prior to the ISA bus as the controller is part of the south bridge.
In Local Bus mode, the PCI bus is not accessed and the Flash Chip Select is the control signal to monitor.

Figure 4-3. Power-on timing diagram



4.5.2 RESET SEQUENCE

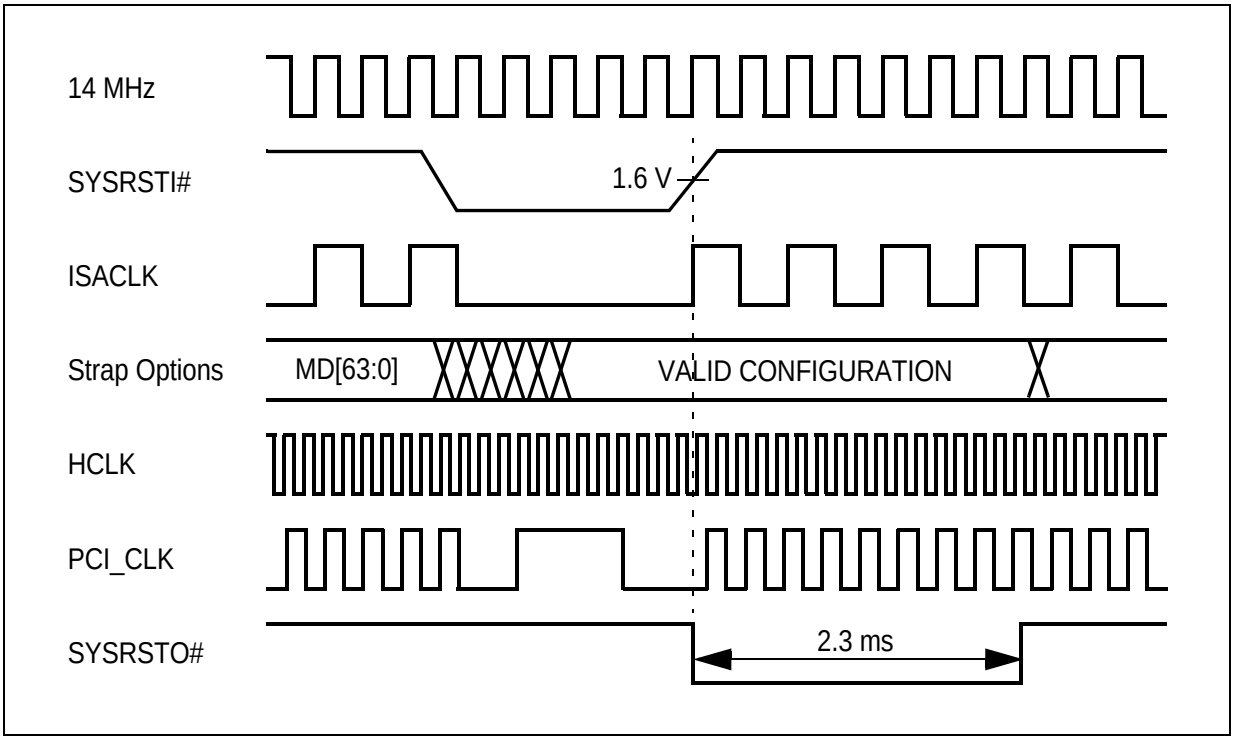
Figure 4-4 describes the reset sequence of the STPC, also called warm reset.

The constraints on the strap options and the bus activities are the same as for the cold reset.
The SYSRSTI# pulse duration must be long enough to have all the strap options stabilized and must be adjusted depending on resistor values.

It is mandatory to have a clean reset pulse without glitches as the STPC could then sample invalid strap option setting and enter into an unpredictable mode.

While SYSRSTI# is active, the PCI clock PLL runs in open loop mode at a speed of few 100's KHz.

Figure 4-4. Reset timing diagram



4.5.3 SDRAM INTERFACE

Figure 4-5, Table 4-6 lists the AC characteristics of the SDRAM interface. The MCLKx clocks are the input clock of the SDRAM devices.

Figure 4-5. Synchronous Read Cycle

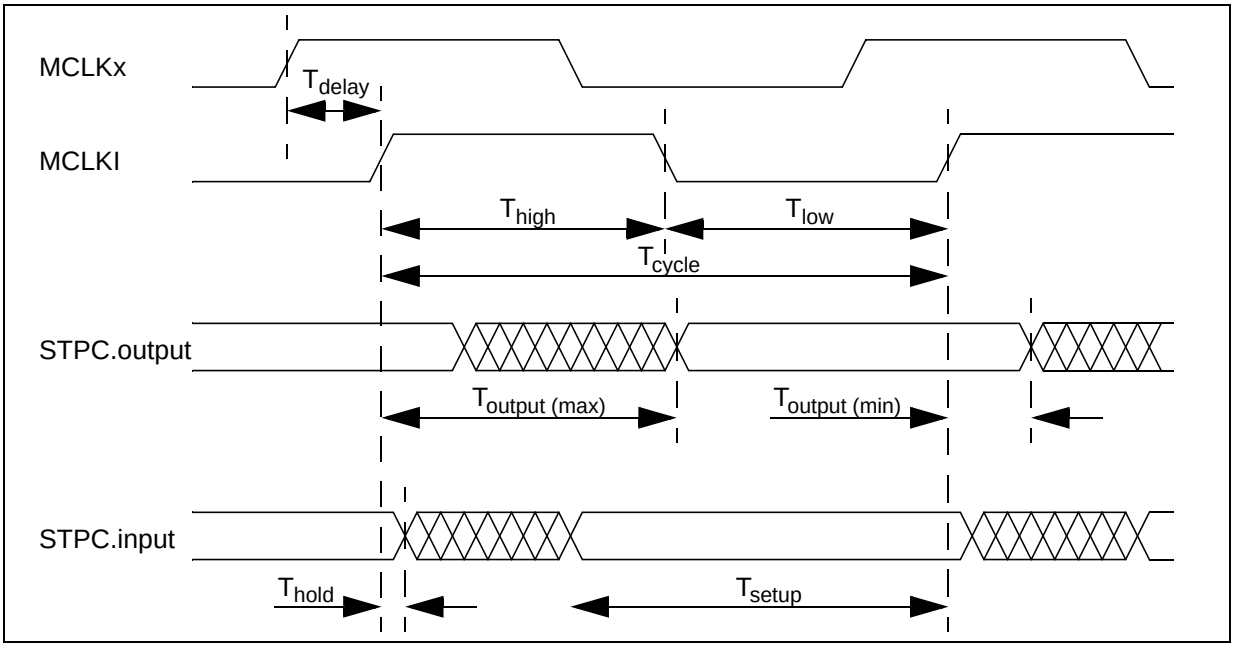


Table 4-6. SDRAM Bus AC Timings

Name	Parameter	Min	Typ	Max	Unit
Tcycle	MCLKI Cycle Time	TBD		TBD	ns
Thigh	MCLKI High Time	TBD		TBD	ns
Tlow	MCLKI Low Time	TBD		TBD	ns
	MCLKI Rising Time	TBD		TBD	ns
	MCLKI Falling Time	TBD		TBD	ns
Tdelay	MCLKx to MCLKI delay	-0,5		2	ns
Toutput	MCLKI to RAS # Valid	1.7		2.4	ns
	MCLKI to CAS # Valid	1.0		1.5	ns
	MCLKI to CS # Valid	0.5		1.3	ns
	MCLKI to DQM[ ] Outputs Valid	0.7		1.8	ns
	MCLKI to MD[ ] Outputs Valid	0.6		1.5	ns
	MCLKI to MA[ ] Outputs Valid	1.2		1.9	ns
	MCLKI to MWE # Valid	1.4		2.2	ns
Tsetup	MD[63:0] setup to MCKLI	1.9		2.3	ns
Thold	MD[63:0] hold from MCKLI	3.6		4.7	ns
Note: These timings are for a load of 50pF.					

For correct operation, the programmable read clock delay (RDCLK) must not be activated.

4.5.4 PCI INTERFACE

Figure 4-6 and Table 4-7. list the AC characteristics of the PCI interface. PCICLKx stands for any PCI device clock input.

Figure 4-6. PCI Timing Diagram

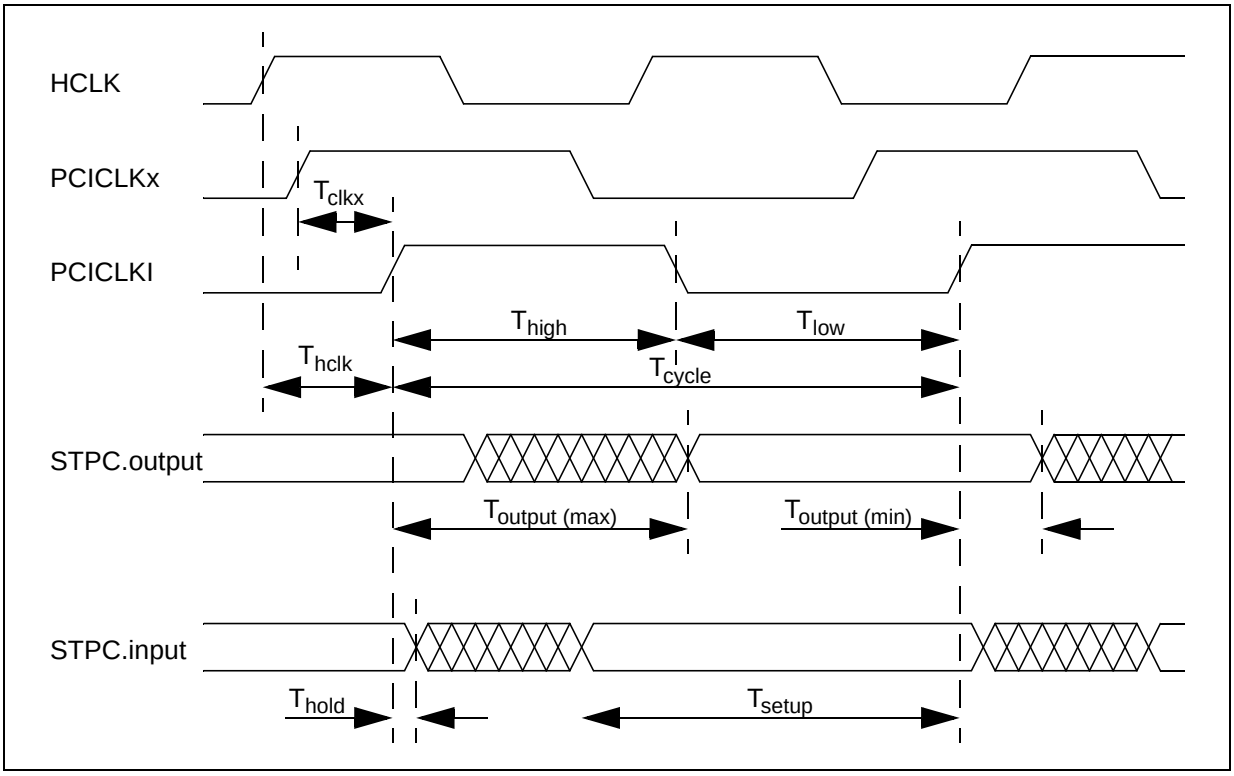


Table 4-7. PCI Bus AC Timings

Name	Parameter	Min	Typ	Max	Unit
	HCLK to PCICLKO delay (MD[30:27] = 0000)	4,30	-	5,50	ns
Thclk	HCLK to PCICLKI delay	-	6	-	ns
Tclkx	PCICLKI to PCICLKx skew	-0.5	0	0.5	ns
Tcycle	PCICLKI Cycle Time	30			ns
Thigh	PCICLKI High Time	13			ns
Tlow	PCICLKI Low Time	13			ns
	PCICLKI Rising Time			1.5	ns
	PCICLKO to PCICLKI delay	0,5	-	1,8	ns
Note: These timings are for a load of 50pF.					

4.5.5 IPC INTERFACE

Table 4-8 lists the AC characteristics of the IPC interface.

Figure 4-7. IPC timing diagram

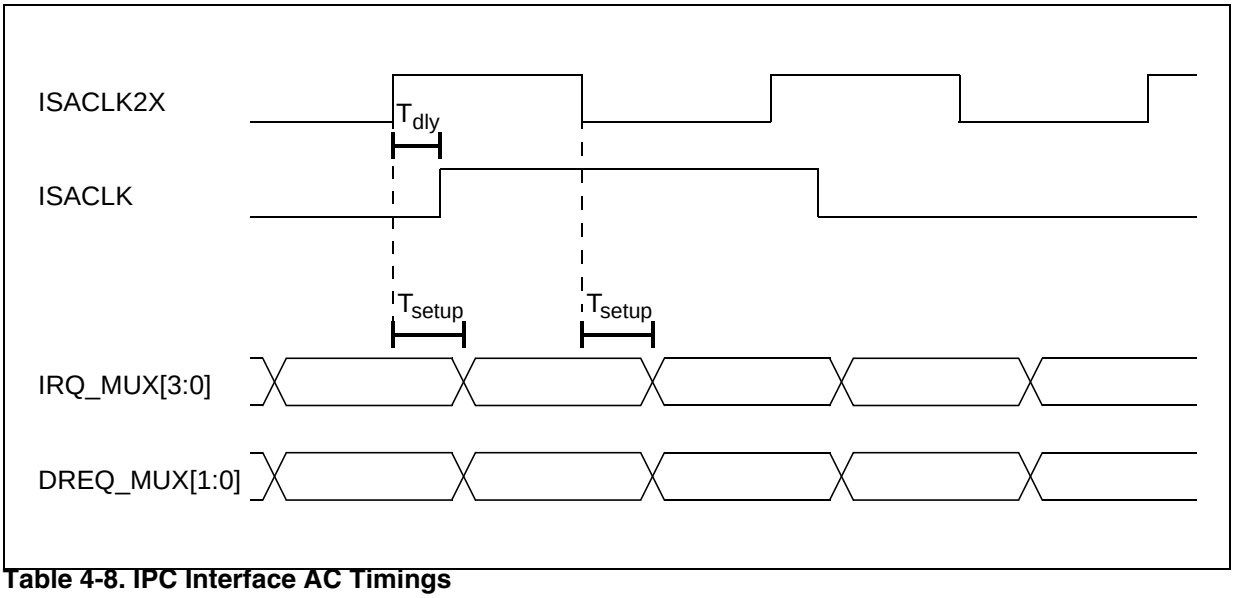


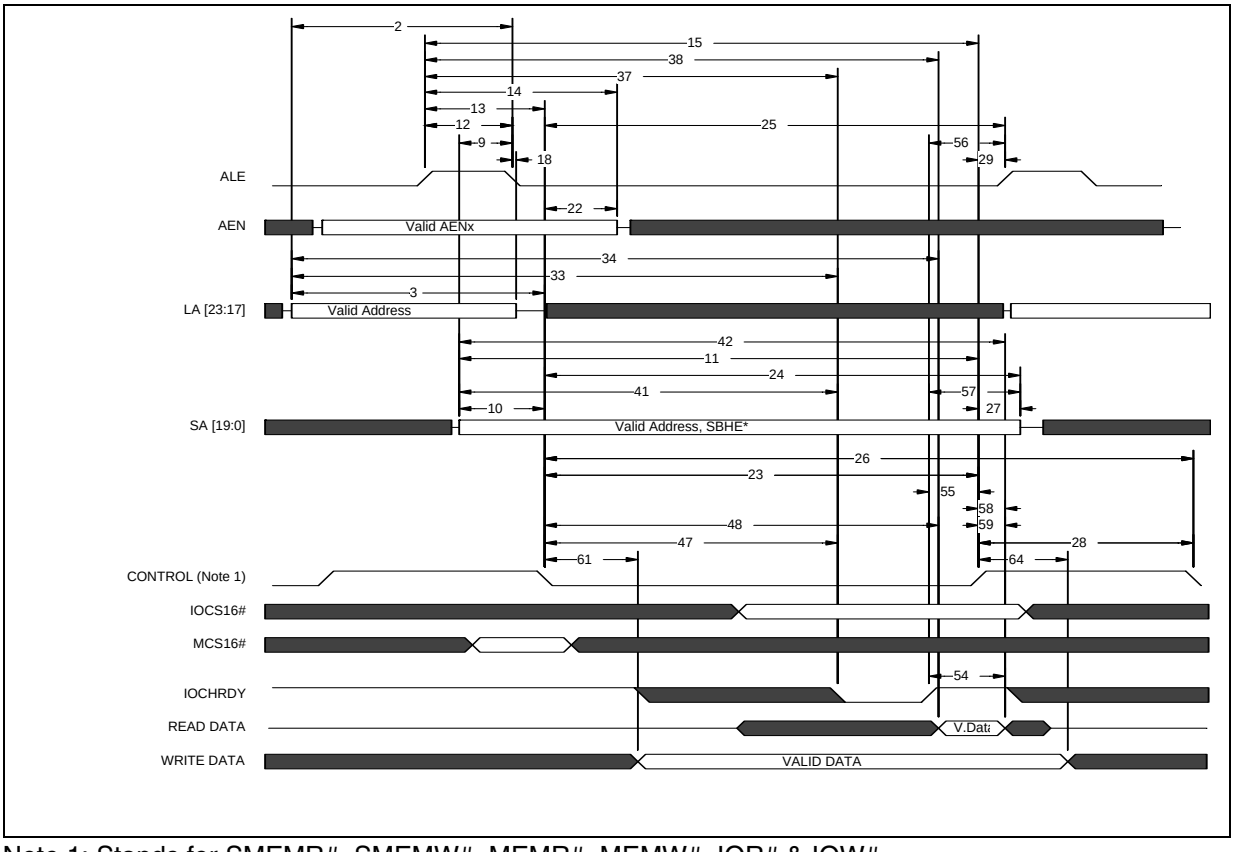
Table 4-8. IPC Interface AC Timings

Name	Parameter	Min	Max	Unit
T_{setup}	IRQ_MUX[3:0] Input setup to ISACLK2X	0	-	nS
T_{setup}	DREQ_MUX[1:0] Input setup to ISACLK2X	0	-	nS

4.5.6 ISA INTERFACE AC TIMING CHARACTERISTICS

Figure 4-8 and Table 4-9 list the AC characteristics of the ISA interface.

Figure 4-8. ISA Cycle (ref Table 4-9.)



Note 1: Stands for SMEMR#, SMEMW#, MEMR#, MEMW#, IOR# & IOW#.

The clock has not been represented as it is dependent on the ISA Slave mode.

Table 4-9. ISA Bus AC Timing

Name	Parameter	Min	Max	Units
2	LA[23:17] valid before ALE# negated	5T		Cycles
3	**LA[23:17] valid before MEMR#, MEMW# asserted**			
3a	Memory access to 16-bit ISA Slave	5T		Cycles
3b	Memory access to 8-bit ISA Slave	5T		Cycles
9	SA[19:0] & SBHE valid before ALE# negated	1T		Cycles
10	**SA[19:0] & SBHE valid before MEMR#, MEMW# asserted**			
10a	Memory access to 16-bit ISA Slave	2T		Cycles
10b	Memory access to 8-bit ISA Slave	2T		Cycles
10	**SA[19:0] & SHBE valid before SMEMR#, SMEMW# asserted**			
10c	Memory access to 16-bit ISA Slave	2T		Cycle
10d	Memory access to 8-bit ISA Slave	2T		Cycle
Note: The signal numbering refers to Figure 4-8				

Table 4-9. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
10e	SA[19:0] & SBHE valid before IOR#, IOW# asserted		2T		Cycles
11	**ISACLK2X to IOW# valid**				
	11a	Memory access to 16-bit ISA Slave - 2BCLK	2T		Cycles
	11b	Memory access to 16-bit ISA Slave - Standard 3BCLK	2T		Cycles
	11c	Memory access to 16-bit ISA Slave - 4BCLK	2T		Cycles
	11d	Memory access to 8-bit ISA Slave - 2BCLK	2T		Cycles
11e		Memory access to 8-bit ISA Slave - Standard 3BCLK	2T		Cycles
12	ALE# asserted before ALE# negated		1T		Cycles
13	**ALE# asserted before MEMR#, MEMW# asserted**				
	13a	Memory Access to 16-bit ISA Slave	2T		Cycles
	13b	Memory Access to 8-bit ISA Slave	2T		Cycles
13	**ALE# asserted before SMEMR#, SMEMW# asserted**				
	13c	Memory Access to 16-bit ISA Slave	2T		Cycles
	13d	Memory Access to 8-bit ISA Slave	2T		Cycles
13e	ALE# asserted before IOR#, IOW# asserted		2T		Cycles
14	**ALE# asserted before AL[23:17]**				
	14a	Non compressed	15T		Cycles
	14b	Compressed	15T		Cycles
15	**ALE# asserted before MEMR#, MEMW#, SMEMR#, SMEMW# negated**				
	15a	Memory Access to 16-bit ISA Slave- 4 BCLK	11T		Cycles
	15e	Memory Access to 8-bit ISA Slave- Standard Cycle	11T		Cycles
18a	ALE# negated before LA[23:17] invalid (non compressed)		14T		Cycles
18a	ALE# negated before LA[23:17] invalid (compressed)		14T		Cycles
22	**MEMR#, MEMW# asserted before LA[23:17]**				
	22a	Memory access to 16-bit ISA Slave.	13T		Cycles
	22b	Memory access to 8-bit ISA Slave.	13T		Cycles
23	**MEMR#, MEMW# asserted before MEMR#, MEMW# negated**				
	23b	Memory access to 16-bit ISA Slave Standard cycle	9T		Cycles
	23e	Memory access to 8-bit ISA Slave Standard cycle	9T		Cycles
23	**SMEMR#, SMEMW# asserted before SMEMR#, SMEMW# negated**				
	23h	Memory access to 16-bit ISA Slave Standard cycle	9T		Cycles
	23l	Memory access to 16-bit ISA Slave Standard cycle	9T		Cycles
23	**IOR#, IOW# asserted before IOR#, IOW# negated**				
	23o	Memory access to 16-bit ISA Slave Standard cycle	9T		Cycles
	23r	Memory access to 8-bit ISA Slave Standard cycle	9T		Cycles
24	**MEMR#, MEMW# asserted before SA[19:0]**				
	24b	Memory access to 16-bit ISA Slave Standard cycle	10T		Cycles
	24d	Memory access to 8-bit ISA Slave - 3BLCK	10T		Cycles
	24e	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
	24f	Memory access to 8-bit ISA Slave - 7BCLK	10T		Cycles
24	**SMEMR#, SMEMW# asserted before SA[19:0]**				
	24h	Memory access to 16-bit ISA Slave Standard cycle	10T		Cycles
	24i	Memory access to 16-bit ISA Slave - 4BCLK	10T		Cycles
	24k	Memory access to 8-bit ISA Slave - 3BCLK	10T		Cycles
Note: The signal numbering refers to Figure 4-8					

Table 4-9. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
	24l	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
24	**IOR#, IOW# asserted before SA[19:0]**				
	24o	I/O access to 16-bit ISA Slave Standard cycle	19T		Cycles
	24r	I/O access to 16-bit ISA Slave Standard cycle	19T		Cycles
25	**MEMR#, MEMW# asserted before next ALE# asserted**				
	25b	Memory access to 16-bit ISA Slave Standard cycle	10T		Cycles
	25d	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
25	**SMEMR#, SMEMW# asserted before next ALE# asserted**				
	25e	Memory access to 16-bit ISA Slave - 2BCLK	10T		Cycles
	25f	Memory access to 16-bit ISA Slave Standard cycle	10T		Cycles
	25h	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
25	**IOR#, IOW# asserted before next ALE# asserted**				
	25i	I/O access to 16-bit ISA Slave Standard cycle	10T		Cycles
	25k	I/O access to 16-bit ISA Slave Standard cycle	10T		Cycles
26	**MEMR#, MEMW# asserted before next MEMR#, MEMW# asserted**				
	26b	Memory access to 16-bit ISA Slave Standard cycle	12T		Cycles
	26d	Memory access to 8-bit ISA Slave Standard cycle	12T		Cycles
26	**SMEMR#, SMEMW# asserted before next SMEMR#, SMEMW# asserted**				
	26f	Memory access to 16-bit ISA Slave Standard cycle	12T		Cycles
	26h	Memory access to 8-bit ISA Slave Standard cycle	12T		Cycles
26	**IOR#, IOW# asserted before next IOR#, IOW# asserted**				
	26i	I/O access to 16-bit ISA Slave Standard cycle	12T		Cycles
	26k	I/O access to 8-bit ISA Slave Standard cycle	12T		Cycles
28	**Any command negated to MEMR#, SMEMR#, MEMR#, SMEMW# asserted**				
	28a	Memory access to 16-bit ISA Slave	3T		Cycles
	28b	Memory access to 8-bit ISA Slave	3T		Cycles
28	**Any command negated to IOR#, IOW# asserted**				
	28c	I/O access to ISA Slave	3T		Cycles
29a	MEMR#, MEMW# negated before next ALE# asserted		1T		Cycles
29b	SMEMR#, SMEMW# negated before next ALE# asserted		1T		Cycles
29c	IOR#, IOW# negated before next ALE# asserted		1T		Cycles
33	**LA[23:17] valid to IOCHRDY negated**				
	33a	Memory access to 16-bit ISA Slave - 4 BCLK	8T		Cycles
	33b	Memory access to 8-bit ISA Slave - 7 BCLK	14T		Cycles
34	**LA[23:17] valid to read data valid**				
	34b	Memory access to 16-bit ISA Slave Standard cycle	8T		Cycles
	34e	Memory access to 8-bit ISA Slave Standard cycle	14T		Cycles
37	**ALE# asserted to IOCHRDY# negated**				
	37a	Memory access to 16-bit ISA Slave - 4 BCLK	6T		Cycles
	37b	Memory access to 8-bit ISA Slave - 7 BCLK	12T		Cycles
	37c	I/O access to 16-bit ISA Slave - 4 BCLK	6T		Cycles
	37d	I/O access to 8-bit ISA Slave - 7 BCLK	12T		Cycles
38	**ALE# asserted to read data valid**				
	38b	Memory access to 16-bit ISA Slave Standard Cycle	4T		Cycles
Note: The signal numbering refers to Figure 4-8					

Table 4-9. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
	38e	Memory access to 8-bit ISA Slave Standard Cycle	10T		Cycles
	38h	I/O access to 16-bit ISA Slave Standard Cycle	4T		Cycles
	38l	I/O access to 8-bit ISA Slave Standard Cycle	10T		Cycles
41	**SA[19:0] SBHE valid to IOCHRDY negated**				
	41a	Memory access to 16-bit ISA Slave	6T		Cycles
	41b	Memory access to 8-bit ISA Slave	12T		Cycles
	41c	I/O access to 16-bit ISA Slave	6T		Cycles
	41d	I/O access to 8-bit ISA Slave	12T		Cycles
42	**SA[19:0] SBHE valid to read data valid**				
	42b	Memory access to 16-bit ISA Slave Standard cycle	4T		Cycles
	42e	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
	42h	I/O access to 16-bit ISA Slave Standard cycle	4T		Cycles
	42l	I/O access to 8-bit ISA Slave Standard cycle	10T		Cycles
47	**MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW# asserted to IOCHRDY negated**				
	47a	Memory access to 16-bit ISA Slave	2T		Cycles
	47b	Memory access to 8-bit ISA Slave	5T		Cycles
	47c	I/O access to 16-bit ISA Slave	2T		Cycles
	47d	I/O access to 8-bit ISA Slave	5T		Cycles
48	**MEMR#, SMEMR#, IOR# asserted to read data valid**				
	48b	Memory access to 16-bit ISA Slave Standard Cycle	2T		Cycles
	48e	Memory access to 8-bit ISA Slave Standard Cycle	5T		Cycles
	48h	I/O access to 16-bit ISA Slave Standard Cycle	2T		Cycles
	48l	I/O access to 8-bit ISA Slave Standard Cycle	5T		Cycles
54	**IOCHRDY asserted to read data valid**				
	54a	Memory access to 16-bit ISA Slave	1T(R)/2T(W)		Cycles
	54b	Memory access to 8-bit ISA Slave	1T(R)/2T(W)		Cycles
	54c	I/O access to 16-bit ISA Slave	1T(R)/2T(W)		Cycles
	54d	I/O access to 8-bit ISA Slave	1T(R)/2T(W)		Cycles
55a	IOCHRDY asserted to MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW# negated		1T		Cycles
55b	IOCHRY asserted to MEMR#, SMEMR# negated (refresh)		1T		Cycles
56	IOCHRDY asserted to next ALE# asserted		2T		Cycles
57	IOCHRDY asserted to SA[19:0], SBHE invalid		2T		Cycles
58	MEMR#, IOR#, SMEMR# negated to read data invalid		0T		Cycles
59	MEMR#, IOR#, SMEMR# negated to data bus float		0T		Cycles
61	**Write data before MEMW# asserted**				
	61a	Memory access to 16-bit ISA Slave	2T		Cycles
	61b	Memory access to 8-bit ISA Slave (Byte copy at end of start)	2T		Cycles
61	**Write data before SMEMW# asserted**				
	61c	Memory access to 16-bit ISA Slave	2T		Cycles
	61d	Memory access to 8-bit ISA Slave	2T		Cycles
61	**Write Data valid before IOW# asserted**				
	61e	I/O access to 16-bit ISA Slave	2T		Cycles
	61f	I/O access to 8-bit ISA Slave	2T		Cycles
Note: The signal numbering refers to Figure 4-8					

Table 4-9. ISA Bus AC Timing

Name	Parameter	Min	Max	Units
64a	MEMW# negated to write data invalid - 16-bit	1T		Cycles
64b	MEMW# negated to write data invalid - 8-bit	1T		Cycles
64c	SMEMW# negated to write data invalid - 16-bit	1T		Cycles
64d	SMEMW# negated to write data invalid - 8-bit	1T		Cycles
64e	IOW# negated to write data invalid	1T		Cycles
64f	MEMW# negated to copy data float, 8-bit ISA Slave, odd Byte by ISA Master	1T		Cycles
64g	IOW# negated to copy data float, 8-bit ISA Slave, odd Byte by ISA Master	1T		Cycles
Note: The signal numbering refers to Figure 4-8				

4.5.7 LOCAL BUS INTERFACE

Figure 4-9 to Figure 4-12 and Table 4-11 list the AC characteristics of the Local Bus interface.

Figure 4-9. Synchronous Read Cycle

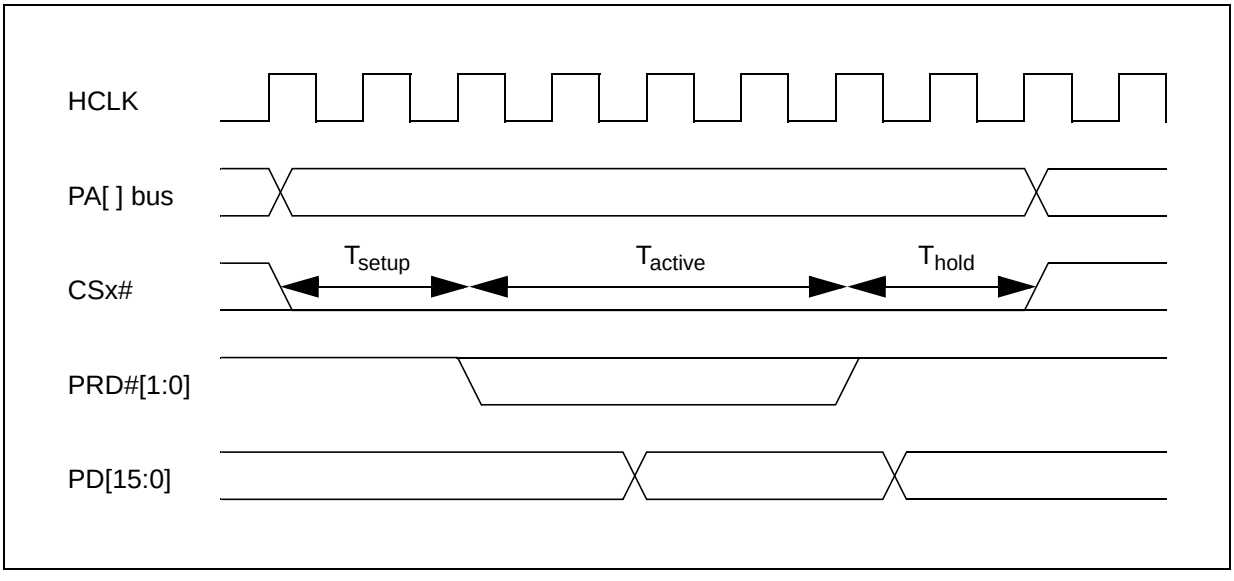


Figure 4-10. Asynchronous Read Cycle

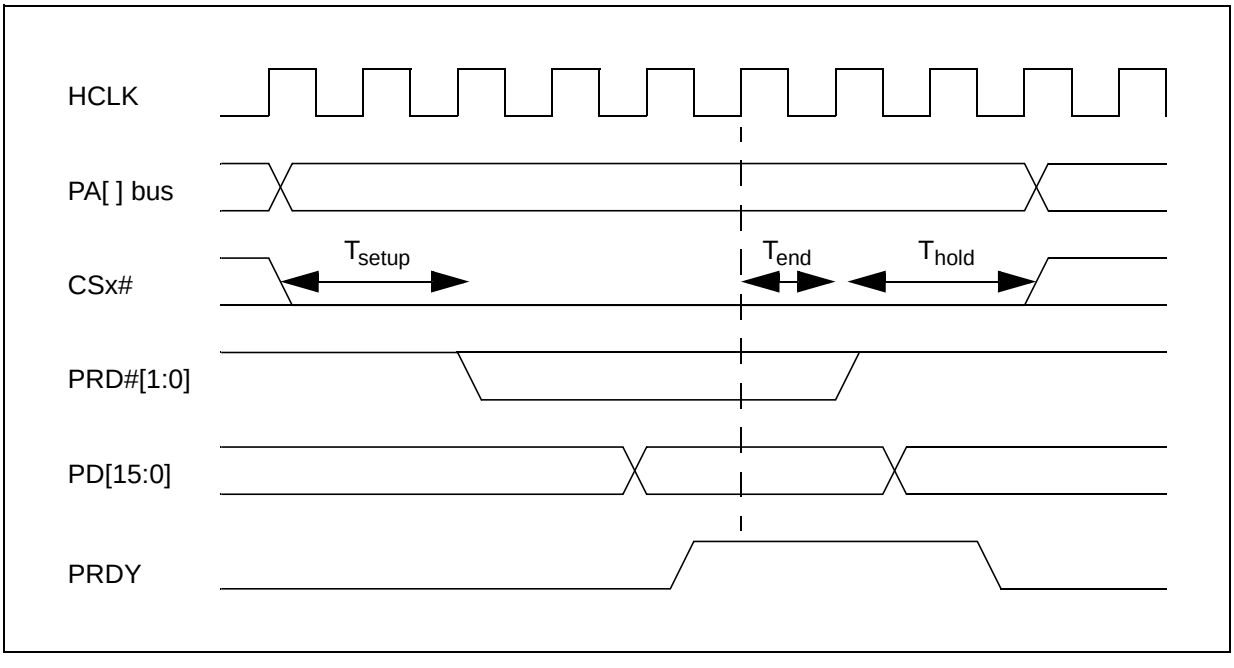


Figure 4-11. Synchronous Write Cycle

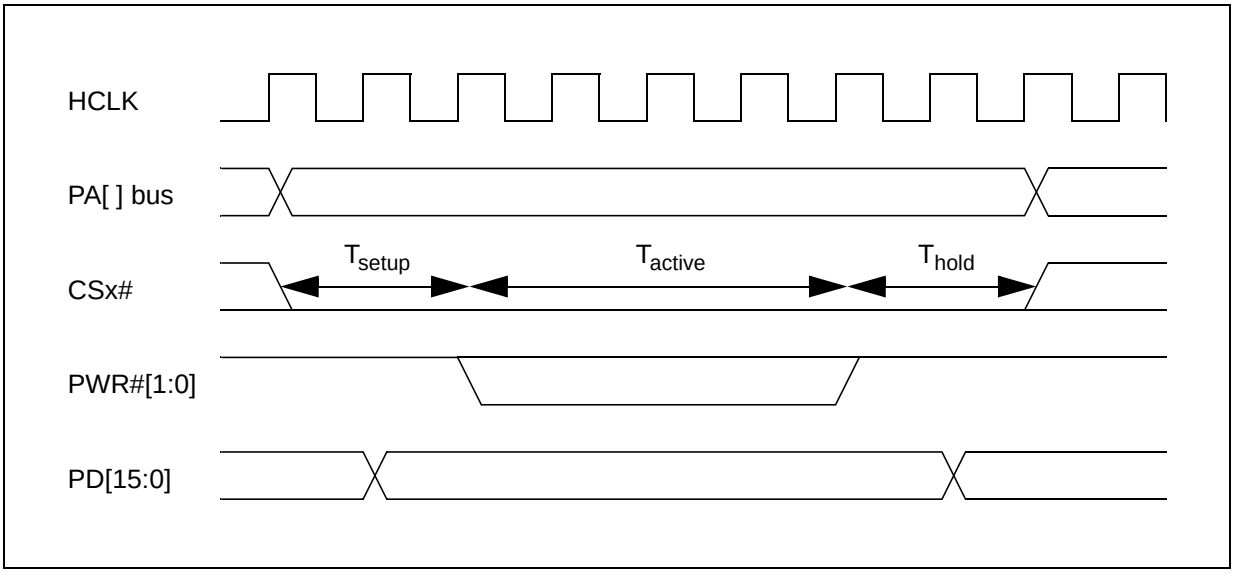
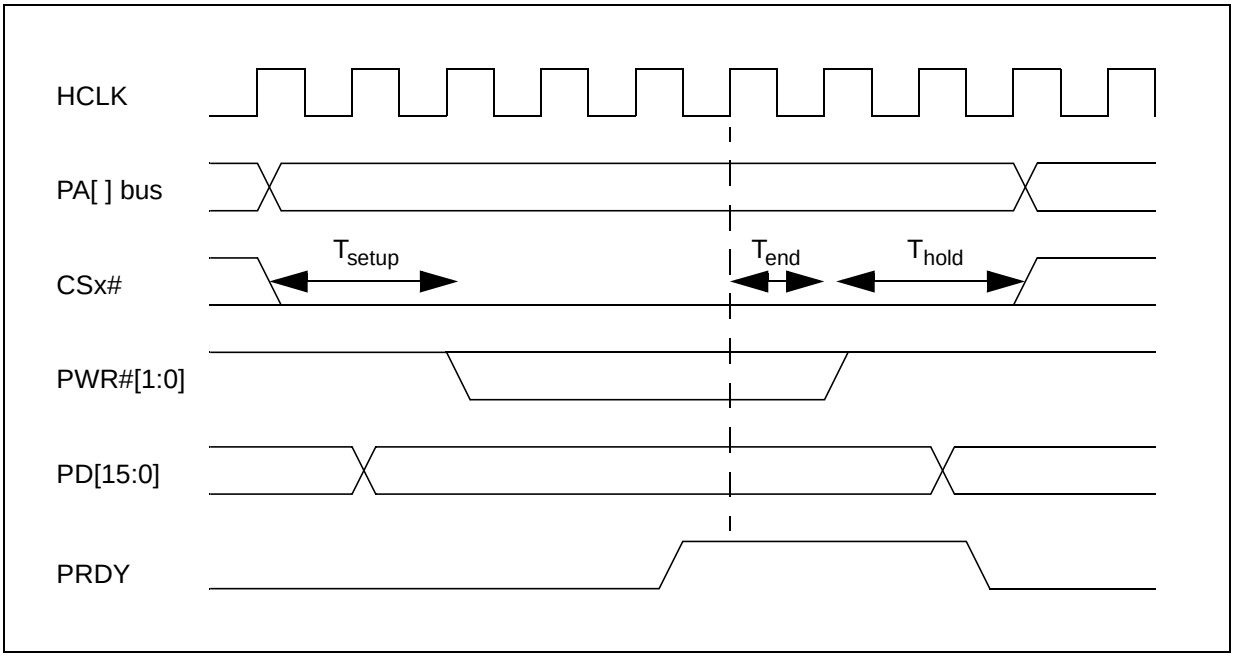


Figure 4-12. Asynchronous Write Cycle



The Table 4-10. below refers to Vh, Va, Vs which are the register value for Setup time, Active Time and Hold time, as described in the Programming Manual.

Table 4-10. Local Bus cycle lenght

Cycle	T_{setup}	T_{active}	T_{hold}	T_{end}	Unit
Memory (FCSx#)	4 + Vh	2 + Va	4 + Vs	4	HCLK
Peripheral (IOCSx#)	8 + Vh	3 + Va	4 + Vs	4	HCLK

Table 4-11. Local Bus Interface AC Timing

Name	Parameters	Min	Max	Units
	HCLK to PA bus	-	15	nS
	HCLK to PD bus	-	15	nS
	HCLK to FCS#[1:0]	-	15	nS
	HCLK to IOCS#[3:0]	-	15	nS
	HCLK to PWR#[1:0]	-	15	nS
	HCLK to PRD#[1:0]	-	15	nS
	PD[15:0] Input setup to HCLK	-	4	nS
	PD[15:0] Input hold to HCLK	2	-	nS
	PRDY Input setup to HCLK	-	4	nS
	PRDY Input hold to HCLK	2	-	nS

4.5.8 USB INTERFACE

The USB interface integrated into the STPC device is compliant with the USB 1.1 standard.

4.5.9 JTAG INTERFACE

Figure 4-13 and Table 4-12 list the AC characteristics of the JTAG interface.

Figure 4-13. JTAG timing diagram

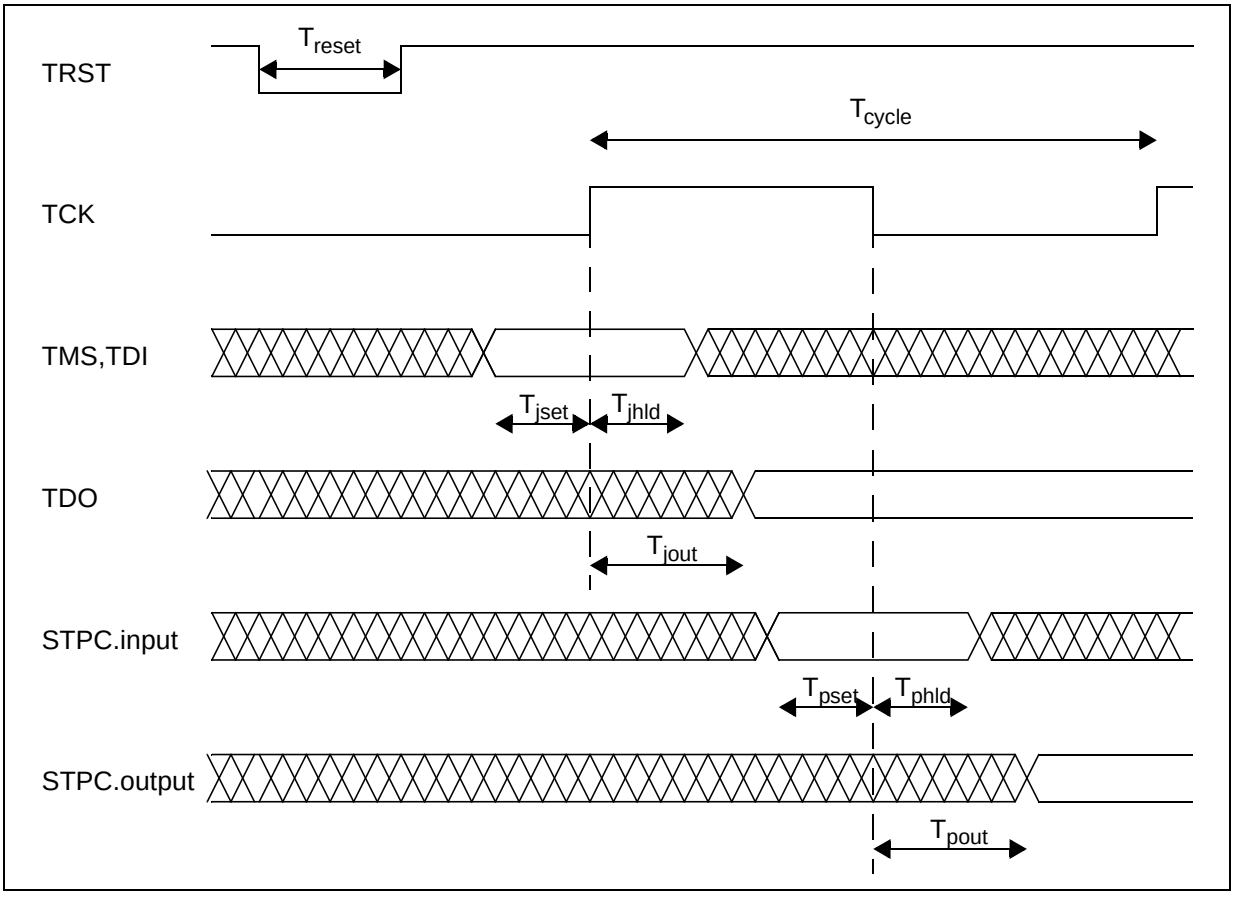


Table 4-12. JTAG AC Timings

Name	Parameter	Min	Max	Unit
Treset	TRST pulse width	1		Tcycle
Tcycle	TCLK period	400		ns
	TCLK rising time		20	ns
	TCLK falling time		20	ns
Tjset	TMS setup time	200		ns
Tjhld	TMS hold time	200		ns
Tjset	TDI setup time	200		ns
Tjhld	TDI hold time	200		ns
Tjout	TCLK to TDO valid		30	ns
Tpset	STPC pin setup time	30		ns
Tphld	STPC pin hold time	30		ns
Tpout	TCLK to STPC pin valid		30	ns

4.5.10 I²C INTERFACE

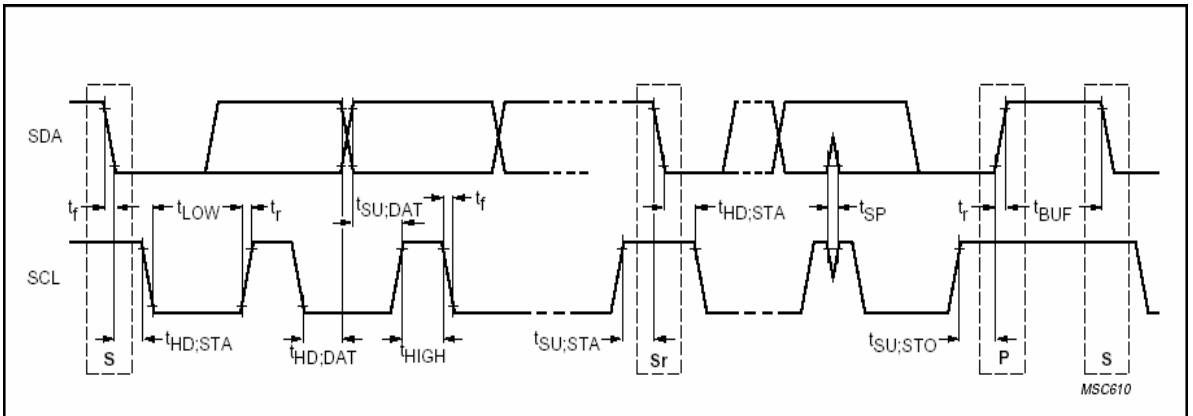
Figure 4-14 and Table 4-13. lists the AC typical characteristics of the I²C interface. All timings are measured when the STPC VEGA operate as master.

Table 4-13. I²C AC Timings

MASTER

PARAMETER	SYMBOL	STANDARD-MODE	FAST-MODE	UNIT
		Typical value	Typical value	
SCL clock frequency.	f_{SCL}	103	390	kHz
Hold time START condition.	$t_{HD;STA}$	9,5	1,8	µs
LOW period of the SCL clock.	t_{LOW}	4,9	1,5	µs
HIGH period of the SCL clock.	t_{HIGH}	4,2	1,12	µs
Set-up time for a repeated START condition.	$t_{SU;STA}$	9,5	1,63	µs
Data Hold time.	$t_{HD;DAT}$	212	380	ns
Data set-up time.	$t_{SU;DAT}$	5	1,38	µs
Rise time of SCL and SDA signals.	t_r	800	152	ns
Fall time of SCL and SDA signals.	t_f	25	38	ns
Set-up time for STOP condition.	$t_{SU;STO}$	308	312	ns
Bus free time between a STOP and START condition	t_{BUF}	70	17,44	µs

Figure 4-14. I²C Timing Diagram.



Definition of timing for F/S-mode devices on the I²C-bus.

5 MECHANICAL DATA

5.1 388-PIN PACKAGE DIMENSIONS

The pin numbering for the STPC 388-pin Plastic BGA package is shown in Figure 5-1.

Dimensions are shown in Figure 5-2, Table 5-1. and Figure 5-3, Table 5-2..

Figure 5-1. 388-Pin PBGA Package - Top View

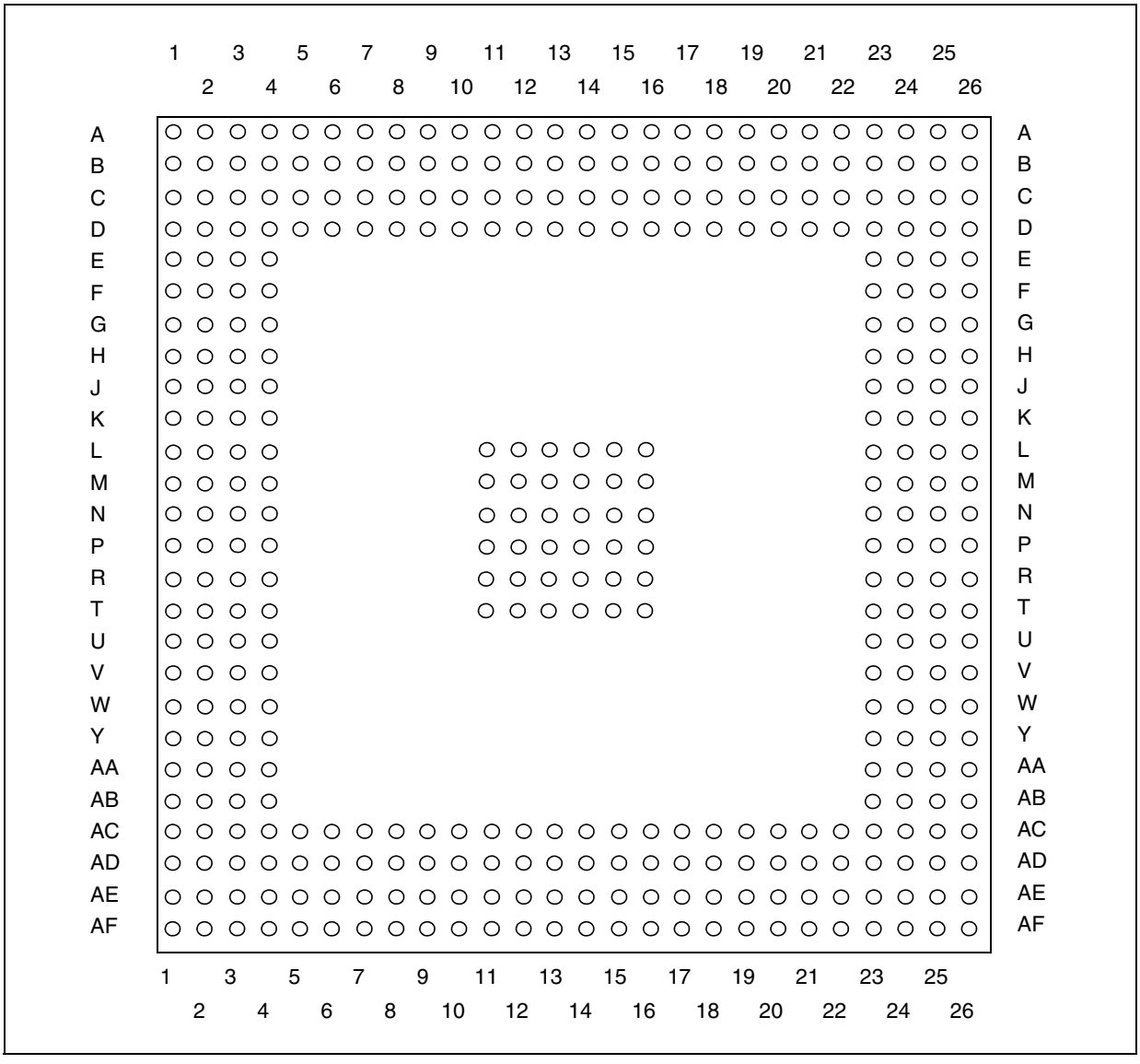


Figure 5-2. 388-pin PBGA Package - PCB Dimensions

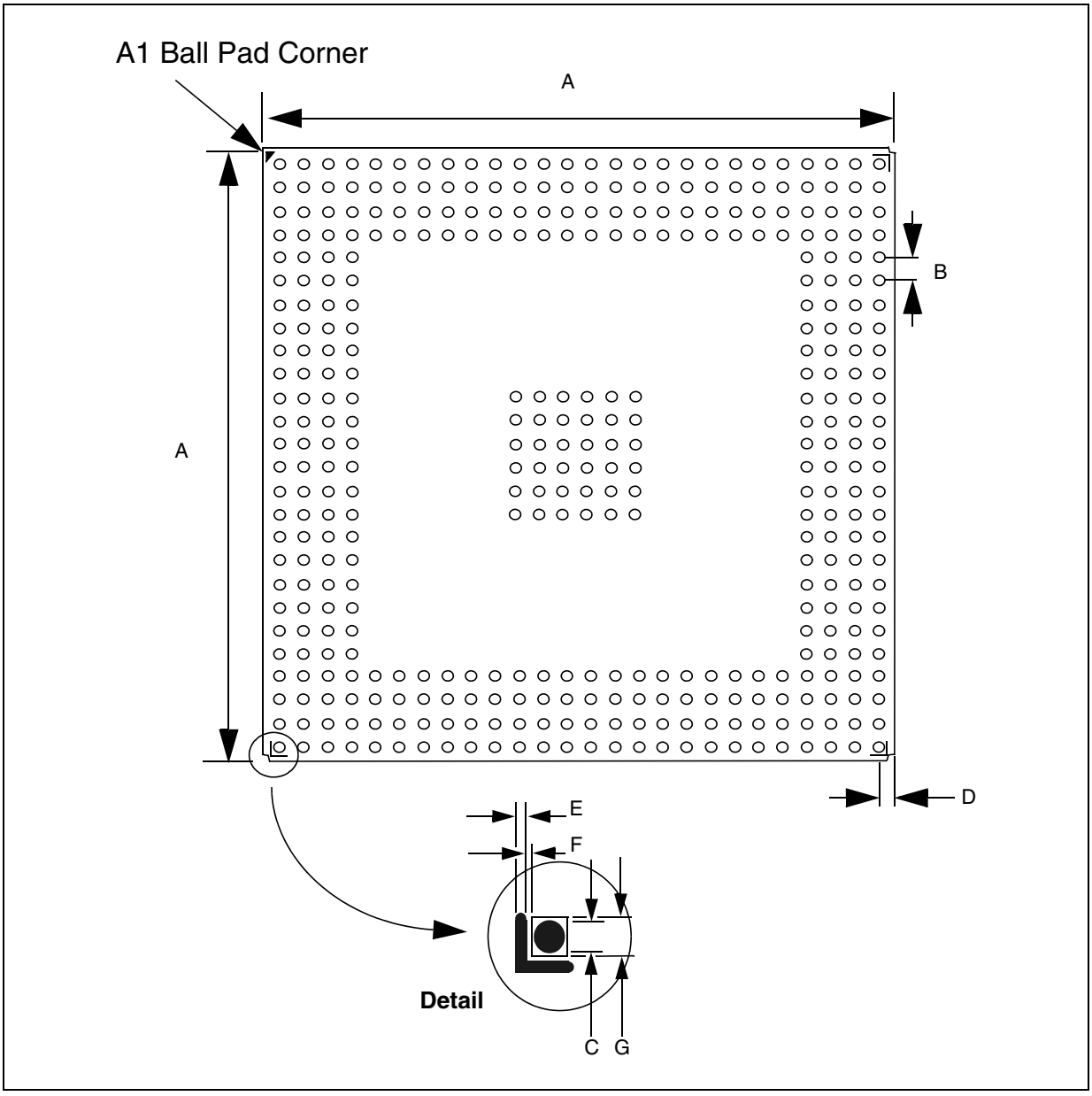


Table 5-1. 388-pin PBGA Package - PCB Dimensions

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	34.95	35.00	35.05	1.375	1.378	1.380
B	1.22	1.27	1.32	0.048	0.050	0.052
C	0.58	0.63	0.68	0.023	0.025	0.027
D	1.57	1.62	1.67	0.062	0.064	0.066
E	0.15	0.20	0.25	0.006	0.008	0.001
F	0.05	0.10	0.15	0.002	0.004	0.006
G	0.75	0.80	0.85	0.030	0.032	0.034

Figure 5-3. 388-pin PBGA Package - Dimensions

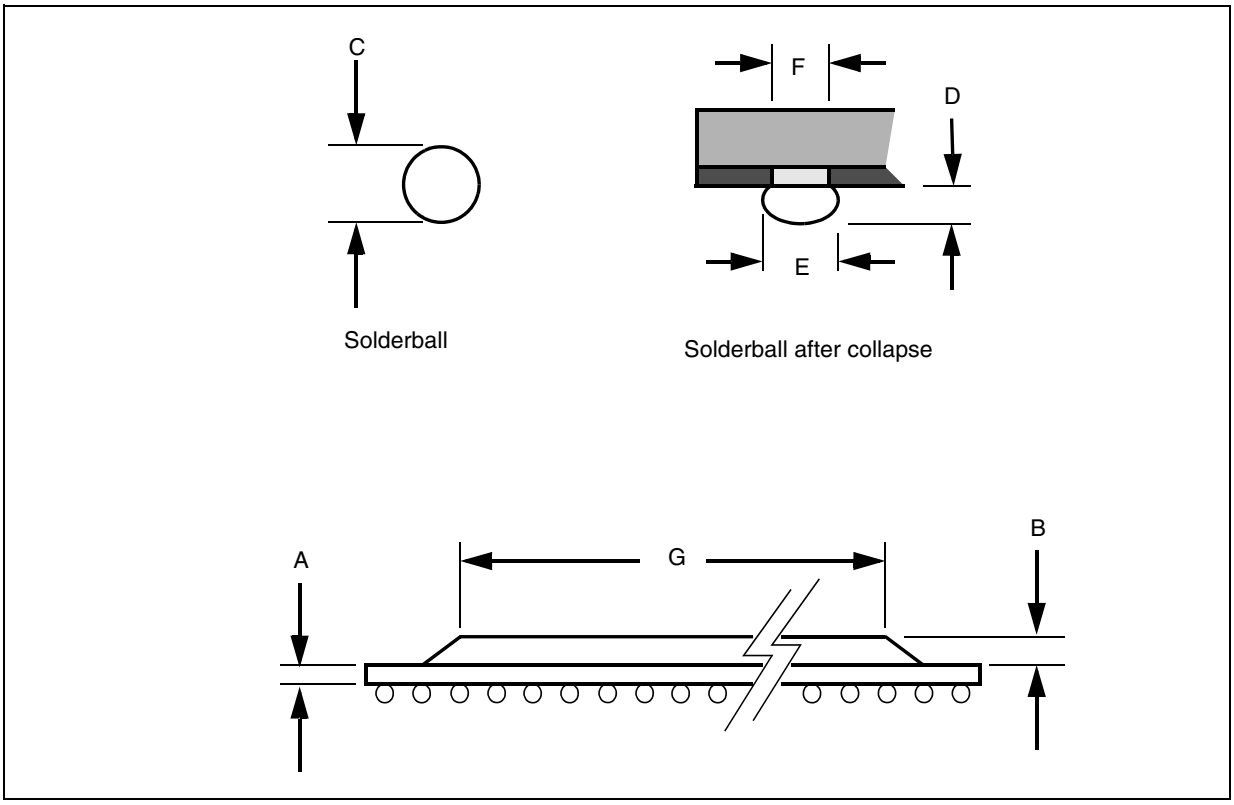


Table 5-2. 388-pin PBGA Package - Dimensions

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.56	0.62	0.020	0.022	0.024
B	1.12	1.17	1.22	0.044	0.046	0.048
C	0.60	0.76	0.92	0.024	0.030	0.036
D	0.52	0.53	0.54	0.020	0.021	0.022
E	0.63	0.78	0.93	0.025	0.031	0.037
F	0.60	0.63	0.66	0.024	0.025	0.026
G		30.0			11.8	

5.2 388-PIN PACKAGE THERMAL DATA

The 388-pin PBGA package has a Power Dissipation Capability of 4.5W. This increases to 6W when used with a Heatsink.

The structure in shown in Figure 5-4.

Thermal dissipation options are illustrated in Figure 5-5 and Figure 5-6.

Figure 5-4. 388-Pin PBGA structure

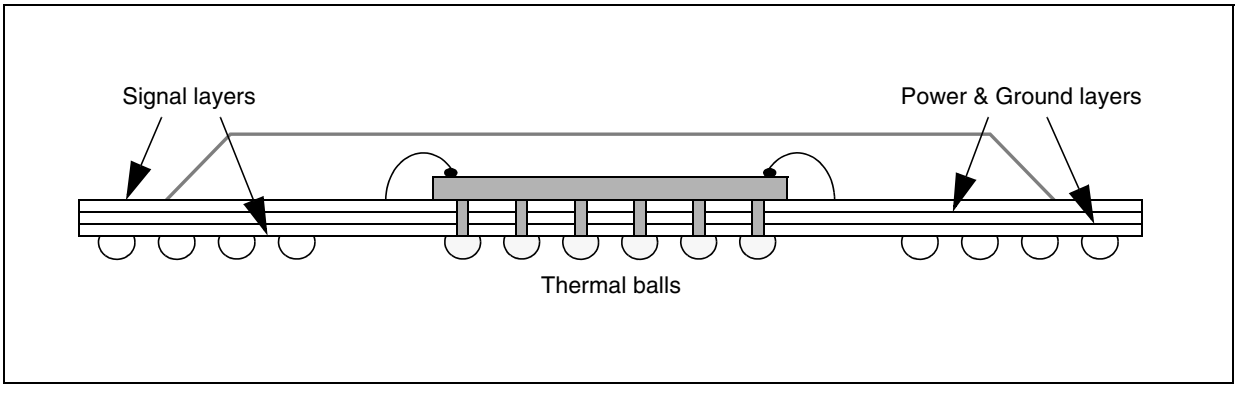


Figure 5-5. Thermal Dissipation Without Heatsink

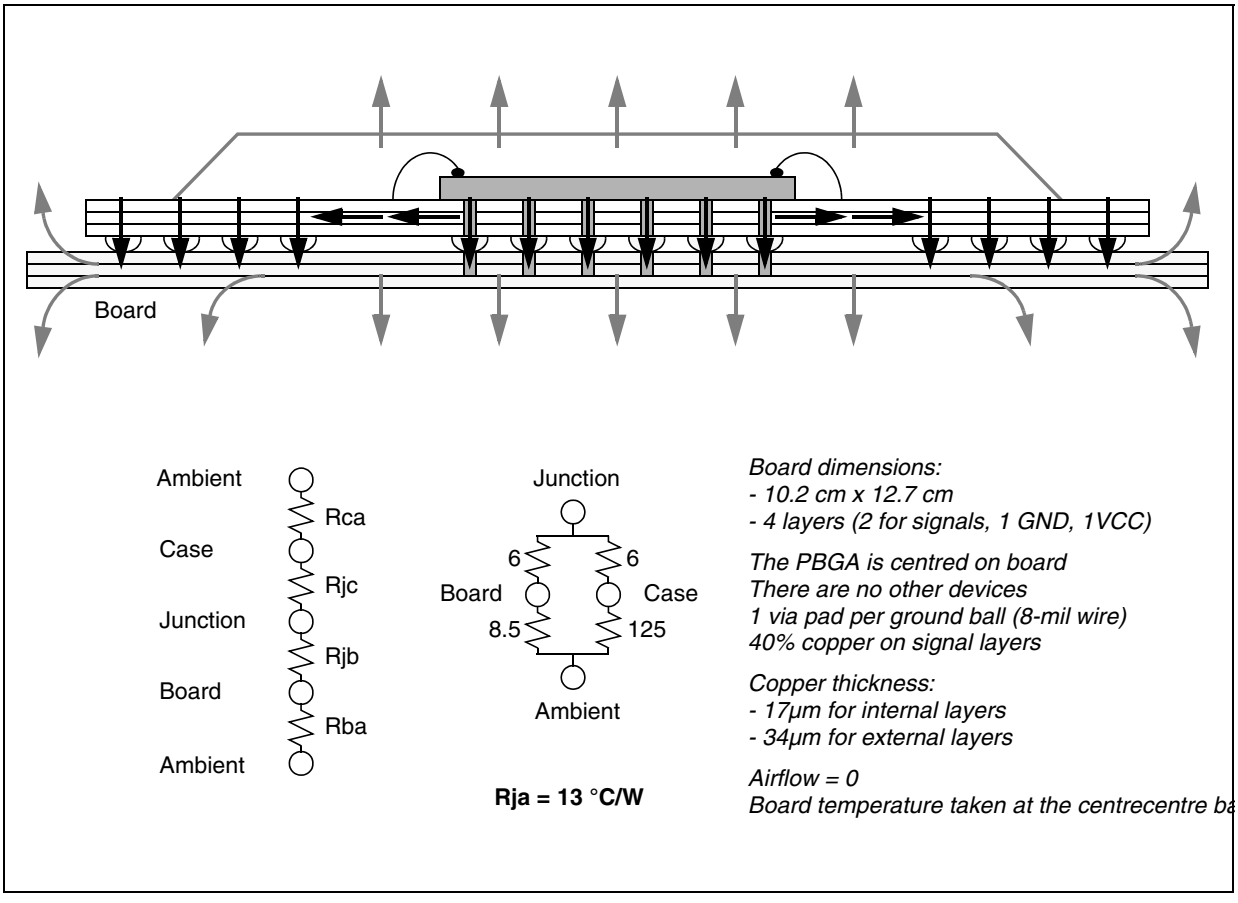
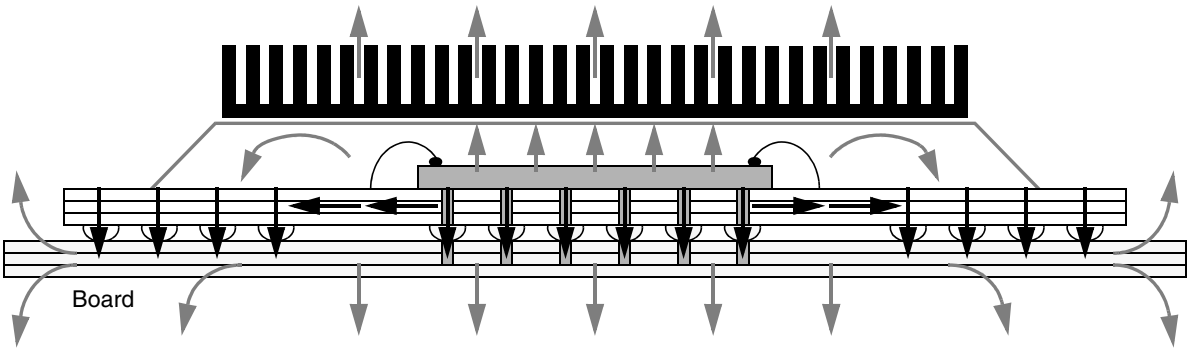
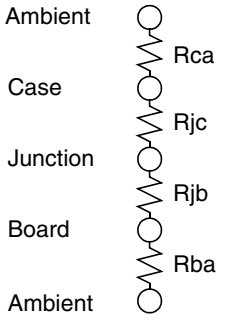
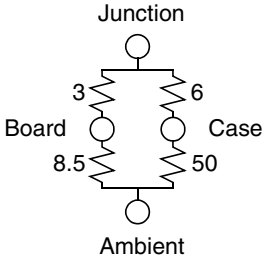


Figure 5-6. Thermal Dissipation With Heatsink







Rja = 9.5 °C/W

Board dimensions:
- 10.2 cm x 12.7 cm
- 4 layers (2 for signals, 1 GND, 1VCC)

The PBGA is centred on board
There are no other devices
1 via pad per ground ball (8-mil wire)
40% copper on signal layers

Copper thickness:
- 17µm for internal layers
- 34µm for external layers

Airflow = 0
Board temperature taken at the centre balls
Heat sink is 11.1°C/W

5.3 SOLDERING RECOMMENDATIONS

High quality, low defect soldering requires identifying the **optimum temperature profile** for reflowing the solder paste, therefore optimizing the process. The heating and cooling rise rates must be compatible with the solder paste and components. A typical profile consists of a preheat, dryout, reflow and cooling sections.

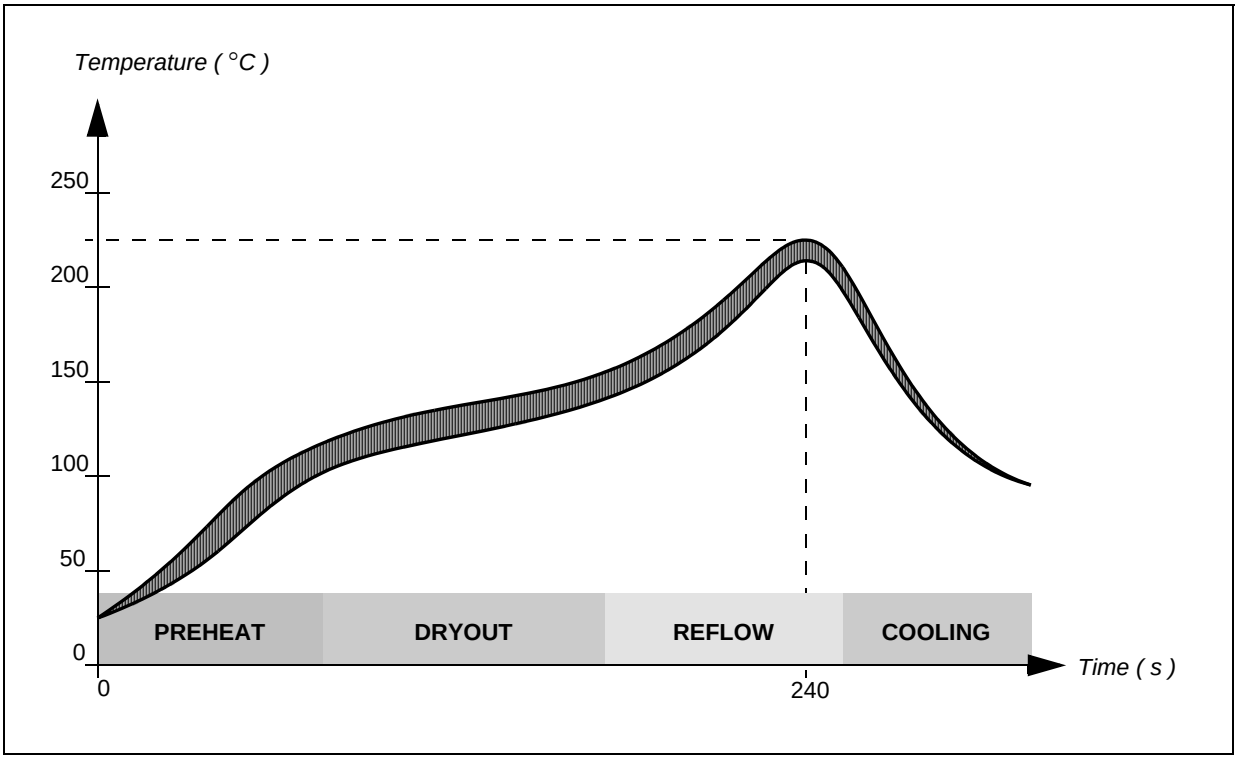
The most critical parameter in the **preheat section** is to minimize the rate of temperature rise to less than 2°C / second, in order to minimize thermal shock on the semi-conductor components.

Dryout section is used primarily to ensure that the solder paste is fully dried before hitting reflow temperatures.

Solder reflow is accomplished in the **reflow zone**, where the solder paste is elevated to a temperature greater than the melting point of the solder. Melting temperature must be exceeded by approximately 20°C to ensure quality reflow.

In reality the profile is not a line, but rather **a range of temperatures** all solder joints must be exposed. The total temperature deviation from component thermal mismatch, oven loading and oven uniformity must be within the band.

Figure 5-7. Reflow soldering temperature range



6 DESIGN GUIDELINES

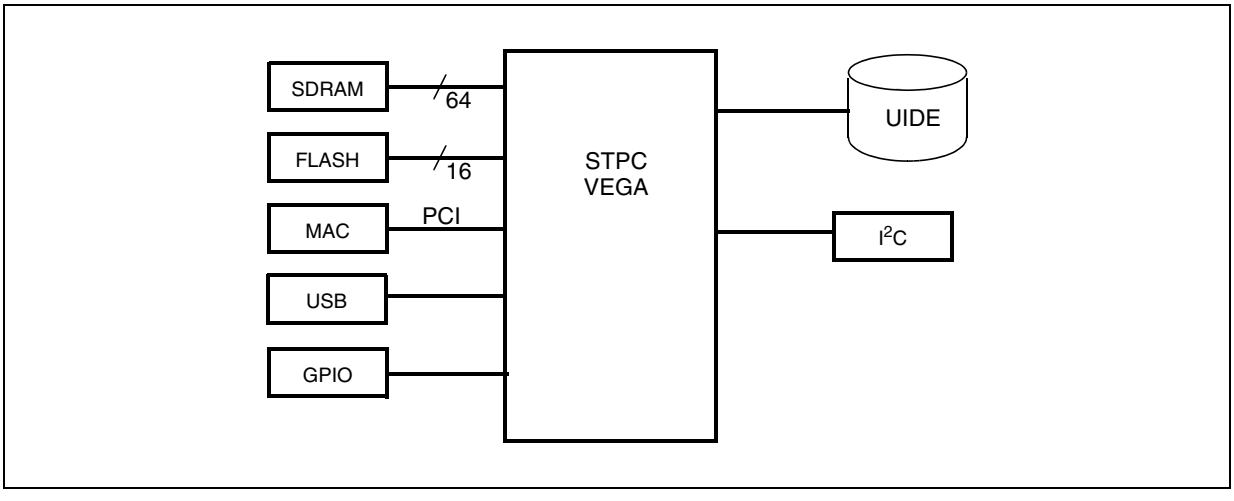
6.1 TYPICAL APPLICATIONS

The STPC Vega is well suited for many display-less applications or together with a PCI graphics/ video device. Some of the possible implementations are described below.

6.1.1 FILE SERVER

A file server is a MAC Ethernet hot-pluggable system that enables the user to obtain additional disk capacity with great flexibility.

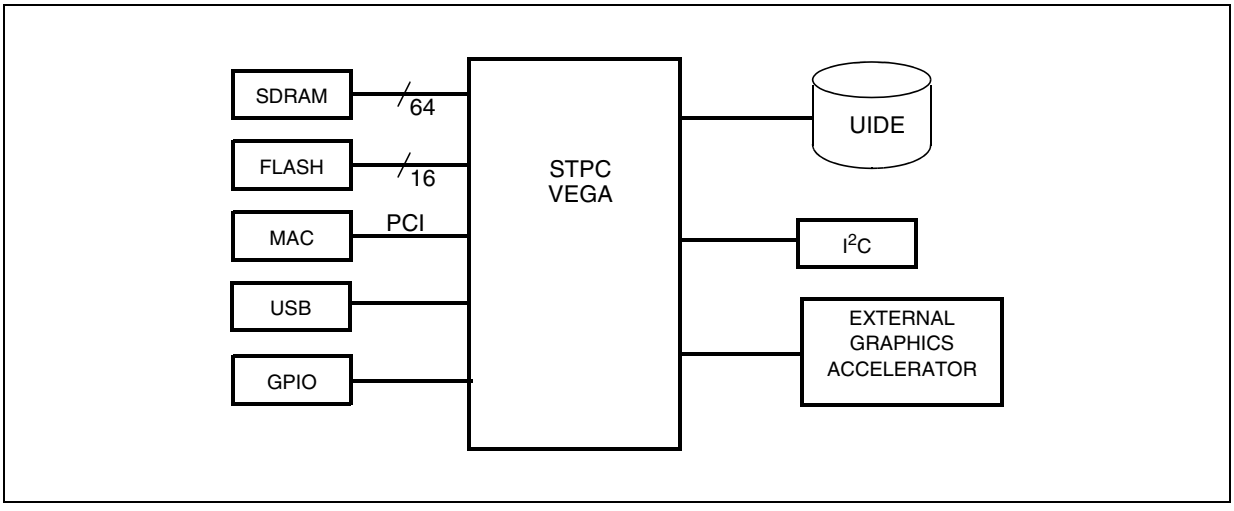
Figure 6-1. File Server



6.1.2 GRAPHICS TERMINAL

An external Graphics accelerator can be added to the STPC Vega on the PCI interface in order to take advantage of specific graphics requirements and added integration of the STPC Vega

Figure 6-2. Graphics Terminal



6.2 STPC CONFIGURATION

The STPC is a very flexible product with decoupled clock domains and strap options enabling a user-optimized configuration.

As some trade-offs are often necessary, it is important to do an analysis of the application needs prior to design a system based on this product. The application constraints are usually the following:
- CPU performance
- graphics / video performance
- power consumption
- PCI bandwidth
- booting time
- EMC

Some other elements can help to tune the choice:
- Code size of CPU Consuming tasks
- Data size and location

On the STPC side, the configurable parameters are the following:
- Synchronous / asynchronous mode
- HCLK speed
- MCLK speed
- CPU Clock Ratios (X2,X2.5, X3, X3.5)
- Local Bus / ISA bus

6.2.1 LOCAL BUS / ISA BUS

The selection between the ISA bus and the Local Bus is relatively simple. The first one is a standard bus but slow. The Local Bus is fast and programmable but doesn't support any DMA nor external master mechanisms. Table 6-1 below summarizes the selection:

Table 6-1. Bus mode selection

Need	Selection
Legacy I/O device (Floppy, ...), Super I/O	ISA Bus
DMA capability (Soundblaster)	ISA Bus
Flash, SRAM, basic I/O device	Local Bus
Fast boot	Local Bus
Boot flash of 4MB or more	Local Bus
Programmable Chip Select	Local Bus

Before implementing a function requiring DMA capability on the ISA bus, it is recommended to check if it exists on PCI, or if it can be implemented differently, in order to use the local bus mode.

6.2.2 CLOCK CONFIGURATION

The CPU clock and the memory clock are independent unless the “synchronous mode” strap option is set (see the STRAP OPTIONS chapter). The potential clock configurations are then relatively limited as listed in Table 6-4.

Table 6-2. Main STPC modes

C	Mode	HCLK MHz	CPU clock clock ratio	MCLK MHz
1	Synchronous	100	200 (X2)	100
2	Asynchronous	100	200 (X2)	66
3	Synchronous	90	180 (X2)	90
4	Synchronous	75	188 (X2.5)	75

The advantage of synchronous mode compared to asynchronous mode is a lower latency when accessing SDRAM from the CPU or the PCI (saves 4 MCLK cycles for the first access of the burst). For the same CPU to Memory transfer performance, MCLK has to be roughly higher by 20MHz in ASYNC mode compared to SYNC mode to get the same system performance level (example: 66MHz SYNC = 86MHz ASYNC).
Prefer the use of SDRAM with CAS Latency equals to 3 (CL2) for the best performance.

The advantage of asynchronous mode is the capability to reprogram the MCLK speed on the fly. This could help for applications where power consumption must be optimized.

Table 6-3 below gives some examples. The right column correspond to the configuration number as described in Table 6-4:

Table 6-3. Clock mode selection

Constraints	C
Need CPU power Critical code fits into L1 cache	1
Need CPU power Code or data does not fit into L1 cache	3
Need high PCI bandwidth	1
Need flexible SDRAM speed	2

Obviously, the values for HCLK or MCLK can be reduced compared to Table 6-4 in case there is no need to push the device to its limits, or when avoiding specific frequency ranges (FM radio band for example).

6.3 ARCHITECTURE RECOMMENDATIONS

This section describes the recommended implementations for the STPC interfaces. For more details, download the **Reference Schematics** from the STPC web site.

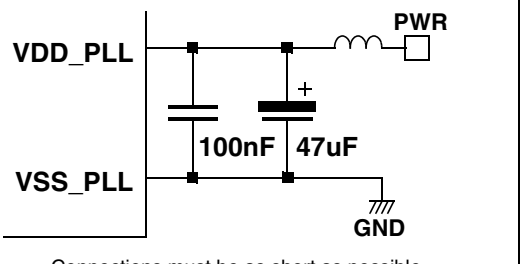
6.3.1 POWER DECOUPLING

An appropriate decoupling of the various STPC power pins is mandatory for optimum behaviour. When insufficient, the integrity of the signals is deteriorated, the stability of the system is reduced and EMC is increased.

6.3.1.1. PLL decoupling

This is the most important as the STPC clocks are generated from a single 14MHz stage using multiple PLLs which are highly sensitive analog cells. The frequencies to filter are the 25-50 KHz range which correspond to the internal loop bandwidth of the PLL and the 10 to 100 MHz frequency of the output. PLL power pins can be tied together to simplify the board layout.

Figure 6-3. PLL decoupling



6.3.1.2. Decoupling of 3.3V and Vcore

A power plane for each of these supplies with one decoupling capacitance for each power pin is the minimum. The use of multiple capacitances with values in decade is the best (for example: 10pF, 1nF, 100nF, 10uF), the smaller the value, the closer to the power pin. Connecting the various digital power planes through capacitances will reduce furthermore the overall impedance and electrical noise.

6.3.2 14MHZ OSCILLATOR STAGE

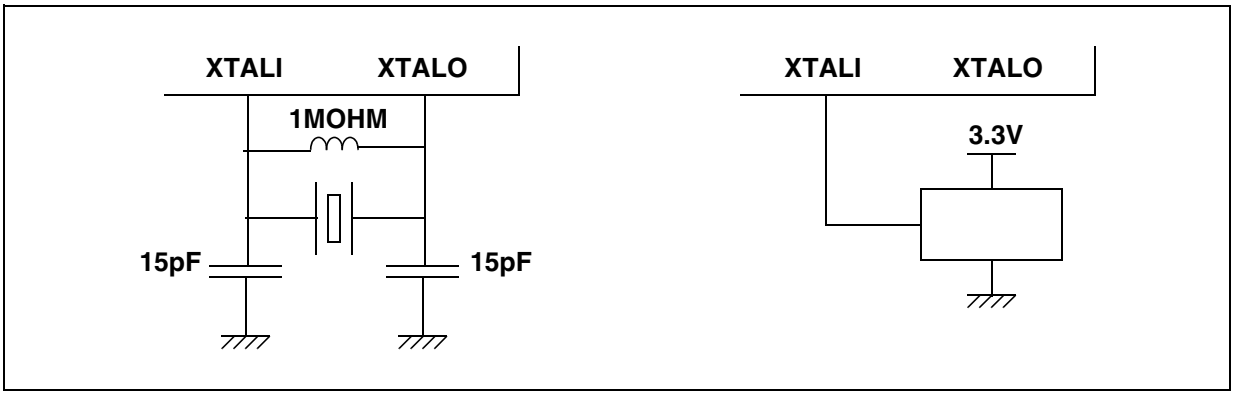
The 14.31818 MHz oscillator stage can be implemented using a quartz crystal, which is the preferred and cheaper solution, or using an external 3.3V oscillator.

The crystal must be used in its series-cut fundamental mode and not in overtone mode. It must have an Equivalent Series Resistance (ESR, sometimes referred to as Rm) of less than 50 Ohms (typically 8 Ohms) and a shunt capacitance (Co) of less than 7 pF. The balance capacitors of 16 pF must be added, one connected to each pin, as shown in Figure 6-4.

In the event of an external oscillator providing the master clock signal to the STPC device, the LVTTL signal should be connected to XTALI, as shown in Figure 6-4.

As this clock is the reference for all the other on-chip generated clocks, it is **strongly recommended to shield this stage**, including the 2 wires going to the STPC balls, in order to reduce the jitter to the minimum and reach the optimum system stability.

Figure 6-4. 14.31818 MHz stage



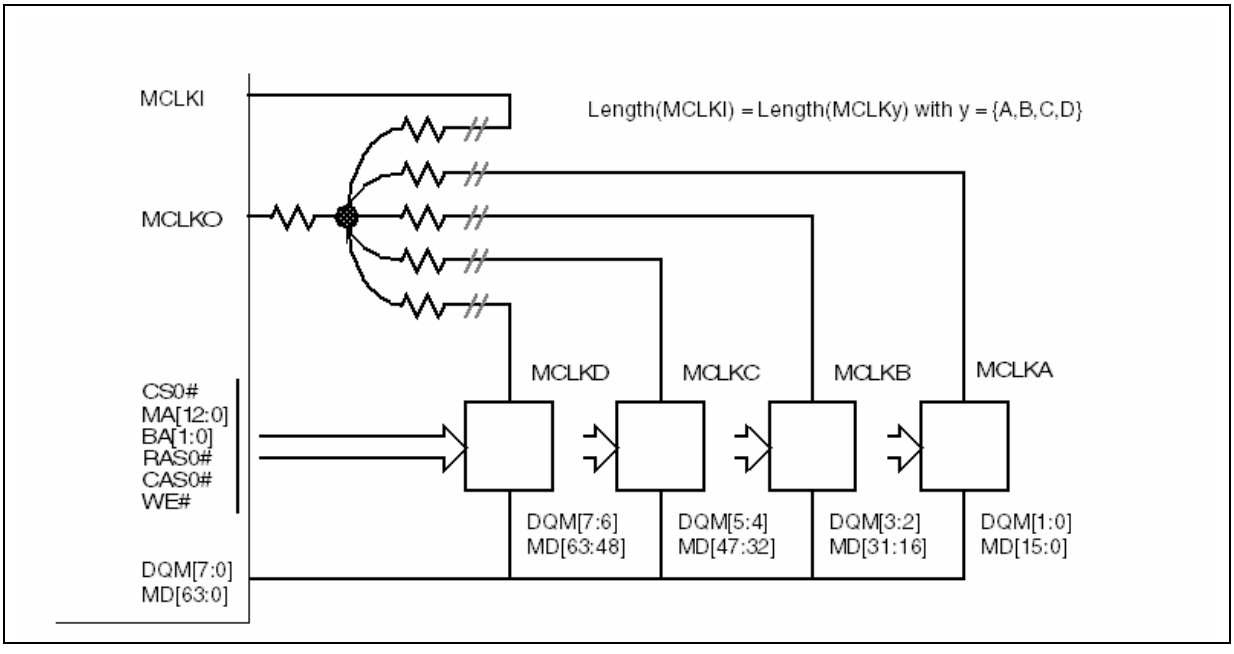
6.3.3 SDRAM

The STPC provides all the signals for SDRAM control. Up to 256 MByte of main memory is supported. All Banks must be 64-bit wide. Up to four memory banks are available when using 16 Mbit devices. Up to two banks only can be connected when using 64 Mbit, 128 Mbit and 256 Mbit components, due to the reallocation of the CS2# and CS3# signals. This is described in Table 6-4 and Table 6-5.

Host memory extends to the top of populated SDRAM. Bank 0 must always be populated.

Figure 6-5, Figure 6-6 and Figure 6-7 show some typical implementations.

Figure 6-5. One Memory Bank with Four Chips (16-bit)



The purpose of the serial resistors is to reduce signal oscillation and EMI by filtering line reflections. The capacitance in has a filtering effect too, while it is used for propagation delay compensation in the two other figures.

Figure 6-6. One Memory Bank with Eight Chips (8-bit)

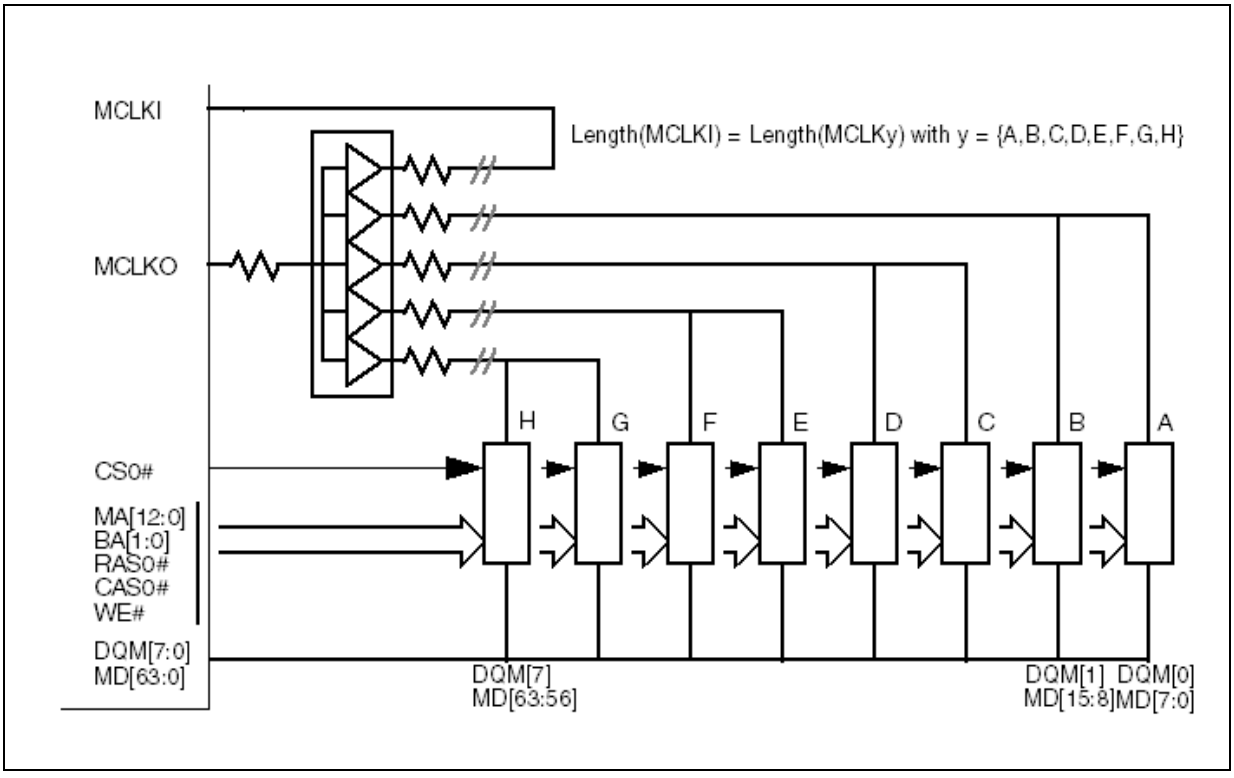
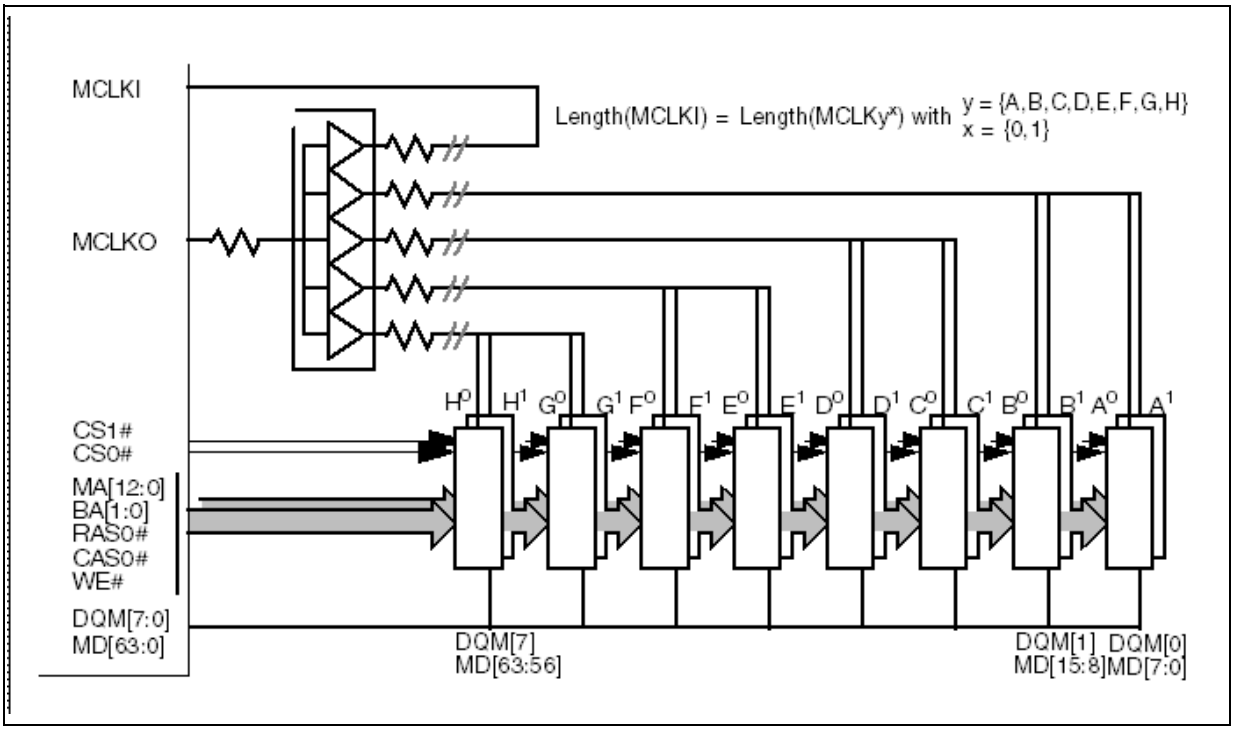


Figure 6-7. Two Memory Banks with Eight Chips (8-bit)



For other implementations like 32-bit SDRAM devices, refers to the SDRAM controller signal multiplexing and address mapping described in the following Table 6-4 and Table 6-5.

Table 6-4. DIMM Pinout

SDRAM Density	16 Mbit	64/128 Mbit	64/128 Mbit	256 Mbit	STPC I/F
Internal Banks	2 Banks	2 Banks	4 Banks	4 Banks	
DIMM Pin Number					
...	MA[10:0]	MA[10:0]	MA[10:0]	MA[10:0]	MA[10:0]
123	-	MA11	MA11	MA11	CS2# (MA11)
126	-	MA12	-	MA12	CS3# (MA12)
39	-	-	BA1 (MA12)	BA1	CS#3 (BA1)
122	BA0(MA11)	BA0 (MA13)	BA0 (MA13)	BA0	BA0

Table 6-5. Address Mapping

Address Mapping: 16 Mbit - Two internal banks															
STPC I/F	BA0				MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
RAS Address	A11				A22	A21	A2	A19	A18	A17	A16	A15	A14	A13	A12
CAS Address	A11				0	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3
Address Mapping: 64/128 Mbit - Two internal banks															
STPC I/F	BA0		MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
RAS Address	A11		A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
CAS Address	A11		0	0	0	A26	A25	A10	A9	A8	A7	A6	A5	A4	A3
Address Mapping: 64/128 Mbit - Four internal banks															
STPC I/F	BA0	BA1		MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
RAS Address	A11	A12		A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13
CAS Address	A11	A12		A27	0	A26	A25	A10	A9	A8	A7	A6	A5	A4	A3
Address Mapping: 256 Mbit - Four internal banks															
STPC I/F	BA0	BA1	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
RAS Address	A11	A12	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13
CAS Address	A11	A12	0	0	0	A27	A26	A10	A9	A8	A7	A6	A5	A4	A3

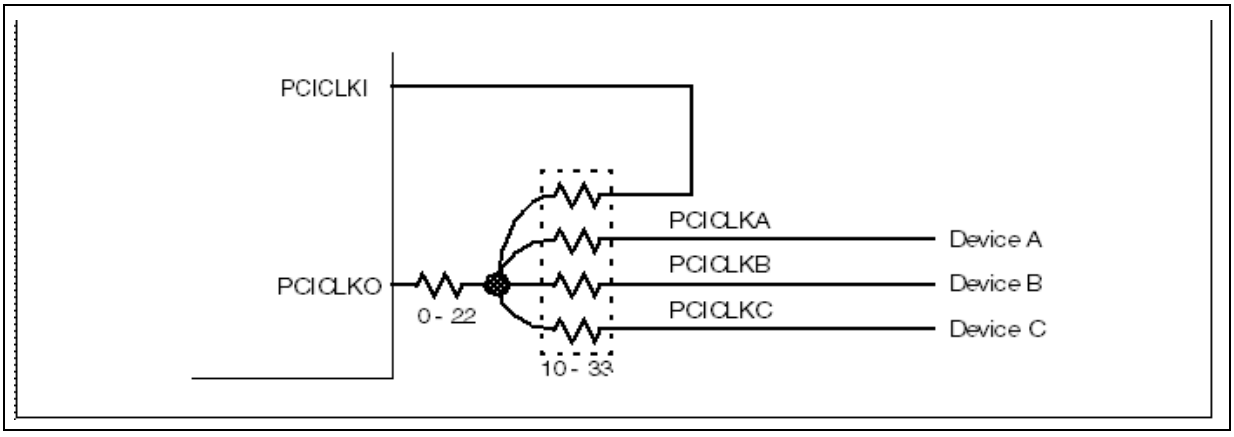
6.3.4 PCI BUS

The PCI bus is always active and the following control signals must be pulled-up to 3.3V or 5V through 8K2 resistors even if this bus is not connected to an external device: FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, LOCK#, SERR#, PCI_REQ#[2:0].

PCI_CLKO must be connected to PCI_CLKI through a 10 to 33 Ohm resistor. Figure 6-8 shows a typical implementation.

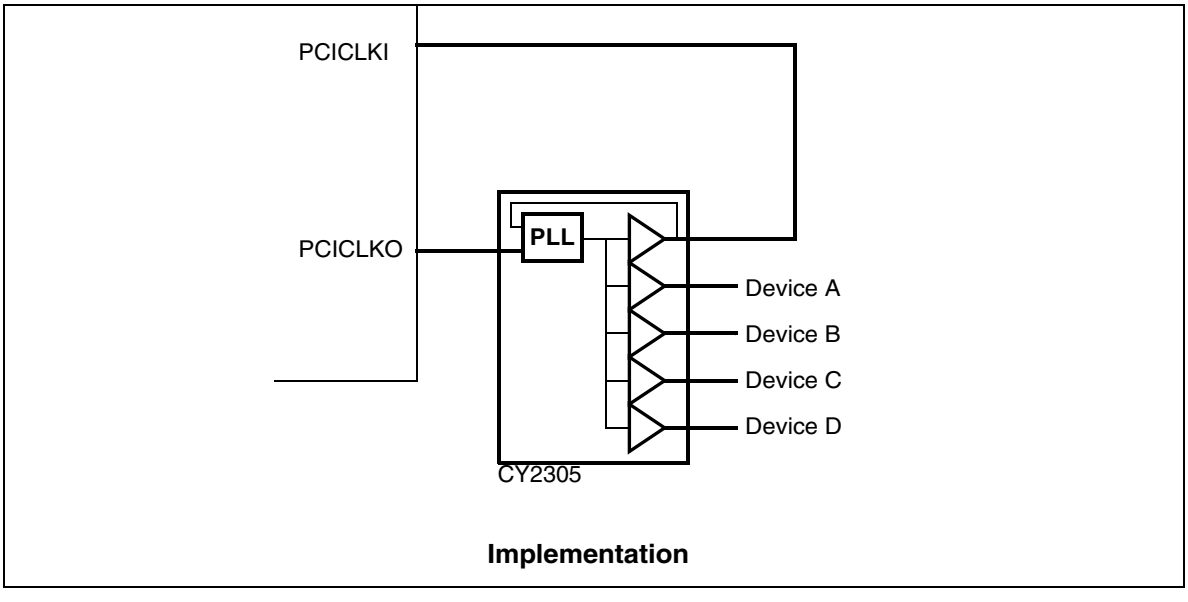
For more information on layout constraints, go to the **place and route recommendations** section

Figure 6-8. Typical PCI clock routing



In the case of higher clock load it is recommended to use a zero-delay clock buffer as described in Figure 6-9. This approach is also recommended when implementing the delay on PCICLKI according to the PCI section of the **Electrical Specifications** chapter.

Figure 6-9. PCI clock routing with zero-delay clock buffer

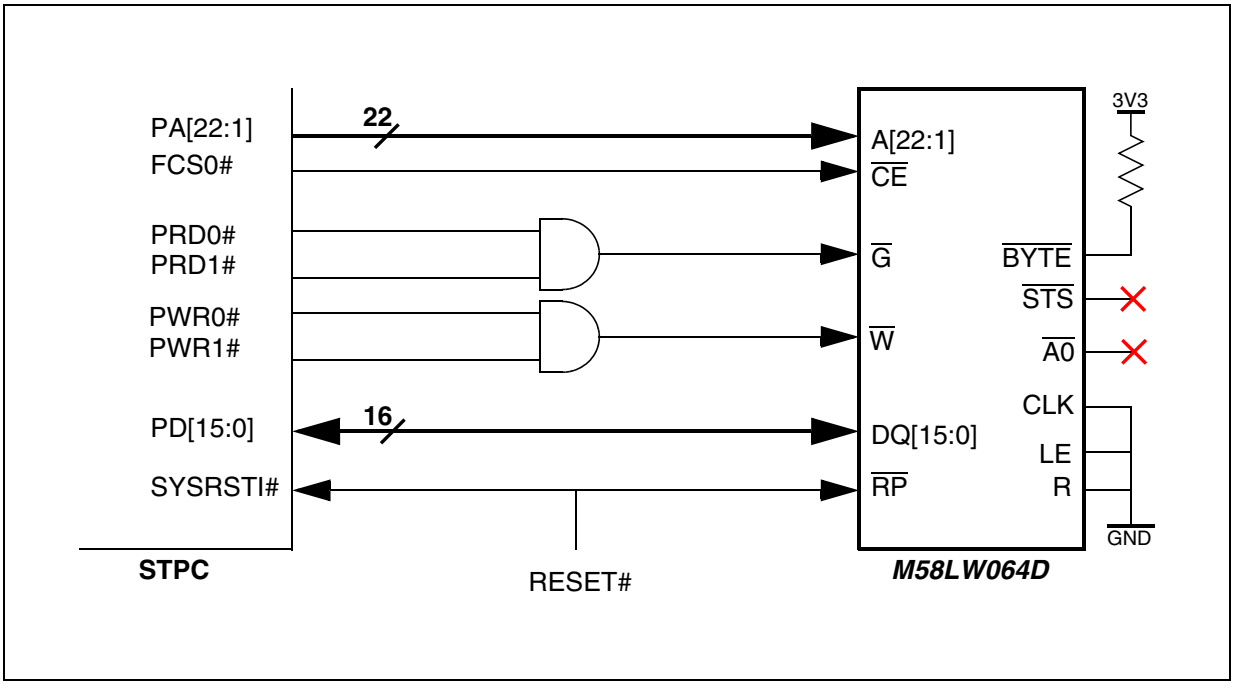


6.3.5 LOCAL BUS

The local bus has all the signals to connect flash devices or I/O devices with the minimum glue logic.

Figure 6-10 describes how to connect a 16-bit boot flash (the corresponding strap options must be set accordingly).

Figure 6-10. Typical 16-bit boot flash implementation

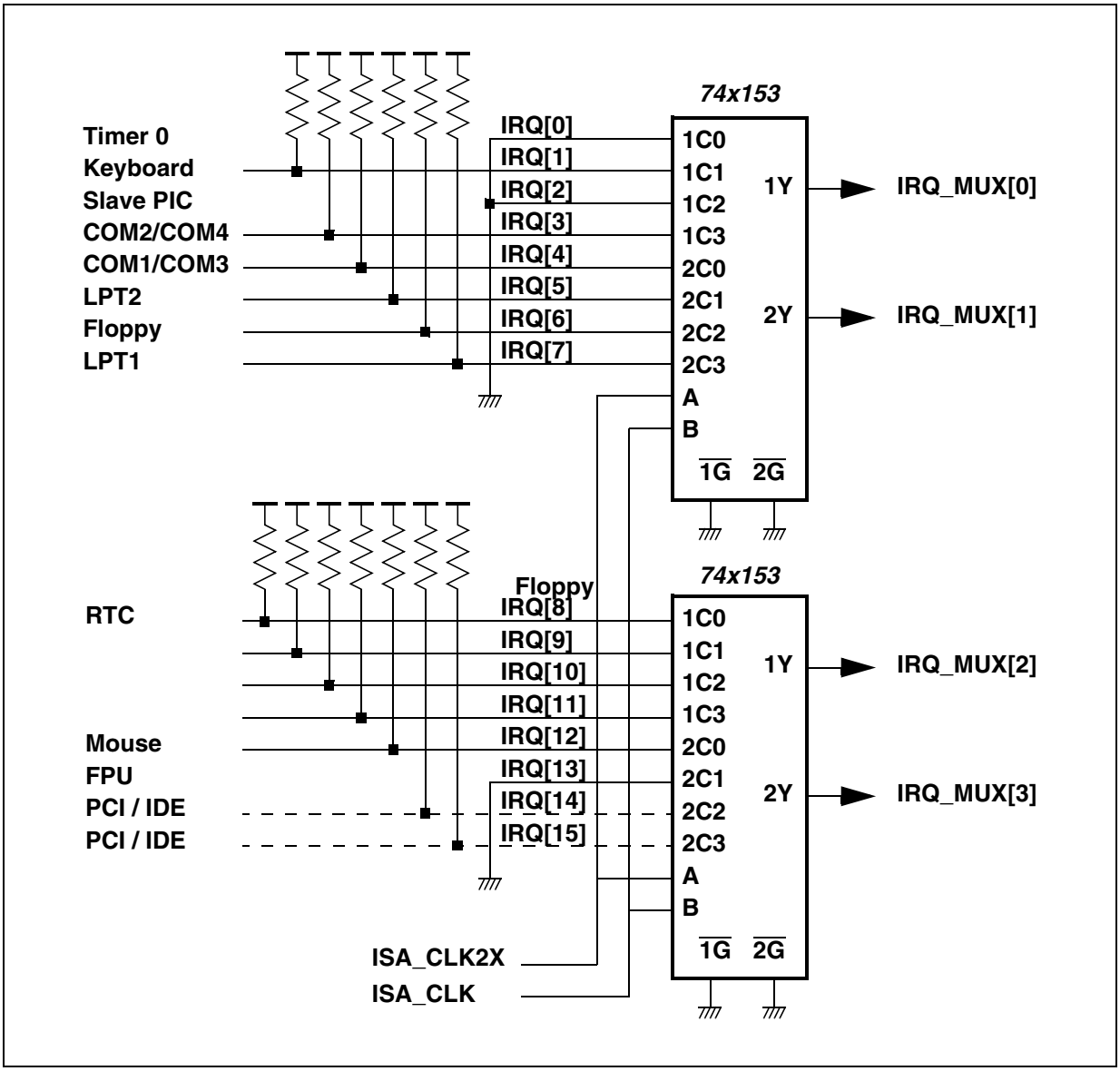


6.3.6 IPC

Most of the IPC signals are multiplexed: Interrupt inputs, DMA Request inputs, DMA Acknowledge outputs. The figure below describes a complete implementation of the IRQ[15:0] time-multiplexing.

When an interrupt line is used internally, the corresponding input can be grounded. In most of the embedded designs, only few interrupts lines are necessary and the glue logic can be simplified.

Figure 6-11. Typical IRQ multiplexing

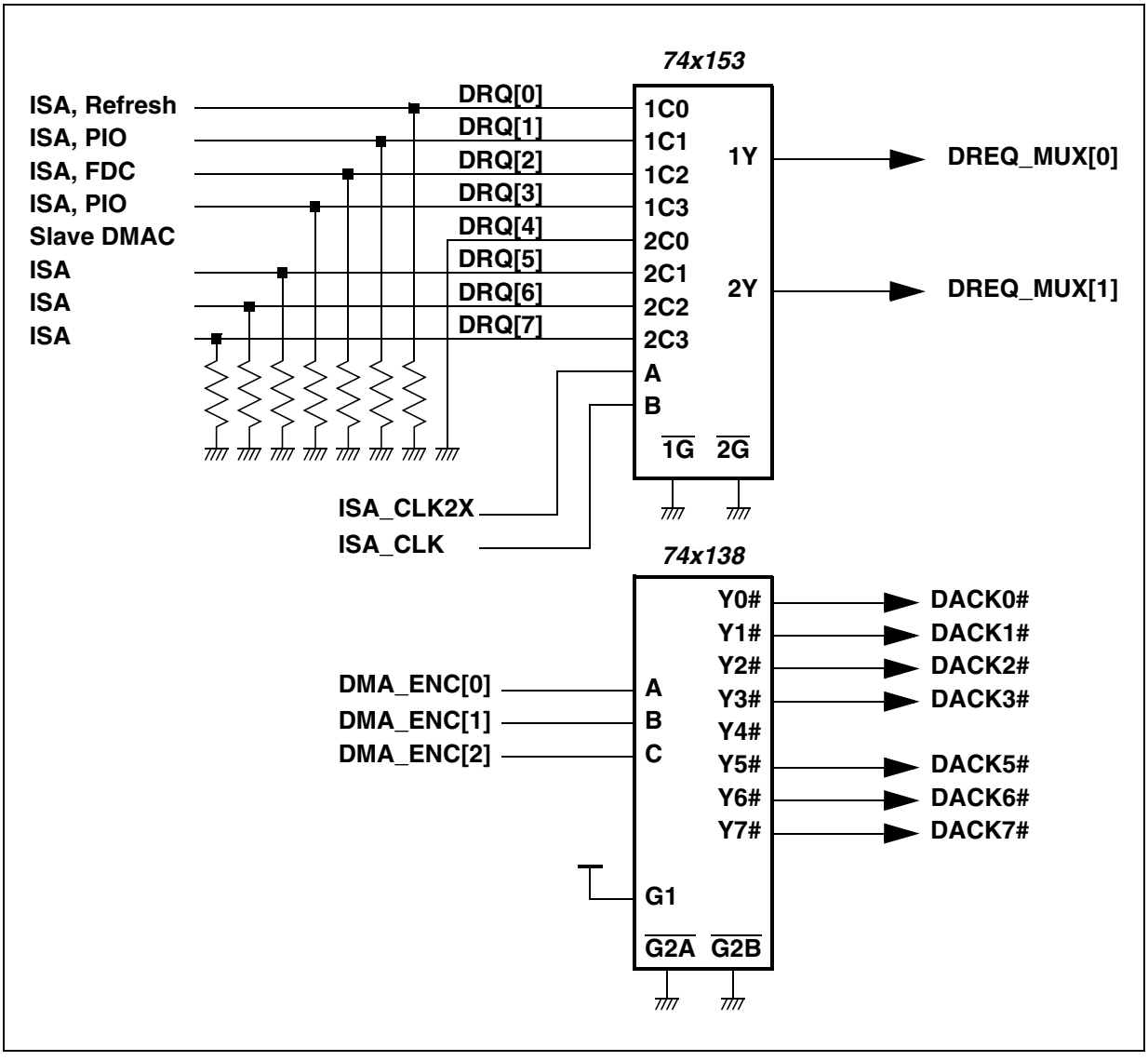


When the interface is integrated into the STPC, the corresponding interrupt line can be grounded as it is connected internally.

For example, if the integrated IDE controller is activated, the IRQ[14] and IRQ[15] inputs can be grounded.

The figure below describes a complete implementation of the external glue logic for DMA Request time-multiplexing and DMA Acknowledge demultiplexing. Like for the interrupt lines, this logic can be simplified when only few DMA channels are used in the application.
This glue logic is not needed in Local bus mode as it does not support DMA transfers.

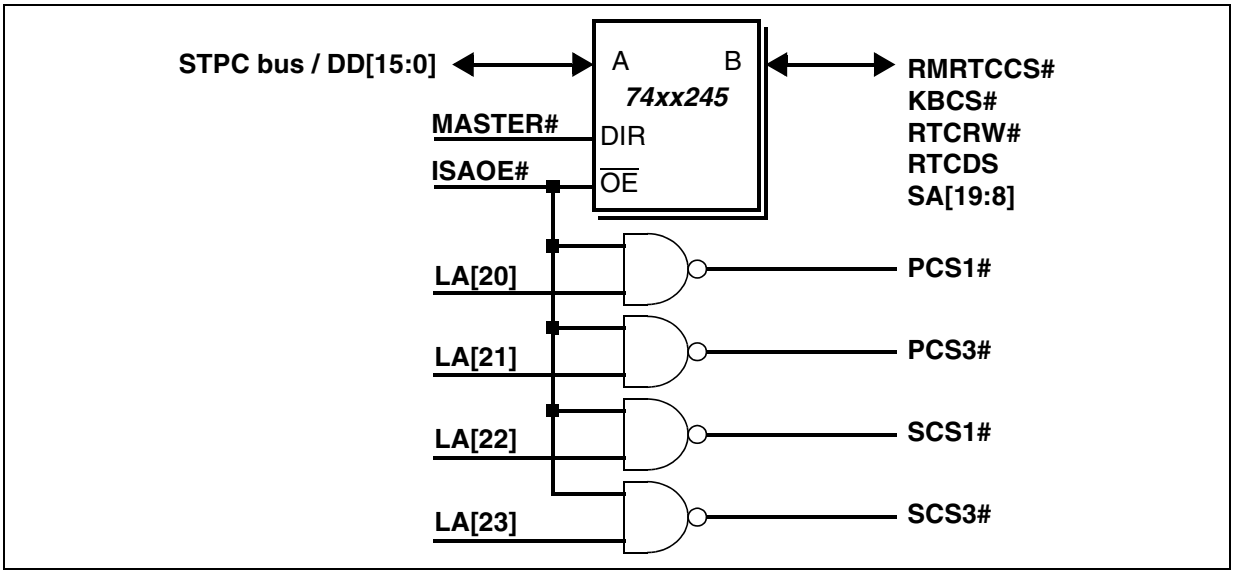
Figure 6-12. Typical DMA multiplexing and demultiplexing



6.3.7 IDE / ISA DYNAMIC DEMULTIPLEXING

Some of the ISA bus signals are dynamically multiplexed to optimize the pin count. Figure 6-13 describes how to implement the external glue logic to demultiplex the IDE and ISA interfaces. In Local Bus mode the 74xx245 and NAND gates can be removed.

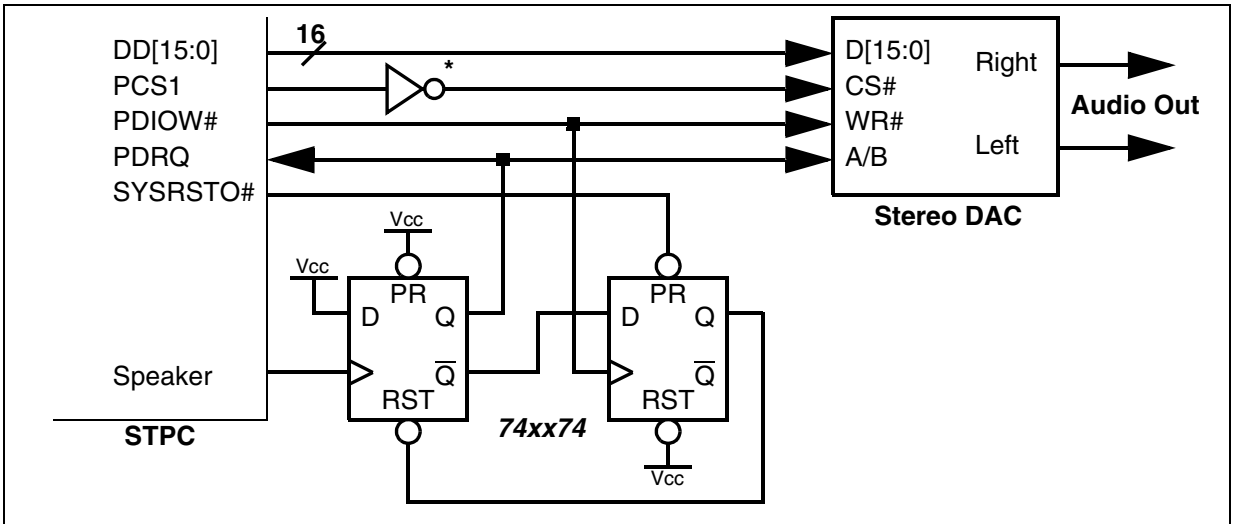
Figure 6-13. Typical IDE / ISA Demultiplexing



6.3.8 BASIC AUDIO USING IDE INTERFACE

When the application requires only basic audio capabilities, an audio DAC on the IDE interface can avoid using a PCI-based audio device (see Figure 6-14). This low cost solution is not CPU consuming thanks to the DMA controller implemented in the IDE controller and can generate 16-bit stereo sound. The clock speed is programmable when using the speaker output.

Figure 6-14. Basic audio on IDE

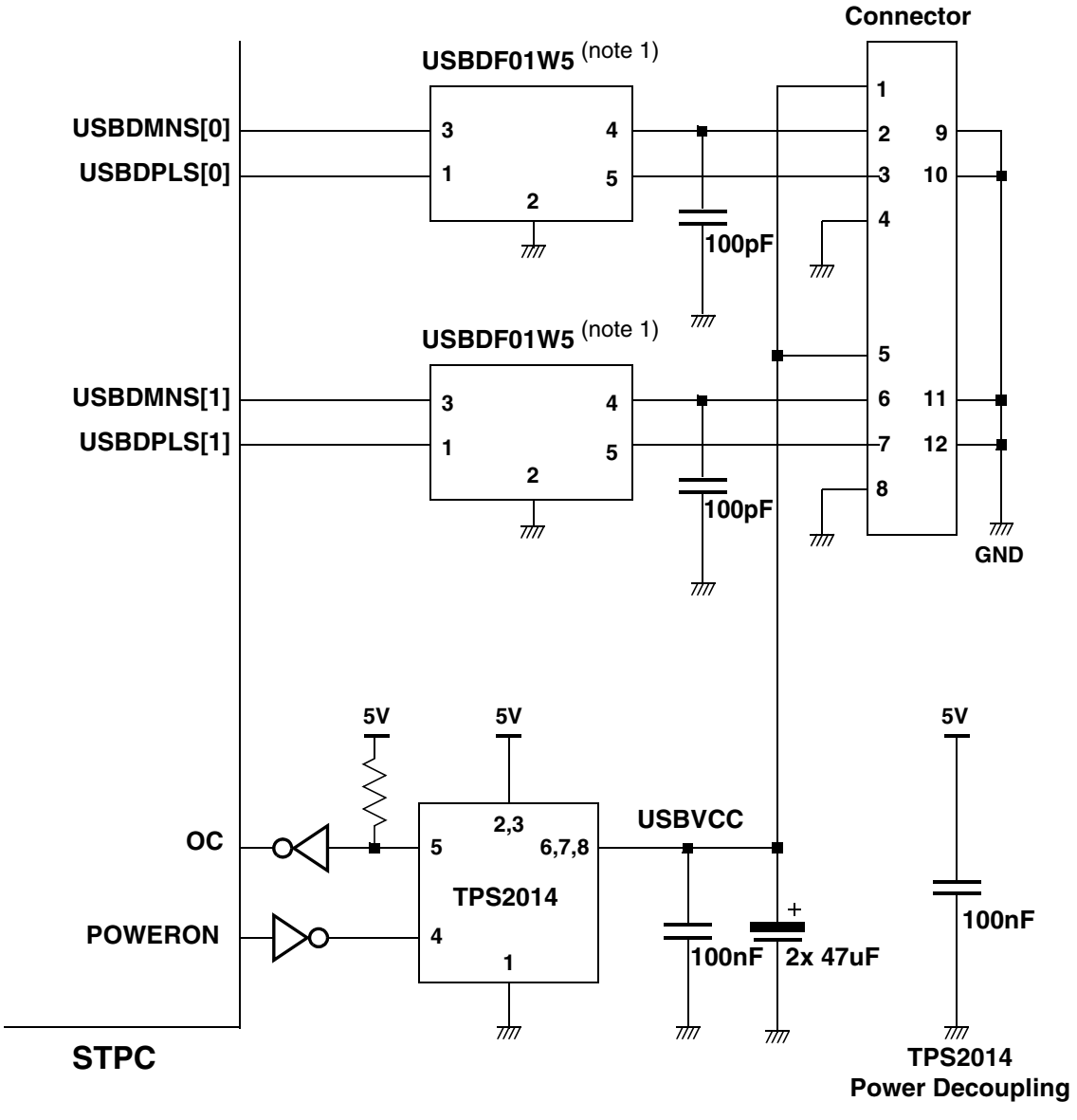


Note * : the inverter can be removed when the DAC CS# is directly connected to GND

6.3.9 USB INTERFACE

The STPC integrates a USB host interface with a 2-port Hub. The only external device needed are the ESD protection circuits USBDF01W5 and an USB power supply controller. Figure 6-15 describes a typical implementation using these devices.

Figure 6-15. Typical USB implementation

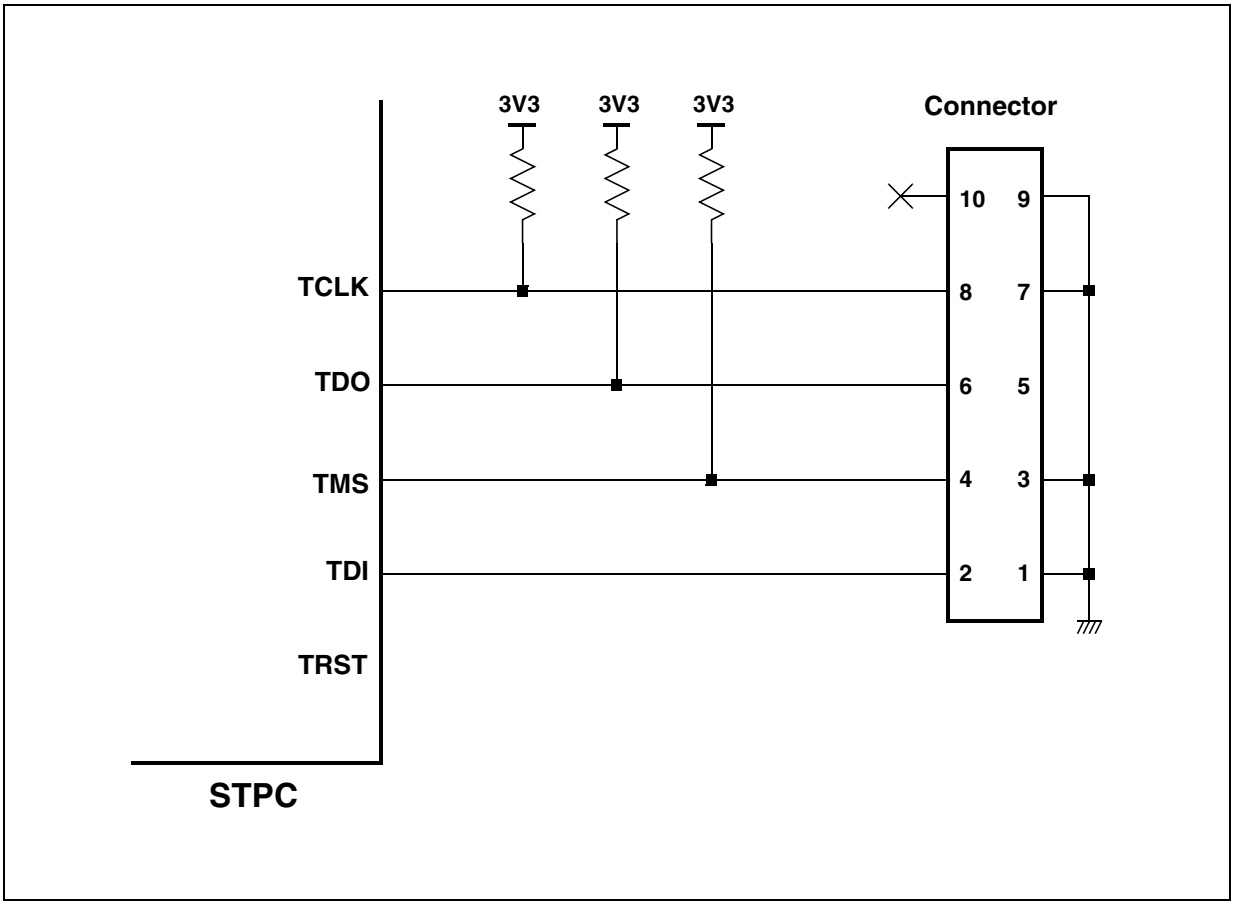


Note 1: The ESD protection will be adequate for most applications. In some instances, problems may occur if the devices on the USB chain do not have enough power to drive the signals adequately. We therefore recommend that you replace the part with discrete components and reduce the value of the capacitor.

6.3.10 JTAG INTERFACE

The STPC integrates a JTAG interface for scan-chain and on-board testing. The only external devices needed are the pull up resistors. Figure 6-16 describes a typical implementation using these devices.

Figure 6-16. Typical JTAG implementation



6.4 PLACE AND ROUTE RECOMMENDATIONS

6.4.1 GENERAL RECOMMENDATIONS

Some STPC Interfaces run at high speed and need to be carefully routed or even shielded like:

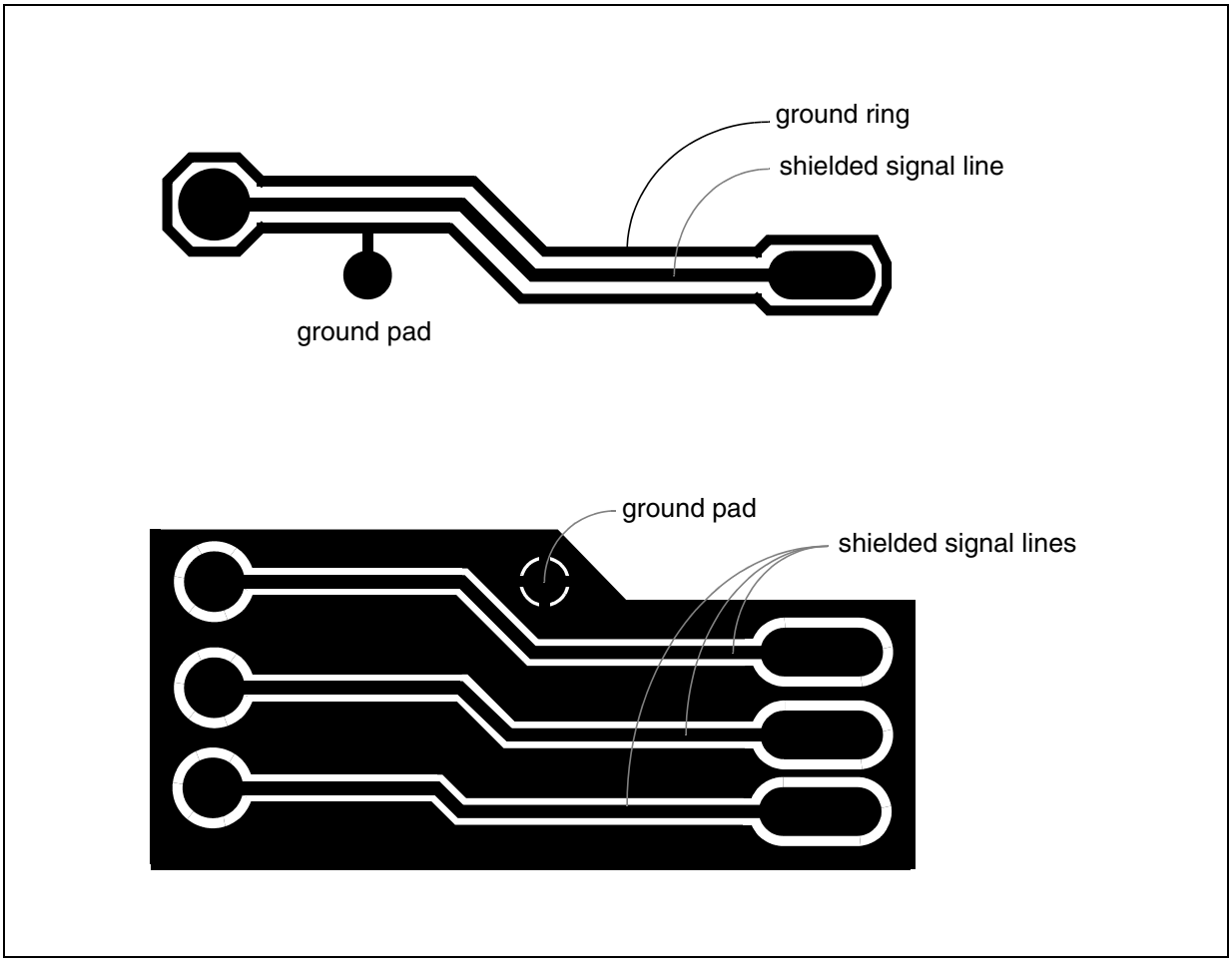
1) Memory Interface
2) PCI bus
3) 14 MHz oscillator stage

All clock signals have to be routed first and shielded for speeds of 27MHz or higher. The high speed signals follow the same constraints, as for the memory and PCI control signals.

The next interfaces to be routed are Memory and PCI.

All the analog noise-sensitive signals have to be routed in a separate area and hence can be routed independently.

Figure 6-17. Shielding signals



6.4.2 PLL DEFINITION AND IMPLEMENTATION

PLLs are analog cells which supply the internal STPC Clocks. To get the cleanest clock, the jitter on the power supply must be reduced as much as possible. This will result in a more stable system.

Each of the integrated PLLs has a dedicated power pin so a single power plane for all of these PLLs, or one wire for each, or any solution in between which help the layout of the board can be used.

Powering these pins with one Ferrite + capacitances is enough. We recommend at least 2 capacitances: one 'big' (few uF) for power storage, and one or 2 smalls (100nF + 1nF) for noise filtering.

6.4.3 MEMORY INTERFACE

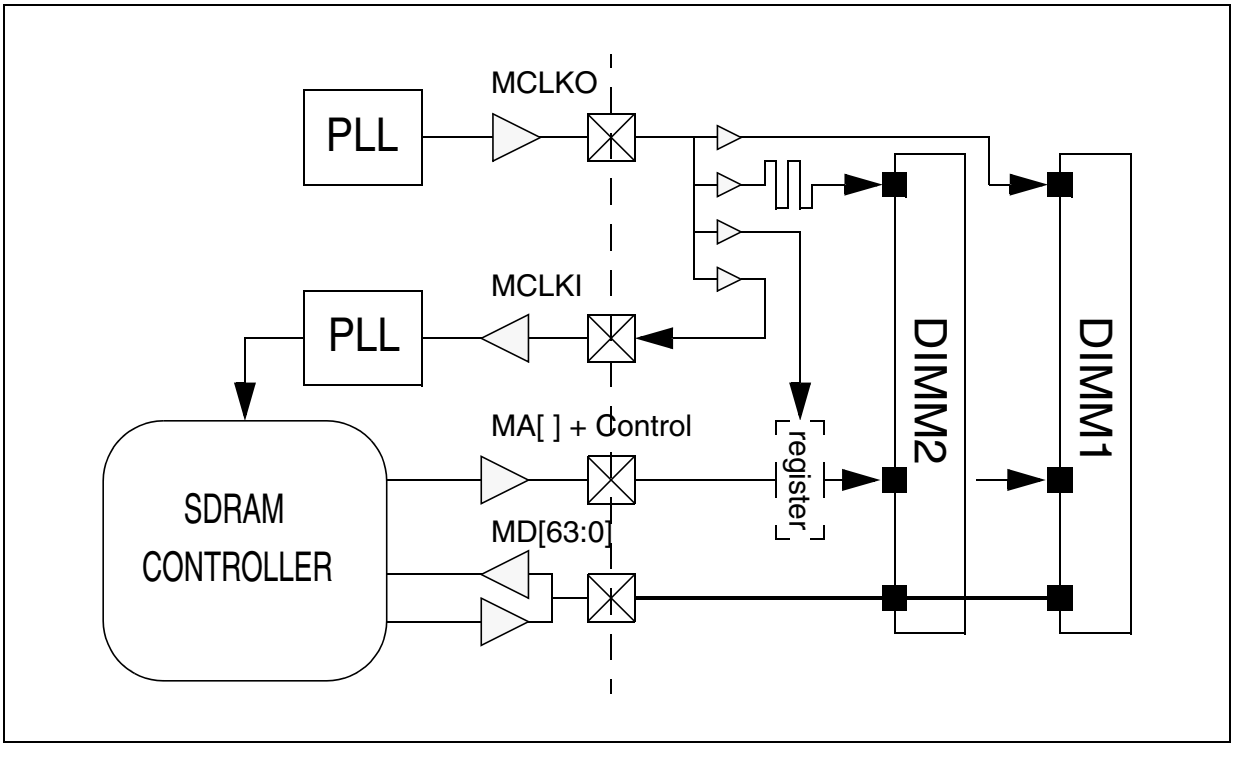
6.4.3.1. Introduction

In order to implement SDRAM memory interfaces which work at clock frequencies of 100 MHz and above, careful consideration has to be given to the timing of the interface with all the various electrical and physical constraints taken into consideration. The guidelines described below are related to SDRAM components on DIMM modules. For applications where the memories are directly soldered to the motherboard, the PCB should be laid out such that the trace lengths fit within the constraints shown here. The traces could be slightly shorter since the extra routing on the DIMM PCB is no longer present but it is then up to the user to verify the timings.

6.4.3.2. SDRAM Clocking Scheme

The SDRAM Clocking Scheme deserves a special mention here. Basically the memory clock is generated on-chip through a PLL and goes directly to the MCLKO output pin of the STPC. The nominal frequency is 100 MHz. Because of the high load presented to the MCLK on the board by the DIMMs it is recommended to rebuffer the MCLKO signal on the board and balance the skew to the clock ports of the different DIMMs and the MCLKI input pin of STPC.

Figure 6-18. Clock Scheme



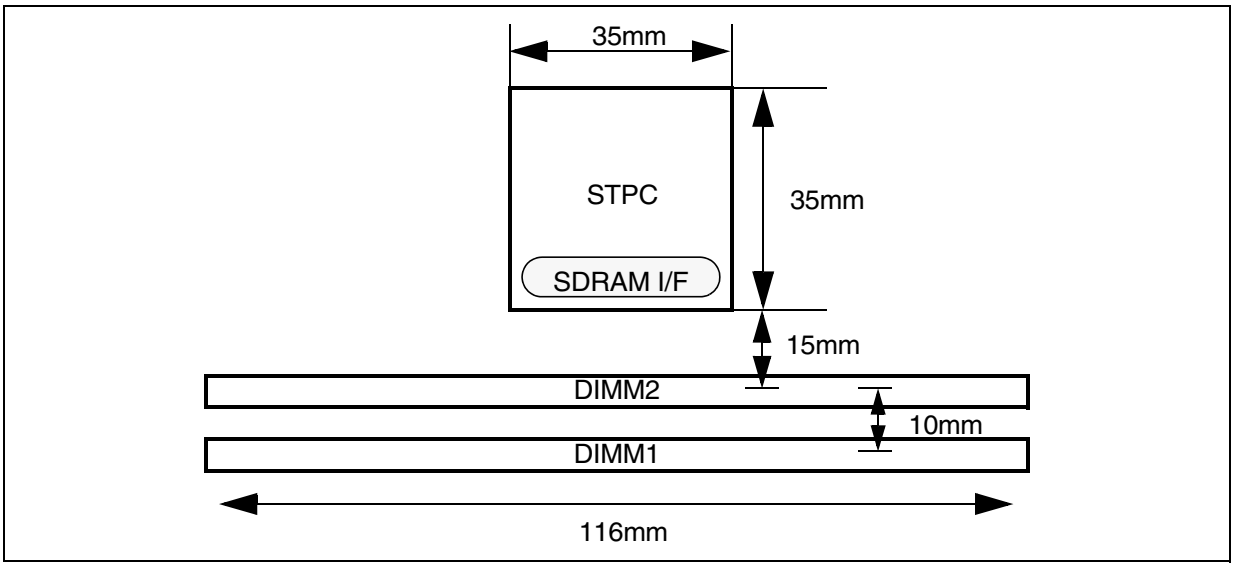
6.4.3.3. Board Layout Issues

The physical layout of the motherboard PCB assumed in this presentation is as shown in Figure 6-19. Because all of the memory interface signal balls are located in the same region of the STPC device, it is possible to orientate the device to reduce the trace lengths. The worst case routing length to the DIMM1 is estimated to be 100 mm.

Figure 6-19. DIMM placement

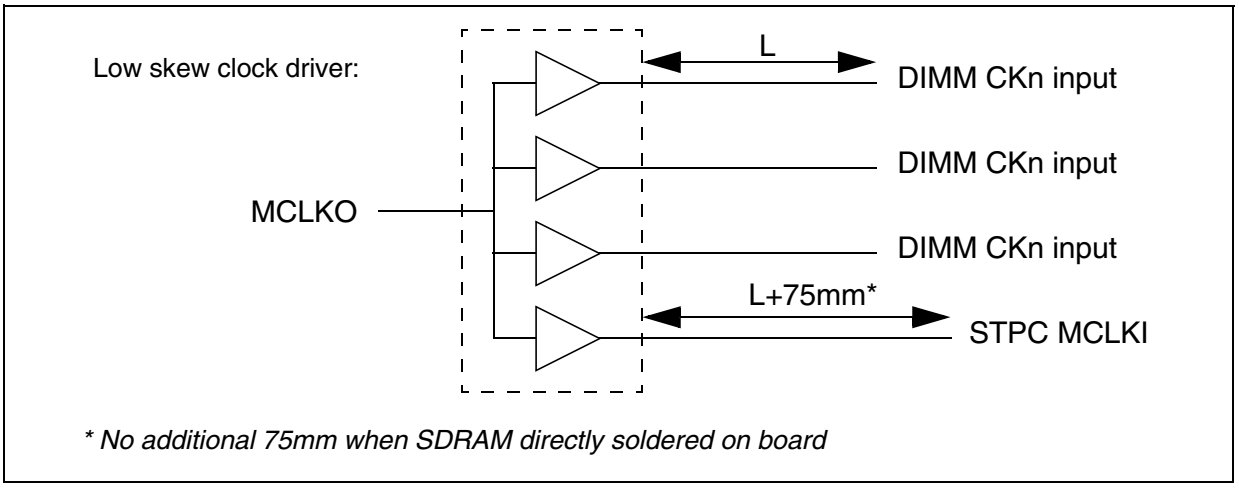
Solid power and ground planes are a must in order to provide good return paths for the signals and to reduce EMI and noise. Also there should be ample high frequency decoupling between the power and ground planes to provide a low impedance path between the planes for the return paths for signal routings which change layers. If possible, the traces should be routed adjacent to the same power or ground plane for the length of the trace.

For the SDRAM interface, the most critical signal is the clock. Any skew between the clocks at the



SDRAM components and the memory controller will impact the timing budget. In order to get well matched clocks at all components it is recommended that all the DIMM clock pins, STPC memory clock input (MCLKI) and any other component using the memory clock are individually driven from a low skew clock driver with matched routing lengths. In other words, all clock line lengths that go from the buffer to the memory chips (MCLKx) and from the buffer to the STPC (MCLKI) must be identical.
This is shown in Figure 6-20.

Figure 6-20. Clock Routing



** No additional 75mm when SDRAM directly soldered on board*

The important factors for the clock buffer are a consistent drive strength and low skew between the outputs. The delay through the buffer is not important so it does not have to be a zero delay PLL type buffer. The trace lengths from the clock driver to the DIMM CKn pins should be matched exactly. Since the propagation speed can vary between PCB layers, the clocks should be routed in a consistent way. The routing to the STPC memory input should be longer by 75 mm to compensate for the extra clock routing on the DIMM. Also a 20 pF capacitor should be placed as near as possible to the clock input of the STPC to compensate for the DIMM's higher clock load. The impedance of the trace used for the clock routing should be matched to the DIMM clock trace impedance (60-75 ohms)**.**To minimise crosstalk the clocks should be routed with spacing to adjacent tracks of at least twice the clock trace width. For designs which use SDRAMs directly mounted on the motherboard PCB all the clock trace lengths should be matched exactly.

The DIMM sockets should be populated starting with the furthest DIMM from the STPC device first (DIMM1). There are two types of DIMM devices; single-row and dual-row. The dual-row devices require two chip select signals to select between the two rows. A STPC device with 4 chip select control lines could control either 4 single-row DIMMs or 2 dual-row DIMMs. When only 2 chip select control lines are activated, only two single-row DIMMs or one dual-row DIMM can be controlled.

When using DIMM modules, schematics have to be done carefully in order to avoid data buses completely crossing on the board. This has to be checked at the library level. In order to achieve the layout shown in Figure 6-21, schematics have to implement the crossing described in Figure 6-22. The DQM signals must be exchanged using the same order.

Figure 6-21. Optimum Data Bus Layout for DIMM

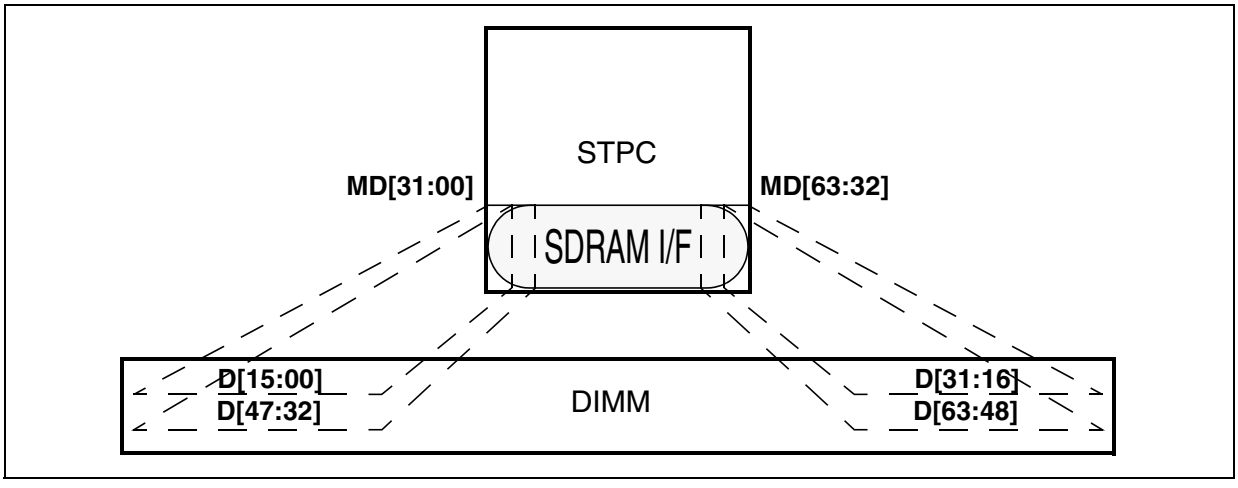
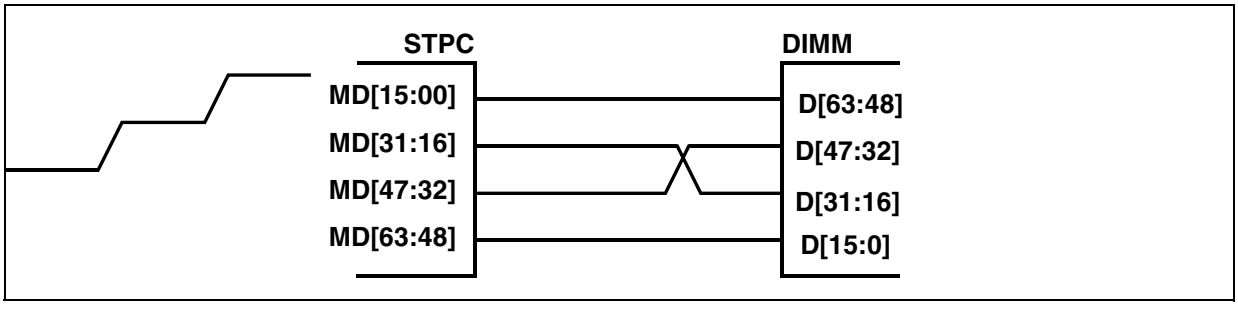


Figure 6-22. Schematics for Optimum Data Bus Layout for DIMM



6.4.3.4. Summary

For unbuffered DIMMs the address/control signals will be the most critical for timing. The simulations show that for these signals the best way to drive them is to use a parallel termination. For applications where speed is not so critical series termination can be used as this will save power. Using a low impedance such as 50Ω for these critical traces is recommended as it both reduces the delay and the overshoot.

The other memory interface signals will typically be not as critical as the address/control signals. Using lower impedance traces is also beneficial for the other signals but if their timing is not as critical as the address/control signals they could use the default value. Using a lower impedance implies using wider traces which may have an impact on the routing of the board.

The layout of this interface can be validated by an electrical simulation using the IBIS model available on the STPC web site.

6.4.4 PCI INTERFACE

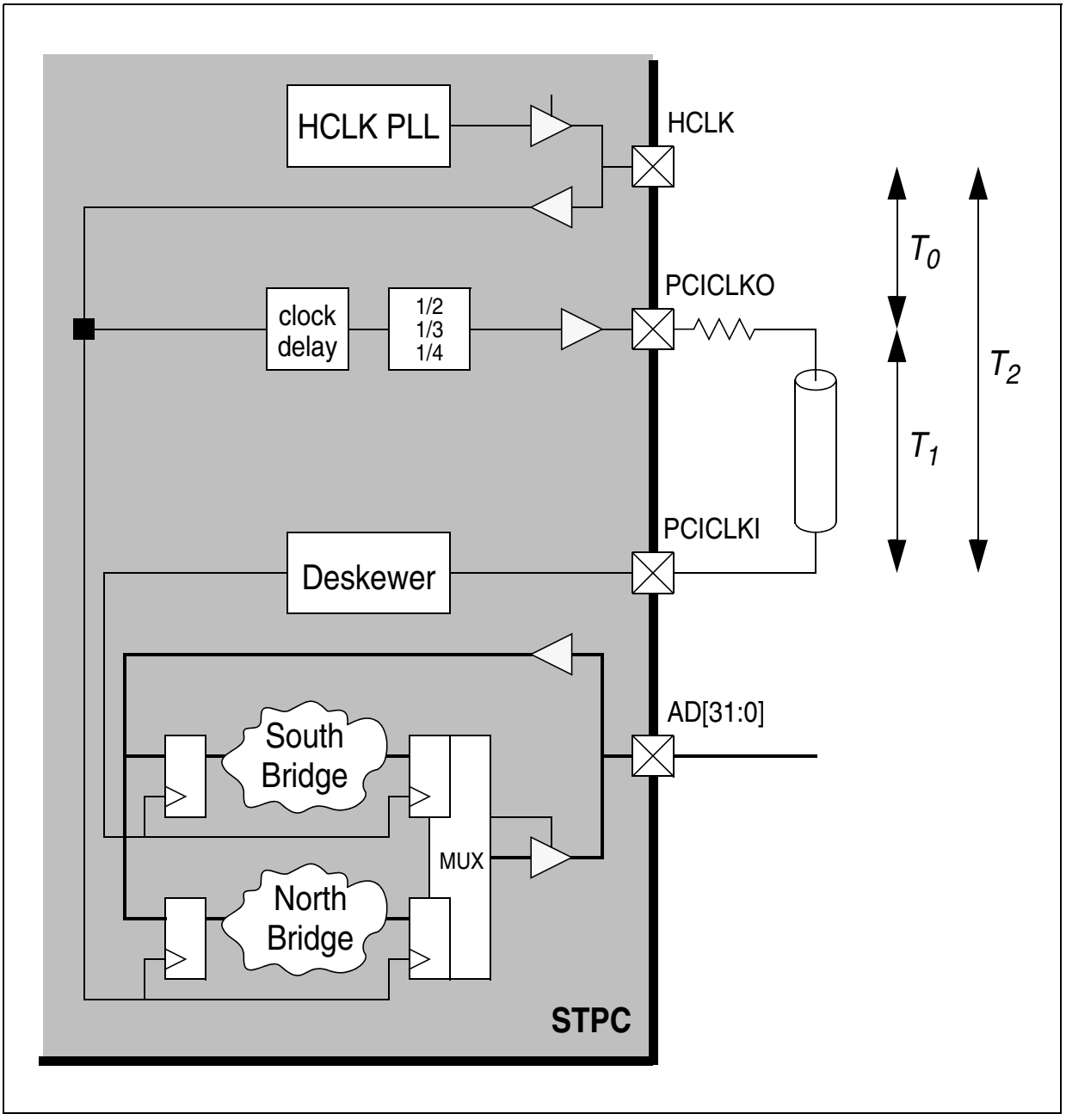
6.4.4.1. Introduction

In order to achieve a PCI interface which works at clock frequencies up to 33MHz, careful consideration has to be given to the timing of the interface with all the various electrical and physical constraints taken into consideration.

6.4.4.2. PCI Clocking Scheme

The PCI Clocking Scheme deserves a special mention here. Basically the PCI clock (PCICLKO) is generated on-chip from HCLK through a programmable delay line and a clock divider. The nominal frequency is 33MHz. This clock must be looped to PCICLKI and goes to the internal South Bridge through a deskewer. On the contrary, the internal North Bridge is clocked by HCLK, putting some additionnal constraints on T_0 and T_1.

Figure 6-23. Clock Scheme

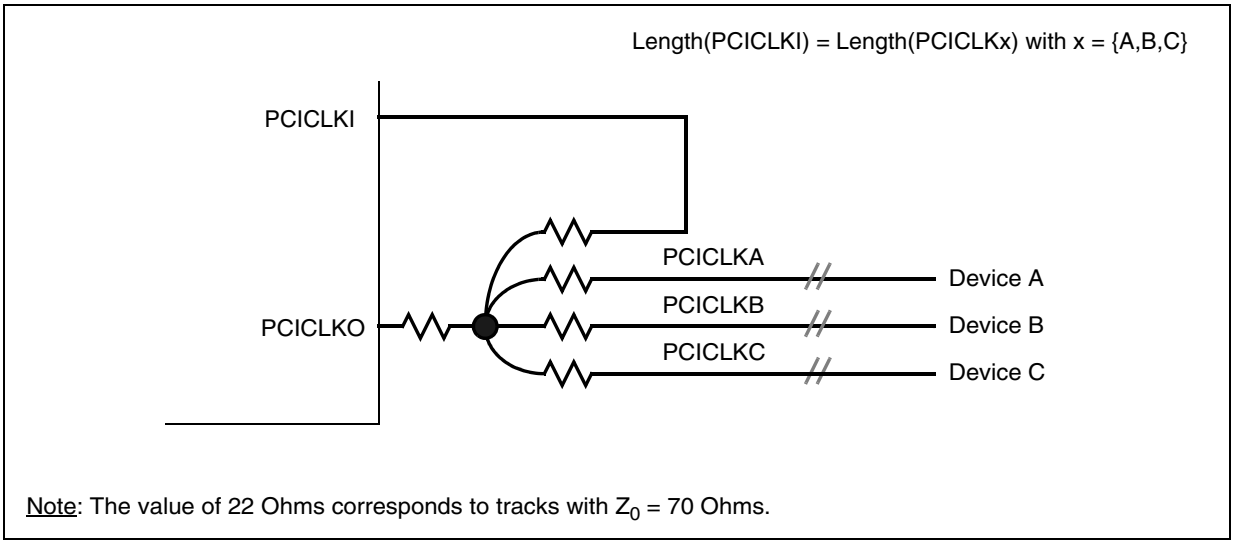


6.4.4.3. Board Layout Issues

The physical layout of the motherboard PCB assumed in this presentation is as shown in Figure 6-24. For the PCI interface, the most critical signal is the clock. Any skew between the clocks at the PCI components and the STPC will impact the timing budget. In order to get well matched clocks at all components it is recommended that all the PCI clocks are individually driven from a serial resistance with matched routing lengths. In other words, all clock line lengths that go from the resistor to the PCI chips (PCICLKx) must be identical.

The figure below is for PCI devices soldered on-board. In the case of a PCI slot, the wire length must be shortened by 2.5" to compensate the clock layout on the PCI board. The maximum clock skew between all devices is 2ns according to PCI specifications.

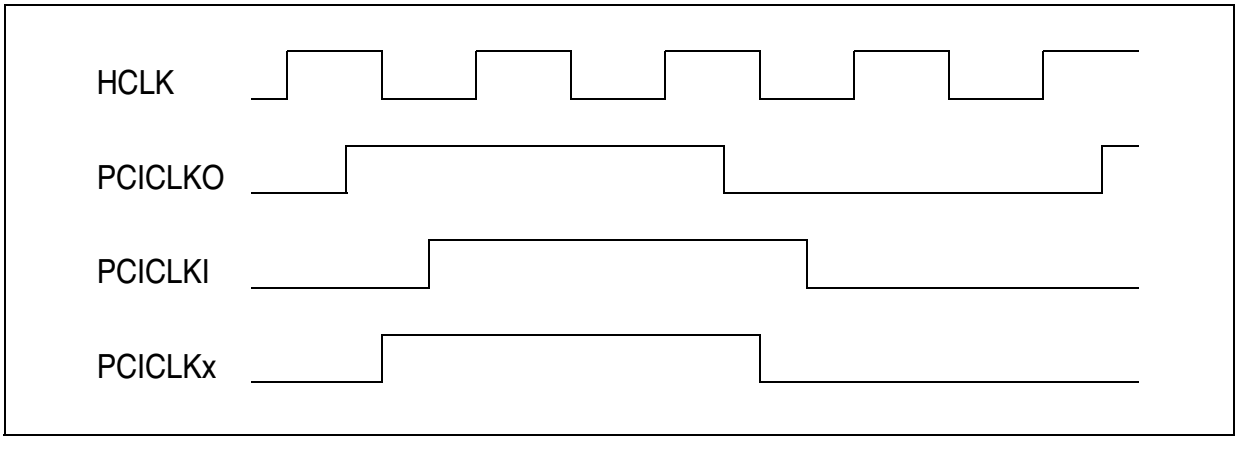
Figure 6-24. Typical PCI clock routing



Note: The value of 22 Ohms corresponds to tracks with Z_0 = 70 Ohms.

The Figure 6-25 describes a typical clock delay implementation. The exact timing constraints are listed in the PCI section of the **Electrical Specifications** Chapter.

Figure 6-25. Clocks relationships



6.5 THERMAL DISSIPATION

6.5.0.1. Power Saving

Thermal dissipation of the STPC depends mainly on supply voltage. When the system does not need to work at the upper voltage limit, it may therefore be beneficial to reduce the voltage to the lower voltage limit, where possible. This could save a few 100's of mW.

The second area to look at is unused interfaces and functions. Depending on the application, some input signals can be grounded, and some blocks not powered or shutdown. Clock speed dynamic adjustment is also a solution that can be used along with the integrated power management unit.

6.5.0.2. Thermal Balls

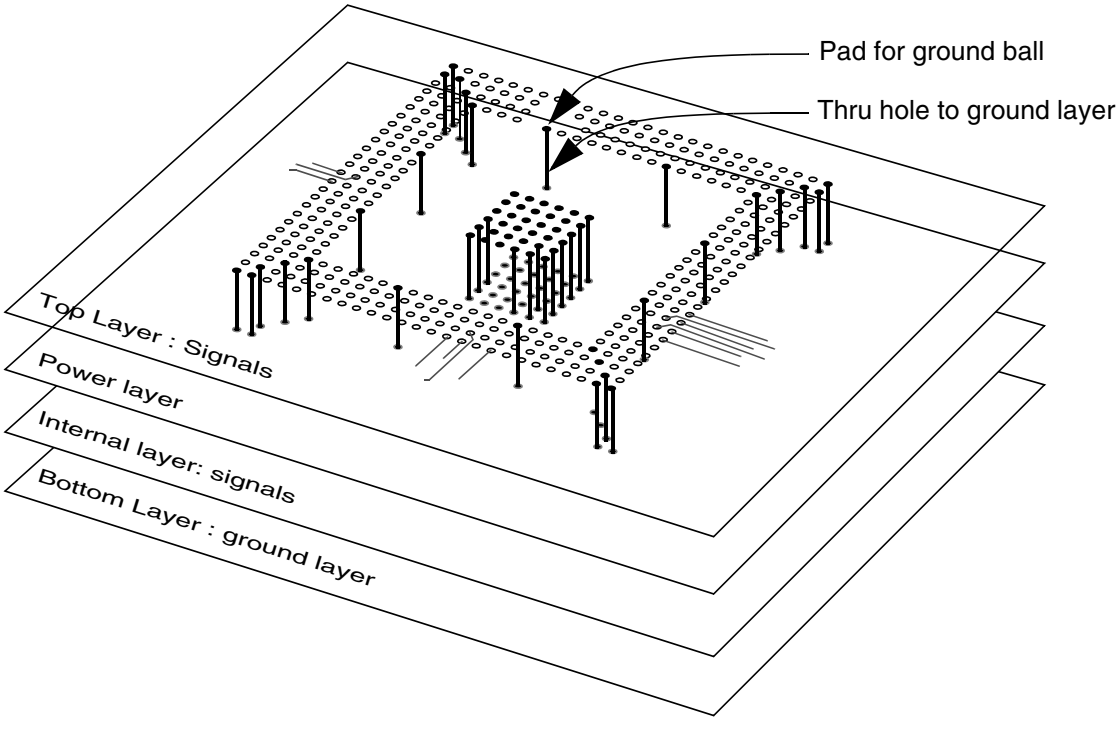
The standard way to route thermal balls to ground layer implements only one via pad for each ball pad, connected using a 8-mil wire.

With such configuration the Plastic BGA package does 90% of the thermal dissipation through the ground balls, and especially the central thermal balls which are directly connected to the die. The remaining 10% is dissipated through the case. Adding a heat sink reduces this value to 85%.

As a result, some basic rules must be followed when routing the STPC in order to avoid thermal problems.

As the whole ground layer acts as a heat sink, the ground balls must be directly connected to it, as illustrated in Figure 6-26. If one ground layer is not enough, a second ground plane may be added.

Figure 6-26. Ground Routing

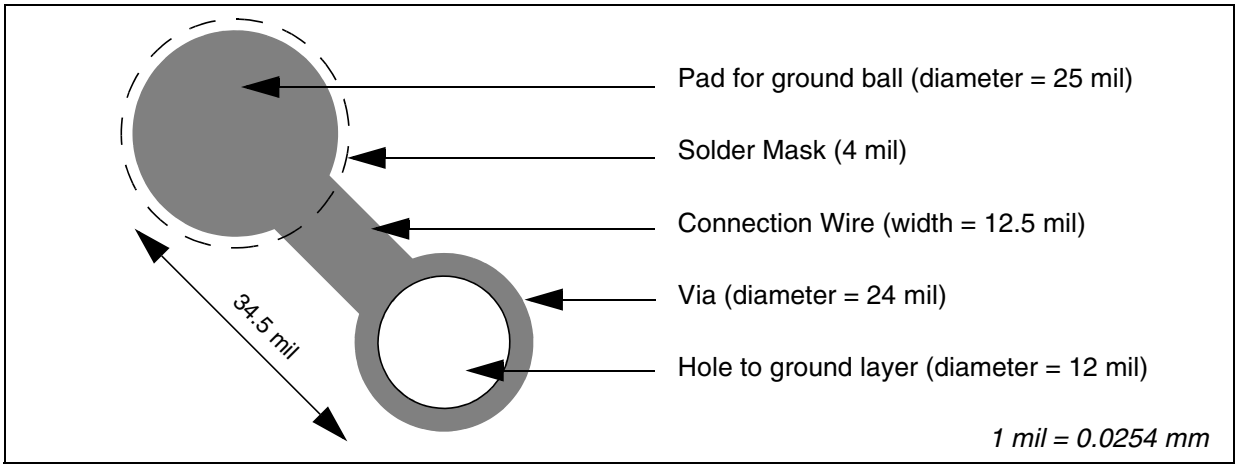


Note: For better visibility, ground balls are not all routed.

When considering thermal dissipation, one of the most important parts of the layout is the connection between the ground balls and the ground layer.

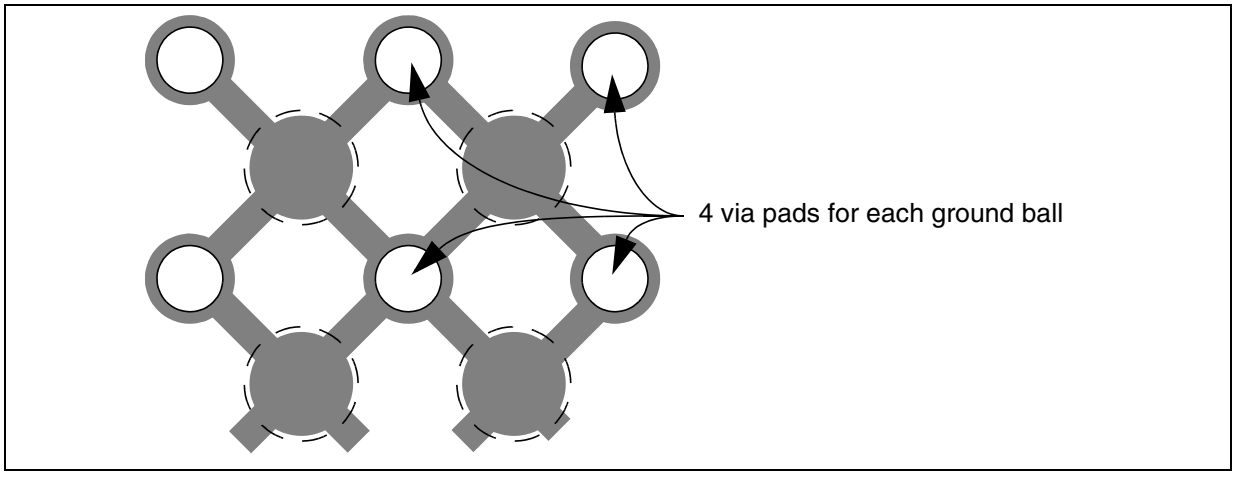
A 1-wire connection is shown in Figure 6-27. The use of a 8-mil wire results in a thermal resistance of 105°C/W assuming copper is used (418 W/m.°K). This high value is due to the thickness (34 µm) of the copper on the external side of the PCB.

Figure 6-27. Recommended 1-wire Power/Ground Pad Layout



Considering only the central matrix of 36 thermal balls and one via for each ball, the global thermal resistance is 2.9°C/W. This can be easily improved using four 12.5 mil wires to connect to the four vias around the ground pad link as in Figure 6-28. This gives a total of 49 vias and a global resistance for the 36 thermal balls of 0.5°C/W.

Figure 6-28. Recommended 4-wire Ground Pad Layout

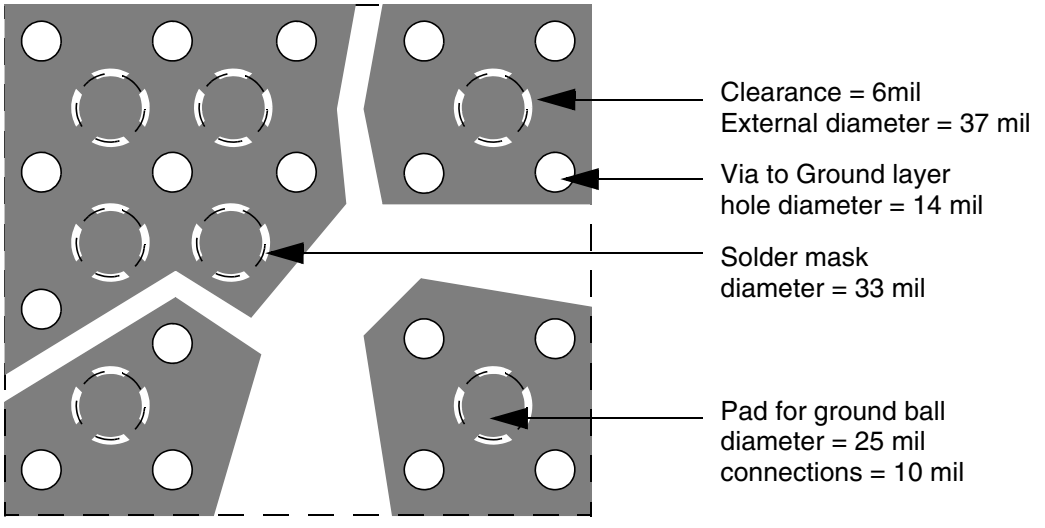


The use of a ground plane like in Figure 6-29 is even better.

To avoid solder wicking over to the via pads during soldering, it is important to have a solder mask of 4 mil around the pad (NSMD pad). This gives a diameter of 33 mil for a 25 mil ground pad.

To obtain the optimum ground layout, place the vias directly under the ball pads. In this case no local board distortion is tolerated.

Figure 6-29. Optimum Layout for Central Ground Ball - Top Layer



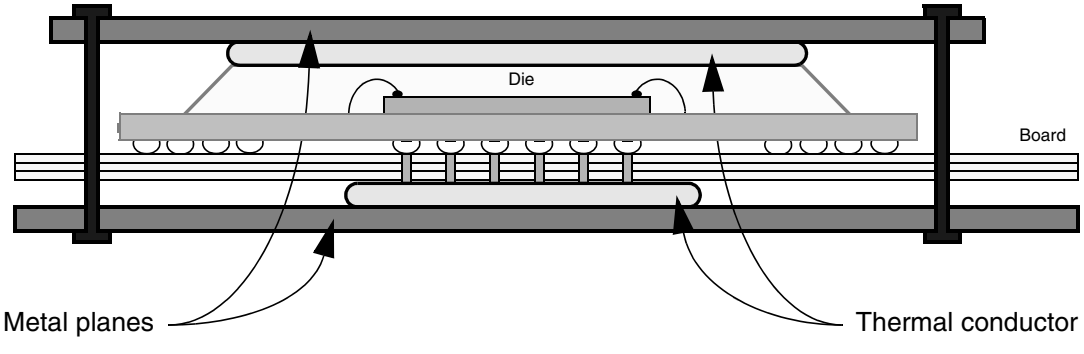
6.5.0.3. Heat Dissipation

The thickness of the copper on PCB layers is typically 34 µm for external layers and 17 µm for internal layers. This means that thermal dissipation is not good; high board temperatures are concentrated around the devices and these fall quickly with increased distance.

Where possible, place a metal layer inside the PCB; this improves dramatically the spread of heat and hence the thermal dissipation of the board.

The possibility of using the whole system box for thermal dissipation is very useful in cases of high internal temperatures and low outside temperatures. Bottom side of the PBGA should be thermally connected to the metal chassis in order to propagate the heat flow through the metal. Thermally connecting also the top side will improve furthermore the heat dissipation. Figure 6-30 illustrates such an implementation.

Figure 6-30. Use of Metal Plate for Thermal Dissipation



As the PCB acts as a heat sink, the layout of top and ground layers must be done with care to maximize the board surface dissipating the heat. The only limitation is the risk of losing routing channels. Figure 6-31 and Figure 6-32 show a partial routing with a good thermal dissipation thanks to an optimized placement of power and signal vias.

The ground plane should be on bottom layer for the best heat spreading (thicker layer than internal ones) and dissipation (direct contact with air).

Figure 6-31. Layout for Good Thermal Dissipation - Top Layer

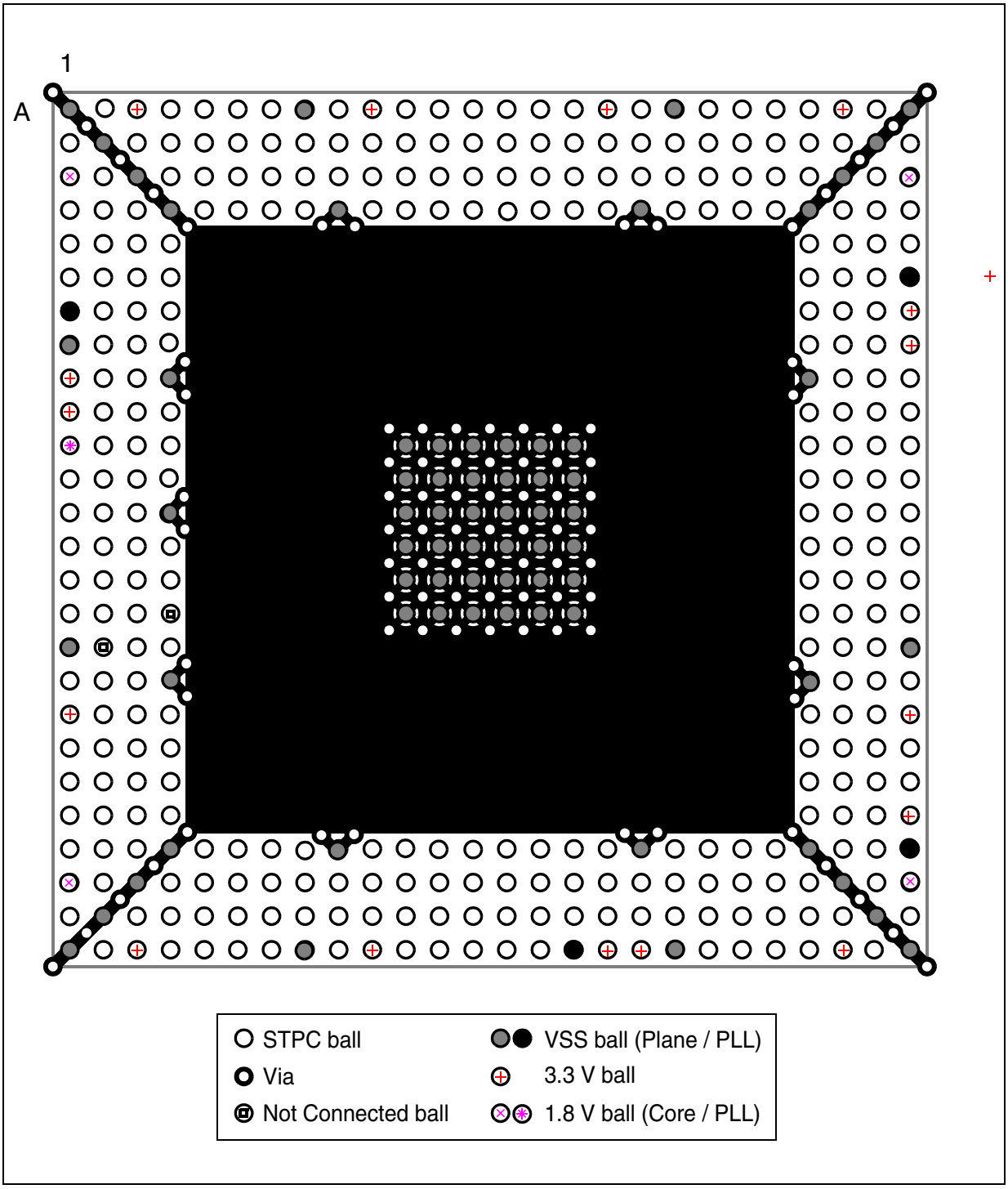
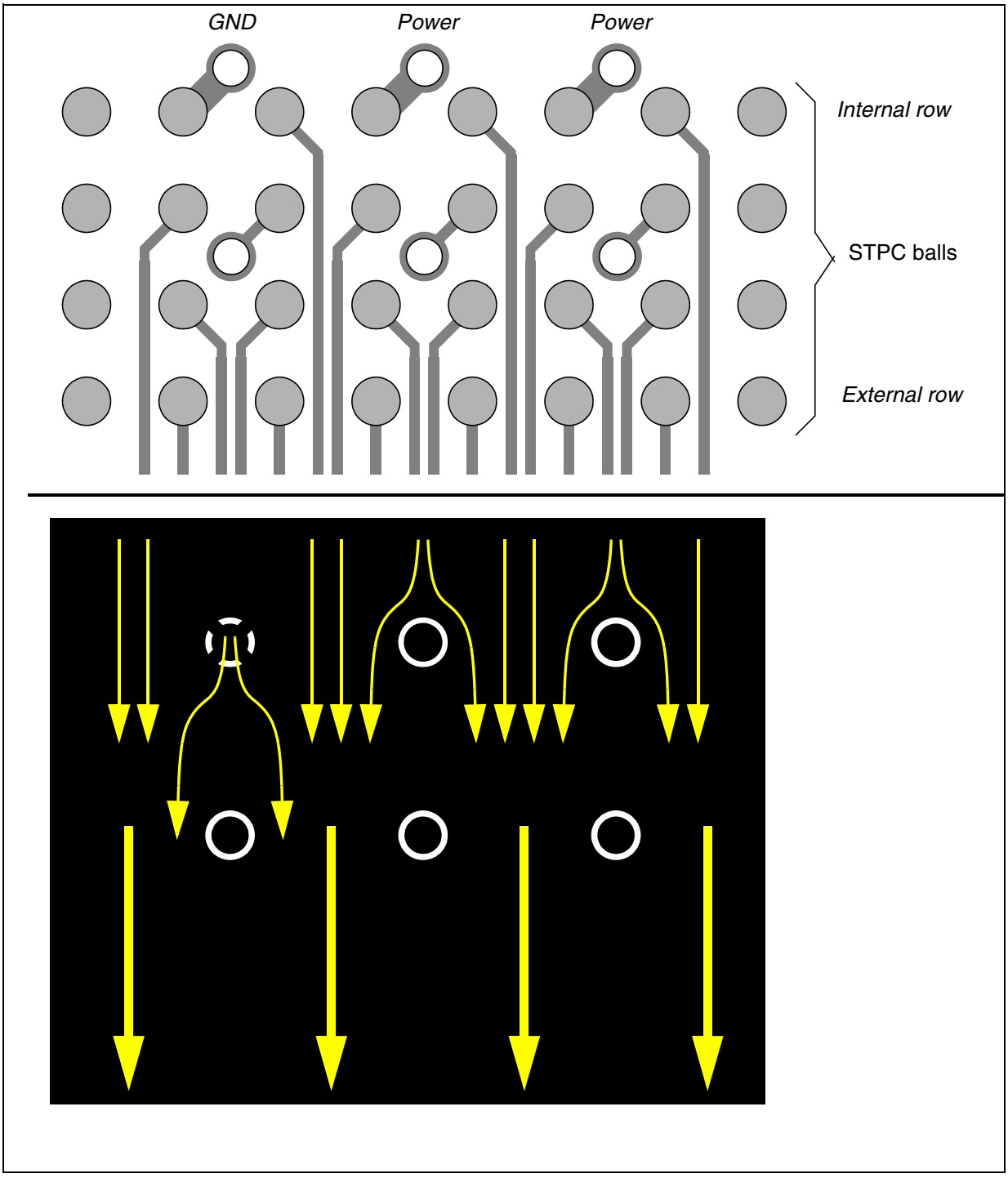


Figure 6-32. Recommend Signal Wiring (Top & Ground Layers) with Corresponding Heat Flow



6.6 DEBUG METHODOLOGY

In order to bring a STPC-based board to life with the best efficiency, it is recommended to follow the check-list described in this section.

6.6.1 POWER SUPPLIES

In parallel with the assembly process, it is useful to get a bare PCB to check the potential short-circuits between the various power and ground planes. This test is also recommended when the first boards are back from assembly. This will avoid unpleasant surprises in case of a short-circuit due to a bad soldering.

When the system is powered on, all power supplies, including the PLL power pins must be checked to be sure the right level is present. See Table 4-2. for the exact supported voltage range:

VDD_CORE: 1.8V
VDD_xxxPLL: 1.8V
VDD: 3.3V

6.6.2 BOOT SEQUENCE

6.6.2.1. Reset input

The checking of the reset sequence is the next step. The waveform of SYSRSTI# must comply with the timings described in Figure 4-3. This signal must not have glitches and must stay low until the 14.31818MHz output (OSC14M) is at the right frequency and the strap options are stabilized to a valid configuration.

In case this clock is not present, check the 14MHz oscillator stage (see Figure 6-3).

6.6.2.2. Strap options

The STPC has been designed to allow configurations for test purposes that differ from the functional configuration. In many cases, the problems at this stage of the debug are the result of bad strap options. This is why it is mandatory to check they are properly setup and sampled during the boot sequence.

The list of all the strap options is summarized at the beginning of Section 3

6.6.2.3. Clocks

Once OSC14M is checked and correct, the next signals to measure are the Host clock (HCLK), PCI clocks (PCI_CLKO, PCI_CLKI) and Memory clock (MCLKO, MCLKI).

HCLK must run at the speed defined by the corresponding strap options (see Section 3) and must not exceed 133MHz. Therefore the appropriate clock multiplication factor must be selected for CPU frequencies above this limit.

PCI_CLKI and PCI_CLKO must be connected as described in Figure 6-24 and not be higher than 33MHz. Their speed depends on HCLK and on the strap option settings in Section 3
To ensure a correct behaviour of the device, refer to the timings constraints, refers to Section 4.5.4

MCLKI and MCLKO must be connected as described in Figure 6-5 to Figure 6-7 depending on the SDRAM implementation. The memory clock must run at HCLK speed when in synchronous mode and must not be higher than 100MHz in any case.

6.6.2.4. Reset output

If SYSRSTI# and all clocks are correct, then the SYSRSTO# output signal should behave as described in Figure 4-3 or Figure 4-4.

6.6.3 ISA MODE

Prior to check the ISA bus control signals, PCI_CLKI, ISA_CLK, ISA_CLK2X, and DEV_CLK must be running properly. If it is not the case, it is probably because one of the previous steps has not been completed.

6.6.3.1. First code fetches

When booting on the ISA bus, the two key signals to check at the very beginning are RMRTCCS# and FRAME#.

The first one is a Chip Select for the boot flash and is multiplexed with the IDE interface. It should toggle together with ISAOE# and MEMRD# to fetch the first 16 bytes of code. This corresponds to the loading of the first line of the CPU cache.

In case RMRTCCS# does not toggle, it is then necessary to check the PCI FRAME# signal. Indeed the ISA controller is part of the South Bridge and all ISA bus cycles are visible on the PCI bus.

If there is no activity on the PCI bus, then one of the previous steps has not been checked properly. If there is activity then there must be something conflicting on the ISA bus or on the PCI bus.

6.6.3.2. Boot Flash size

The ISA bus supports 8-bit and 16-bit memory devices. In case of a 16-bit boot flash, the signal

MEMCS16# must be activated during RMRTCCS# cycle to inform the ISA controller of a 16-bit device.

6.6.3.3. POST code

Once the 16 first bytes are fetched and decoded, the CPU core continue its execution depending on the content of these first data. Usually, it corresponds to a JUMP instruction and the code fetching continues, generating read cycles on the ISA bus.

Most of the BIOS and boot loaders read the content of the flash, decompress it in SDRAM, and then continue the execution by jumping to the entry point in RAM. This boot process ends with a JUMP to the entry point of the OS launcher.
These various steps of the booting sequence are coded by the so-called POST codes (Power-On Self-Test). A 8-bit code is written to the port 80H at the beginning of each stage of the booting process (I/O write to address 0080H) and can be displayed on two 7-segment display, enabling a fast visual check of the booting completion level.
Usually, the last POST code is 0x00 and corresponds to the jump into the OS launcher.

When the execution fails or hangs, the last written code stays visible on that display, indicating either the piece of code to analyse, or the area of the hardware that is not working properly.

6.6.4 LOCAL BUS MODE

As the Local Bus controller is located in the Host interface, there is no access to the cycles on the PCI, reducing the amount of signals to check.

6.6.4.1. First code fetches

When booting on the Local Bus, the key signal to check at the very beginning is FCS0# (or FCS0H#). This signal is a Chip Select for the boot flash and should toggle together with PRD# to fetch the first 16 bytes of code. This corresponds to the loading of the first line of the CPU cache.
In case FCS0# does not toggle, then one of the previous steps has not been done properly, like HCLK speed and CPU clock multiplier (x1, x2).

6.6.4.2. Boot Flash size

The Local Bus supports 8-bit and 16-bit memory devices. The size of the boot device is defined by the strap option **DACK_ENC[1]** as described in Section 3

6.6.4.3. POST code

Like in ISA mode, POST codes can be implemented on the Local Bus. The difference is that an IOCS# must be programmed at I/O address 80H prior to writing these code, the POST display being connected to this IOCS# and to the lower 8 bits of the bus.

6.6.5 SUMMARY

Here is a check-list for the STPC board debug from power-on to CPU execution.

For each step, in case of failure, verify first the corresponding balls of the STPC:
- check if the voltage or activity is correct
- search for potential shortcuts.

For troubleshooting in steps 5 to 10, verify the related strap options:
- value & connection. Refer to Section 3
- see Figure 4-3 or Figure 4-4 for timing constraints

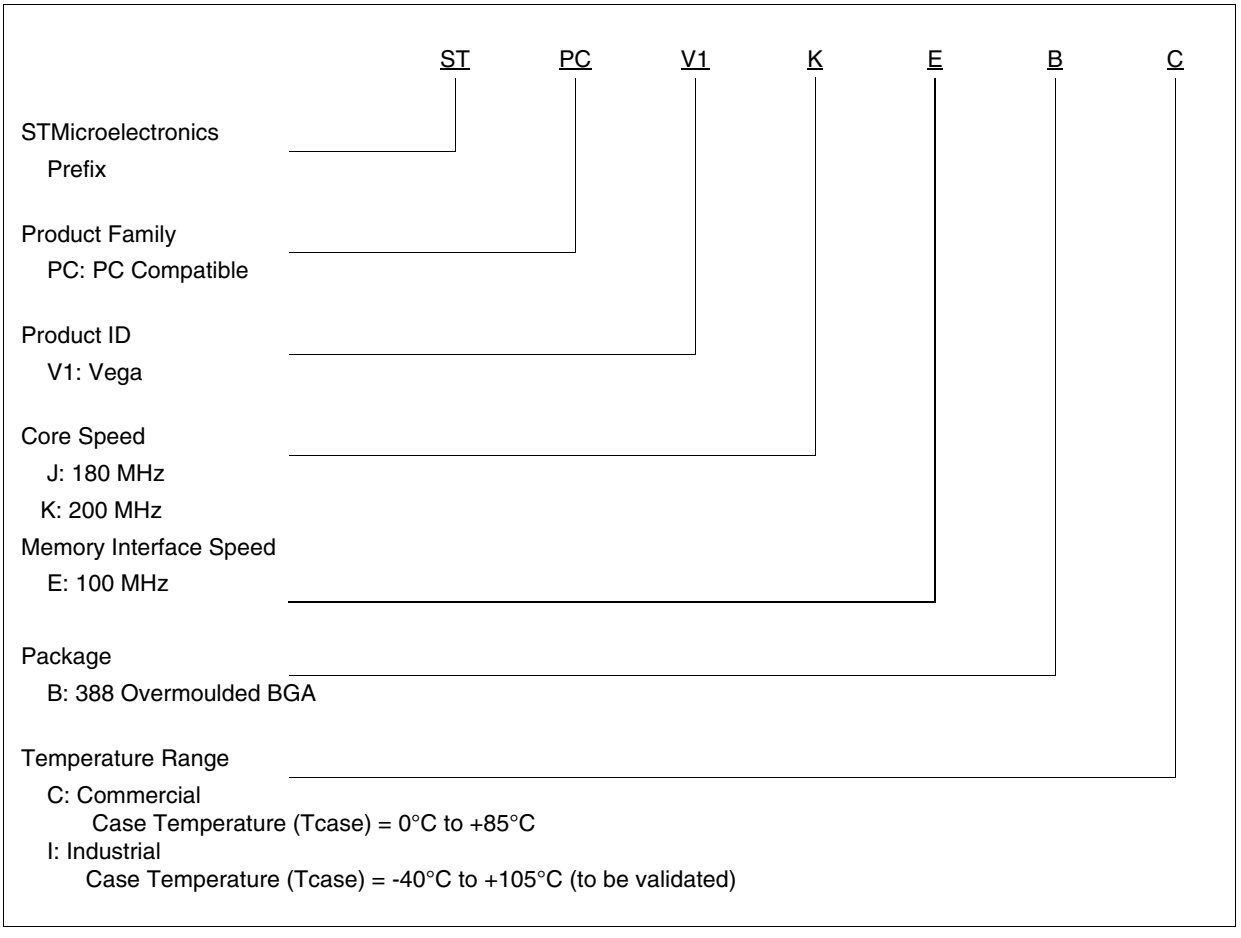
Steps 8a and 9a are for debug in ISA mode while steps 8b and 9b are for Local Bus mode.

	Check:	How?	Troubleshooting
1	Power supplies	Verify that voltage is within specs: - this must include HF & LF noise - avoid full range sweep Refer to Table 4-4. for values	Measure voltage near STPC balls: - use very low GND connection. Add a decoupling capacitor: - the smaller the capacitor, the closer to STPC balls.
2	14.318 MHz	Verify OSC14M speed	The 2 capacitors used with the quartz must match with the capacitance of the crystal. Try other values.
3	SYSRSTI# (Power Good)	Measure SYSRSTI# of STPC See Figure 4-3 for waveforms.	Verify reset generation circuit: - device reference - component values
5	HCLK	Measure HCLK is at selected frequency 25MHz < HCLK < 133MHz	HCLK wire must be as short as possible
6	PCI clocks	Measure PCICLKO: - maximum is 33MHz by standard - check it is at selected frequency Check PCICLKI equals PCICLKO	Verify PCICLKO loops to PCICLKI. Verify maximum skew between any PCI clock branch is below 1,80 ns. In Synchronous mode, check MCLKI.
7	Memory clocks	Measure MCLKO: - use a low-capacitance probe - maximum is 100MHz - check it is at selected frequency - In SYNC mode MCLK=HCLK - in ASYNC mode, default is 66MHz Check MCLKI equals MCLKO	Verify load on MCLKI. Verify MCLK programming (BIOS setting).
4	SYSRSTO#	Measure SYSRSTO# of STPC See Figure 4-3 for waveforms.	Verify SYSRSTI# duration. Verify SYSRSTI# has no glitch. Verify clocks are running.
8a	PCI cycles	Check PCI signals are toggling: - FRAME#, IRDY#, TRDY#, DEVSEL# - these signals are active low. Check, with a logic analyzer, that first PCI cycles are the expected ones: memory read starting at address with lower bits to 0xFFF0	Verify PCI slots If the STPC doesn't boot: - verify data read from boot memory is OK - ensure Flash is correctly programmed - ensure CMOS is cleared

	Check:	How?	Troubleshooting
9a	ISA cycles to boot memory	Check RMRTCCS# & MEMRD# Check directly on boot memory pin	Verify MEMCS16#: - must not be asserted for 8-bit memory Verify IOCHRDY is not be asserted Verify ISAOE# pin: - it controls IDE / ISA bus demultiplexing
8b	Local Bus cycles to boot memory	Check FCS0# & PRD# Check directly on boot memory pin	Verify HCLK speed and CPU clock mode. Verify 8/16bits strap option.
9b		Check, with a logic analyzer, that first Local Bus cycles are the expected one: memory read starting at the top of boot memory less 16 bytes	If the STPC doesn't boot - verify data read from boot memory is OK - ensure Flash is correctly programmed - ensure CMOS is cleared.
10	The CPU fills its first cache line by fetching 16 bytes from boot memory. Then, the first instructions are executed from the CPU. Any boot memory access done after the first 16 bytes is due to the instructions executed by the CPU => Minimum hardware is correctly set, CPU executes code. Please refer to the Bios Writer's Guide or Programming Manual to go further with your board testing.		

7 ORDERING INFORMATION

7.1 ORDERING INFORMATION SCHEME



7.2 ORDER CODES

Part Number	Core Frequency (MHz)	Memory Interface Speed (MHz)	Tcase Range (°C)
STPCV1KEBC	200	100	0°C to +85°
STPCV1JEBI	180	100	-40°C to +105°
STPCV1KEBI	200	100	-40°C to +105°

7.3 CUSTOMER SERVICE

More information is available on the STMicroelectronics Internet site *http://www.st.com/mcu*

8 REVISION HISTORY

Table 8-1. Revision History

Date	Revision	Description of Changes
20-Oct-04	1	First release on internet