LORAL
Fairchild Imaging Sensors

CCD321A/B
455/910—Bit
Analog Shift Register
Charge Coupled Device

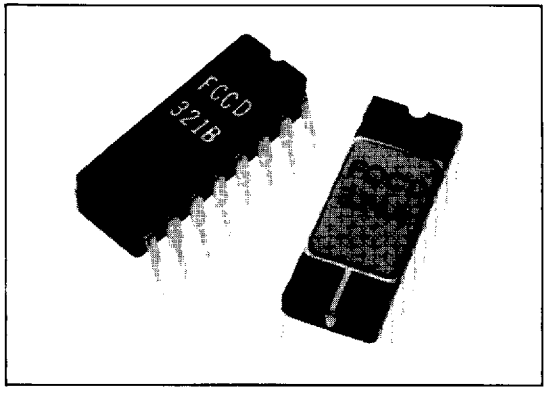
FEATURES

- **Electrically variable analog delay line for audio and video applications.**
- **1 H video delay line capability with broadcast quality performance.**
- **Excellent bandwidth at video and audio rates due to buried channel technology.**
- **Wide range of data rate: from 10 kHz to 20 MHz per 455 section.**
- **High signal to noise ratio — Video: 58 dB, Audio: 65 dB.**
- **Special modifications available — consult factory.**

DESCRIPTION

The CCD321 is an electrically variable analog delay line intended to be used in analog signal processing systems that include delay and temporary storage of analog information. The CCD321 consists of two 455-bit analog shift registers, each with its own injection port, transport clock and output port allowing the device to be used as two 455 or one 910-bit analog delay line.

The CCD321 can be used in applications ranging from video frequencies to audio frequencies. A complete TV line of 63.5μs can be stored with a sampling frequency of 14.318 MHz (four times color subcarrier frequency of 3.58 MHz). Applications in video systems include time base correction, comb filtering and signal-to-noise enhancing. Audio applications include variable delay of audio signals, reverberation effects in stereo equipment, tone delay in organs and musical instruments as well as voice scrambling applications. The CCD321 also finds applications in time base compression and expansion applications where analog data can be fed at one rate to the device, the clocks can be temporarily stopped and then data clocked out at a different rate.



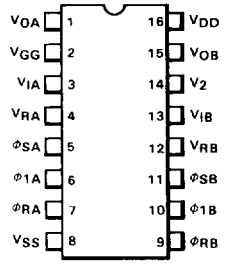
The CCD321B is an improved pin-for-pin replacement for the CCD321A. The CCD321 is available in four different classes as follows:

DEVICE	APPLICATION
CCD321A-1	Broadcast quality video delay line
CCD321A-2/B-2	Industrial video delay line
CCD321A-3/B-3	Time base compression and expansion delay line
CCD321A-4/B-4	Audio delay line

PIN NAMES

Φ_{1A}.Φ_{1B}	Analog Shift Register Transport Clocks
Φ_{SA}.Φ_{SB}	Input Sampling Clocks
Φ_{RA}.Φ_{RB}	Output Sample and Hold Clocks
V_2	Analog Shift Register DC Transport Phase
V_{IA}.V_{IB}	Analog Inputs
V_{RA}.V_{RB}	Analog Reference Inputs
V_{OA}.V_{OB}	Analog Outputs
V_{DD}	Output Drain
V_{GG}	Signal Ground
V_{SS}	Substrate Ground

PIN CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)



Signal Processing

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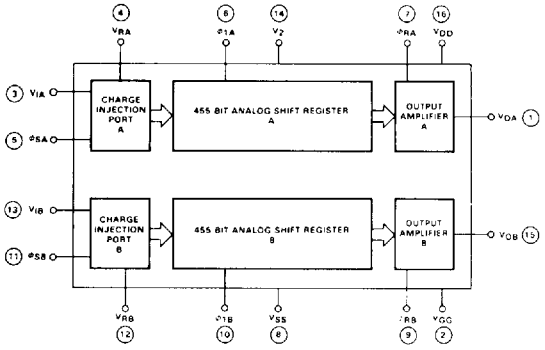
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION — The CCD321 consists of the following elements illustrated in the Block Diagram:

Two Charge Injection Ports — The analog information in voltage form is applied to two input ports at V_{IA} (or V_{IB}). Upon the activation of the analog sample clocks ϕ_{SA} (or ϕ_{SB}) a charge packet linearly dependent on the voltage difference between V_{IA} and V_{RA} (or V_{IB} and V_{RB}) is injected into analog shift register A (or B).

Two 455-Bit Analog Shift Registers — Each register transports the charge packets from the charge injection port to its corresponding output amplifier. Both registers are operated in the 1-1/2 phase mode where one phase (ϕ_{1A} or ϕ_{1B}) is a clock and the other phase (V_2) is an intermediate dc potential. Phases ϕ_{1A} and ϕ_{1B} are completely independent. V_2 is a dc voltage common to both registers.

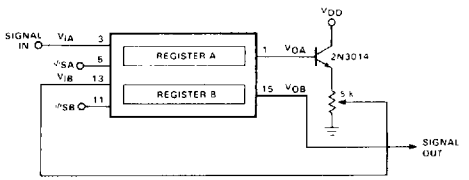
Two Output Amplifiers — Charge packets from each analog shift register are delivered to their corresponding output amplifier as shown in the circuit diagram. Each output amplifier consists of three source follower stages with constant current source bias. A sample and hold transistor is located between the second and third stage of the amplifier. When the gate of the sample and hold transistor is clocked (ϕ_{RA} or ϕ_{RA}) a continuous output waveform is obtained as shown in the timing diagrams. The sample and hold transistor can be defeated by connecting ϕ_{RA} and/or ϕ_{RB} to V_{DD}. In this case the output is a pulse modulated waveform as shown in the timing diagram.

MODES OF OPERATION — The CCD321 can be operated in four different modes:

455-Bit Analog Delay — Either 455-bit analog shift register can be operated independently as a 455-bit delay line. The driving waveforms to operate shift register A is shown in Fig. 10. The input voltage signal is applied directly to V_{IA}. The input sampling clock ϕ_{SA} samples this input voltage and injects a proportional amount of charge packet into the first bit of register A. The input voltage A_1 which is sampled between $t = 0$ and $t = t_C$ appears at the output terminal V_{OA} @ $t = 910t_C$. If the sample and hold circuit is not used then the output appears as a pulse amplitude modulated waveform as shown in the diagram. In that case ϕ_{RA} (pin 7) should be connected to V_{DD} (pin 16). If the sample and hold circuit is used then the output appears as a continuous waveform. Here ϕ_{RA} (pin 7) should be clocked coincident with ϕ_{SA} (pin 5) and the two pins can be connected together.

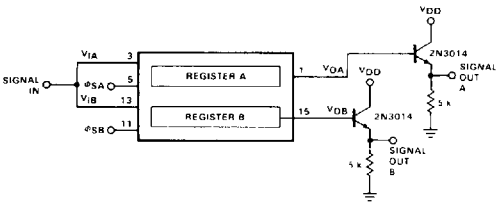
Analog shift register B can be operated in an analogous manner with V_{IB} as the analog input, ϕ_{1B} as the transport clock, ϕ_{SB} as the input sampling clock and ϕ_{RB} as the output sample and hold clock.

910-Bit Analog Delay in Series Mode — The two analog shift registers A and B can be connected in series to provide 910 bits of analog delay as shown in the schematic below. The analog signal input voltage is applied to V_{IA}. The output of register A is connected to the input of register B with a simple emitter follower buffer stage. In order to insure proper charge injection of register B , V_{RB} should be adjusted. The timing diagram shown in Fig. 10 applies in this mode of operation. Here $\phi_{1A} = \phi_{1B}$, $\phi_{SA} = \phi_{SB}$, $\phi_{RA} = V_{DD}$, and ϕ_{RB} is clocked.



910-Bit Analog Delay in Multiplexed Mode — The two analog shift registers can be connected in parallel to provide 910-bit of analog delay as shown in the schematic below. The analog signal input voltage is applied to both V_{IA} and V_{IB}. The outputs at V_{OA} and V_{OB} can be combined as shown in Fig. 8 to recover the analog input information.

The necessary waveforms to operate the device in this mode is shown in Fig. 11. In this case ϕ_{SA} samples the analog input A_1 at V_{IA} between $t = 0$ and $t = t_C$. ϕ_{SB} samples the analog input B, at V_{IB}, between $t = t_C$ and $t = 2t_C$. The output corresponding to A_1 appears at V_{OA} at $t = 910t_C$. The output corresponding to B_1 appears at V_{OB} @ $t = 911t_C$. This mode of operation results in an effective sampling rate of twice the rate of ϕ_{1A}, ϕ_{1B}, ϕ_{SA} and ϕ_{SB}.



Stop/Start Mode Operation — The charge packets in the two analog shift registers can be held stationary by stopping ϕ_{1A} and ϕ_{1B} in their LOW state. ϕ_{SA}, ϕ_{SB}, ϕ_{RA}, ϕ_{RB} can also be stopped in the LOW state or kept clocking as usual. The two shift registers should not be connected in series in the stop-start mode of operation.

The CCD321 is available in four different classes for different applications. The CCD321A-1 is a high quality broadcast 1H delay line for video systems with 1% differential gain and 1° differential phase. The CCD321A-2/B-2 is a high quality video delay line with 3% differential gain and 3° differential phase.

The CCD321A-3/B-3 is tested in the START/STOP mode of operation and parameters are guaranteed in this mode. The CCD321A-4/B-4 is tested at audio speeds; audio parameters are specified and guaranteed. The dc and clock characteristics of the four classes are the same. The ac characteristics vary as shown below.

Caution: The device has limited built-in gate protection. Charge build-up should be minimized. Care should be taken to avoid shortings pins V_{OA} and V_{OB} to ground during operation of the device.

DC CHARACTERISTICS: T_A = 55° C, Note 16

SYMBOL	CHARACTERISTICS	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{DD}	Output Drain Voltage	14.5	15.0	15.5	V	
V_2	Analog Shift Register DC Transport Phase Voltage		6.0		V	Note 1
V_{RA}, V_{RB}	Analog Reference Inputs Voltage		3-7		V	Note 2
V_{GG}	Signal Ground		0.0			
V_{SS}	Substrate Ground		0.0			Note 3
V_{IA}, V_{IB}	Input DC Level		3-7		V	Note 2
V_{OA}, V_{OB}	Output DC Level		6-11		V	V_{DD} = 15 V
R_{IN}	Small Signal Input Resistance		1.0		MΩ	Resistance from Pins 3, 4, 12 or 13 to V_{SS}. V_{IA} = V_{IB} = 3 V
C_{IN}	Small Signal Input Capacitance		10		pF	Capacitance from Pins 3, 4, 12 or 13 to V_{SS}. V_{IA} = V_{IB} = 3 V
R_{OUT}	Small Signal Output Resistance		250		Ω	V_{DD} = 15 V
ODM	Output DC Mismatch Between A & B Registers		±1		V	
OAM	Output AC Mismatch Between A & B Registers		±20		%	

CLOCK CHARACTERISTICS: T_A = 55° C, Note 16

SYMBOL	CHARACTERISTICS	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V\phi_{1AL}$, $V\phi_{1BL}$	Analog Shift Register Transport Clocks LOW	0	0.5	0.8	V	Note 4
$V\phi_{1AH}$, $V\phi_{1BH}$	Analog Shift Register Transport Clocks HIGH	12.0	13.0	15.0	V	Note 4
$V\phi_{SAL}$, $V\phi_{SBL}$	Input Sampling Clocks LOW	0	0.5	0.8	V	Note 5
$V\phi_{SAH}$, $V\phi_{SBH}$	Input Sampling Clocks HIGH	12.0	13.0	15.0	V	Note 5
$V\phi_{RAL}$, $V\phi_{RBL}$	Output Sample and Hold Clocks LOW	0	0.5	0.8	V	Note 6
$V\phi_{RAH}$, $V\phi_{RBH}$	Output Sample and Hold Clocks HIGH	12.0	13.0	15.0	V	Note 6
$f\phi_{1A}$,$f\phi_{1B}$	Analog Shift Register Transport Clock Frequency	0.02		20	MHz	See Note 17
$f\phi_{SA}$,$f\phi_{SB}$	Input Sampling Clocks Frequency	0.02		20	MHz	See Note 17
$f\phi_{RA}$,$f\phi_{RB}$	Output Sample and Hold Clocks Frequency	0.02		20	MHz	See Note 17

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−25°C to 100°C
Operating Temperature	−25°C to 55°C
All Pins with Respect to V_{SS}	−0.3 V to 18 V

CCD321A-1 AC CHARACTERISTICS: T_A = 55°C. Both registers in the multiplexed mode, Clock Rate = 7.16 MHz. Sampling Rate = 14.32 MHz. Vout ≅ 700 mV. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	5.0			MHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
Δ G	Differential Gain			2.0	%	Note 9
Δ φ	Differential Phase			1.0	degree	Note 9
S/N	Signal-to-Noise Ratio	58			dB	Note 10
$V_{I\ (max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	

CCD321A-2/B-2 AC CHARACTERISTICS: T_A = 55°C. Both registers in the multiplexed mode, Clock Rate = 7.16 MHz, Sampling Rate = 14.32 MHz. V_{OUT} ≅ 700 mV. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	4.2	5.0		MHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
Δ G	Differential Gain			3.0	%	Note 9
Δ φ	Differential Phase			3.0	degrees	Note 9
S/N	Signal-to-Noise Ratio	58			dB	Note 10
$V_{I\ (max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	

CCD321A-3/B-3 AC CHARACTERISTICS: T_A= 55°C. Both registers in the multiplexed mode, Clock Rate = 7.16 MHz, Sampling Rate = 14.32 MHz. Clocks are stopped for 300 μs. V_{OUT} ≅ 700 mV after 4.2 MHz low pass filter (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	4.2	5.0		MHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
Δ G	Differential Gain			3.0	%	Note 9
Δ φ	Differential Phase			3.0	degrees	Note 9
S/N	Signal-to-Noise Ratio	55			dB	Note 10
SN	Spacial Noise		10.0	20.0	mV	Notes 11, 12
$V_{I\ (max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	

CCD321A-4/B-4 AC CHARACTERISTICS: T_A=45°C. Both registers in the multiplexed mode, Clock Rate = 7.16 MHz, Sampling Rate = 14.32 MHz. V_{OUT} = 700 mV. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	23	25		kHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
THD	Total Harmonic Distortion		0.5	1.0	%	Note 13
S/N	Signal-to-Noise Ratio	60	65		dB	Note 14
$V_{I\ (max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	
RSO	Rate of Average Signal Offset		15		mv/ms	Note 15

NOTES:
1. V_2 level should be 1/2 of the ϕ_{1A} or ϕ_{2A} HIGH level. Adjustment in the range of ±1 V may be necessary to maximize signal bandwidth.
2. Signal charge injection is proportional to the difference V_I and V_R. Adjustment of either V_I or V_R is necessary to assure proper operation.
3. Negative transients below ground of fast rise and fall times of the clocks may cause charge injection from substrate to the shift registers. Anegative bias on V_{SS} of -2.0 to -5.0 Vdc will eliminate the injection phenomenon.
4. $C_{\phi 1A} = C_{\phi 1B}$ = 30 pF = Capacitance with respect to V_{SS}.
5. $C_{\phi SA} = C_{\phi SB}$ = 10 pF = Capacitance with respect to V_{SS}.
6. $C_{\phi RA} = C_{\phi RB}$ = 10 pF = Capacitance with respect to V_{SS}.
7. Signal Bandwidth is typically 1/3 to 1/2 of the sampling rate. See Fig. 1.
8. Insertion Gain = 20 Log V_{OUT}/V_{IN}.
9. Differential Gain and Differential Phase are measured with Tektronix NTSC Signal Generator (147A) and Vector Scope (520A). See Figure 2.
10. Video S/N is defined as the ratio the peak-to-peak output signal to RMS random (temporal) noise. The peak-to-peak signal is the maximum output level that satisfies the ΔG and Δφ specs. See Fig. 3.
11. In the start/stop mode of operation is recommended that the rise and fall times of ϕ_{1A} and ϕ_{1B} exceed 20 ns to eliminate charge injection.
12. Spacial Noise is the peak-to-peak spacial variation (fixed pattern noise) in the device output after clocks have been stopped. It is usually caused by the variation of leakage current density in the shift registers. Spacial noise is a function of the clock stop period and temperature. See Figure 5.
13. Input Signal = 1 kHz sine wave. See Figure 6.
14. Audio S/N is defined as the ratio of RMS signal to RMS noise at 23 kHz bandwidth. Both are measured with an HP3400A RMS Voltmeter. See Figure 6.
15. Rate of Average-Signal Offset is caused by leakage current in the registers. It is function of temperature. See Figure 7.
16. Devices are tested using the values shown in the typical columns.
17. Devices can be operated beyond 20 MHz without damage. The minimum clock rate can be lower than 10 kHz as shown in Figure 4.

TYPICAL VIDEO PERFORMANCE CURVES

FREQUENCY RESPONSE (FOR SINGLE REGISTER)

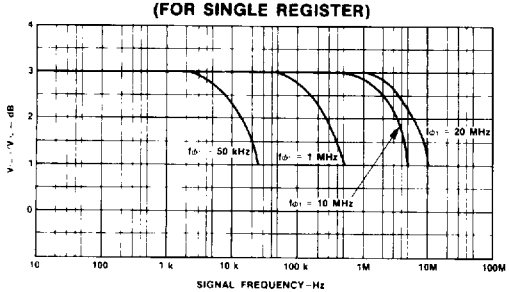


Fig. 1

DIFFERENTIAL GAIN AND PHASE VERSUS OUTPUT VOLTAGE

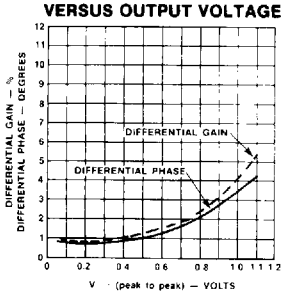


Fig. 2

DIFFERENTIAL GAIN AND PHASE VERSUS S/N RATIO

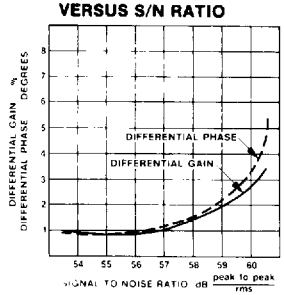


Fig. 3

V_{OUT} MAX VERSUS CLOCK FREQUENCY

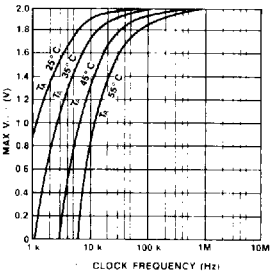


Fig. 4

SPACIAL NOISE VERSUS CLOCK STOP PERIOD

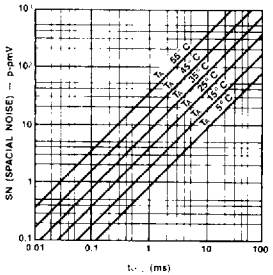


Fig. 5

Signal Processing

TYPICAL AUDIO PERFORMANCE CURVES

TOTAL HARMONIC DISTORTION (THD) AND S/N RATIO VERSUS V_{OUT}

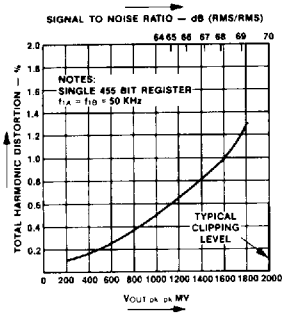


Fig. 6

RATE OF AVERAGE SIGNAL OFFSET VERSUS TEMPERATURE

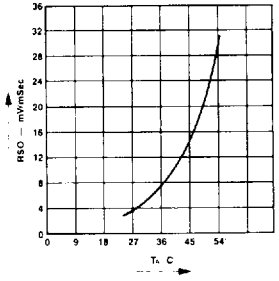


Fig. 7

TEST LOAD CONFIGURATION FOR MULTIPLEXED OPERATION IN VIDEO

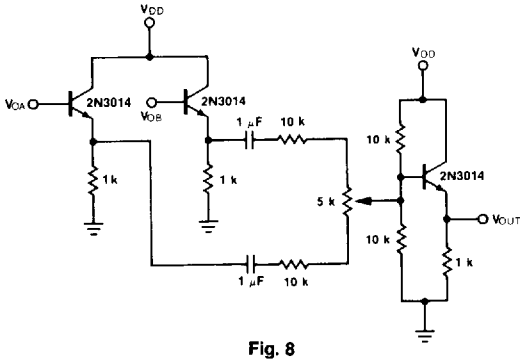


Fig. 8

TEST LOAD CONFIGURATION FOR SINGLE REGISTER OPERATION IN AUDIO AND VIDEO

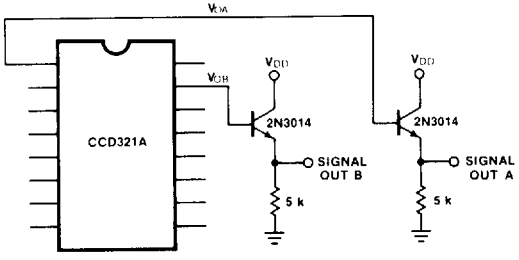
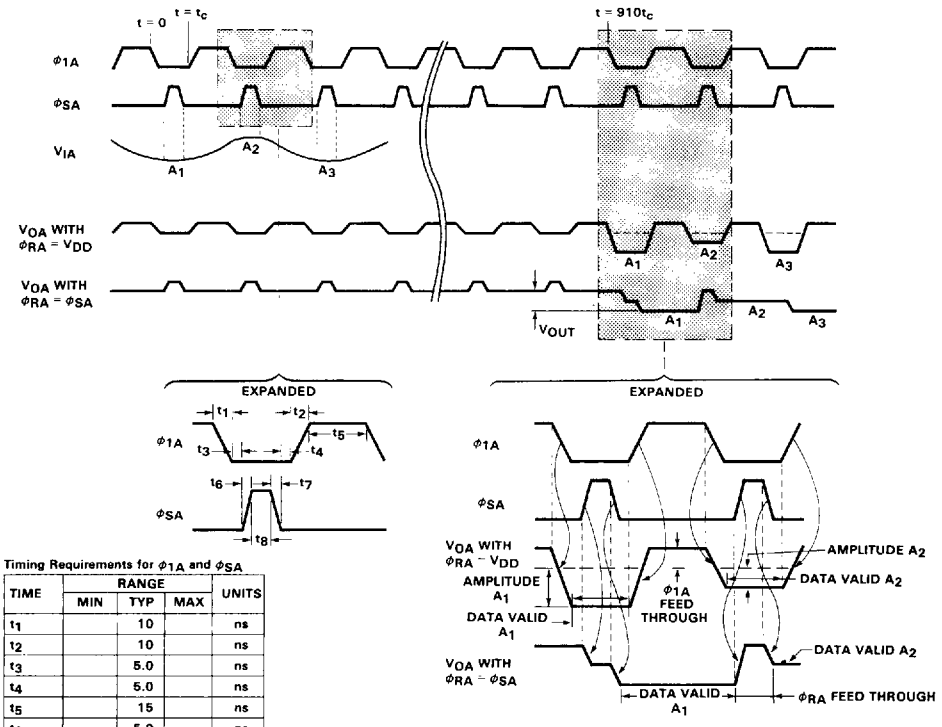


Fig. 9

TIMING DIAGRAM



Timing Requirements for ϕ_{1A} and ϕ_{SA}

TIME	RANGE			UNITS
	MIN	TYP	MAX	
t_1		10		ns
t_2		10		ns
t_3		5.0		ns
t_4		5.0		ns
t_5		15		ns
t_6		5.0		ns
t_7		5.0		ns
t_8		5.0		ns

NOTE:
This timing diagram also applies for shift register B. In this case ϕ_{1A} becomes ϕ_{1B}, ϕ_{SA} becomes ϕ_{SB}, V_{IA} becomes V_{IB} and V_{OA} becomes V_{OB}.

Fig. 10 Analog Shift Register A or B Operation

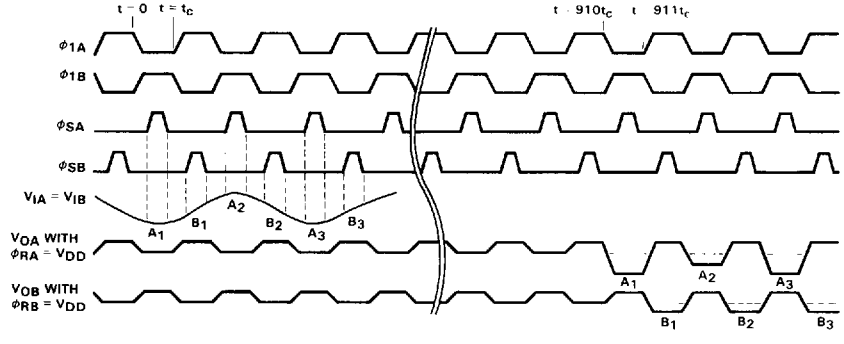
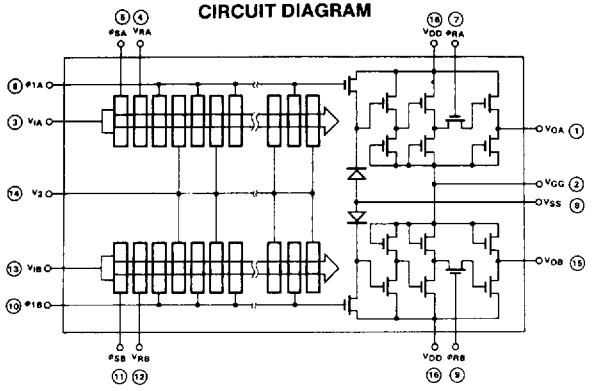


Fig. 11 Analog Shift Register A and B Operation in the Multiplexed Mode

CIRCUIT DIAGRAM



ORDERING INFORMATION

To order the CCD321 specify the "device and package type" as shown below:

CLASS, APPLICATION	SIDEBRAZE PKG.	CERDIP PKG.
Broadcast quality video	CCD321A1	
Industrial quality video	CCD321A2	CCD321B2
Time base compression and expansion	CCD321A3	CCD321B3
Audio delay line	CCD321A4	CCD321B4

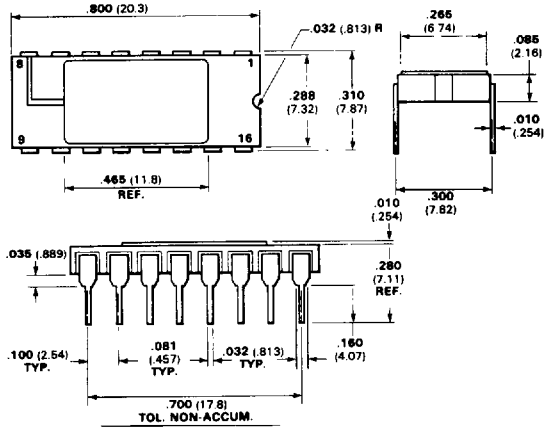
Also available is a fully-assembled module that contains all the necessary circuitry to operate the CCD321. The module is designed to help the system designer become familiar with the operation of the device, and for use in OEM systems.

The CCD321VM is a video module using a CCD321A-3 or B-3. The module includes the necessary electronics to perform time base compression and expansion, and variable video signal delay. The module requires a single power supply for operation.

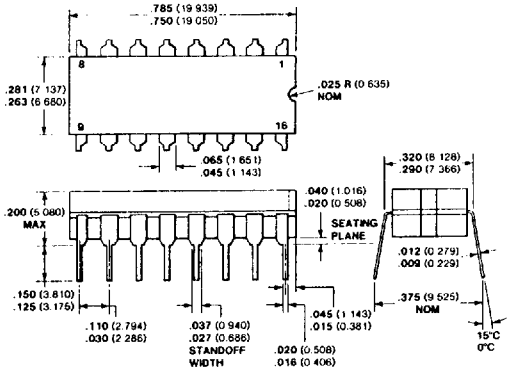
Schematics and component layouts are included in the shipping packages for the CCD321VM. For further information on the CCD321VM please contact your distributor.

PACKAGE OUTLINES

CCD321A: 16-PIN SIDEBRAZED



CCD321B: 16-PIN CERDIP



NOTES:
All dimensions in inches (bold) and millimeters (parentheses).
Header is black ceramic (Al_2O_3).
Pins are Alloy 42, plated with gold (321A) or nickel (321B).
Top cover connected to pin 8 (V_{SS} substrate) on 321A.

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