CYM1623

64K x 16 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 70 ns**
- **40-pin, 0.6-in.-wide DIP package**
- **JEDEC-compatible pin-out**
- **Low active power**
  - **1.3W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **2V data retention (L version)**

Functional Description

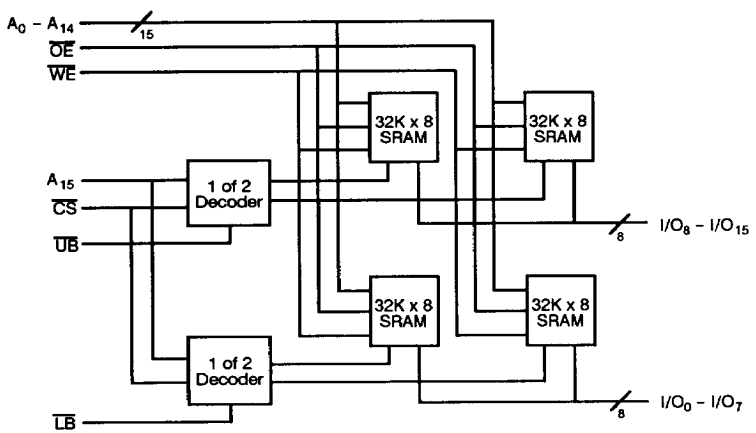
The CYM1623 is a high-performance 1-megabit static RAM module organized as 64K words by 16 bits. The module is constructed using four 32K x 8 static RAMs in leadless chip carriers mounted onto a double-sided multilayer ceramic substrate. A decoder is used to interpret the higher-order address A_{15} and to select one of the two pairs of RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins of the selected byte ($I/O_8 - I/O_{15}$, $I/O_0 - I/O_7$) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

The input/output pins remain in a high-impedance state when chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

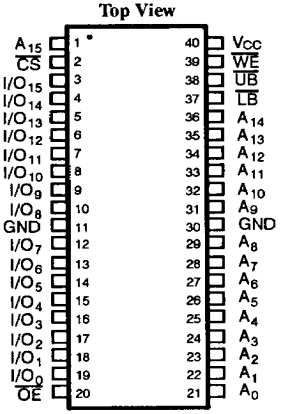
Logic Block Diagram



1623-1

Pin Configuration

DIP
Top View



1623-2

Selection Guide

		1623HD-70	1623HD-85	1623HD-100
Maximum Access Time (ns)		70	85	100
Maximum Operating Current (mA)	Commercial	240	240	240
Maximum Standby Current (mA)	Commercial	70	70	70

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −10°C to +70°C

Supply Voltage to Ground Potential ..... −0.3V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.3V to +7.0V

DC Input Voltage ..... −0.3V to +7.0V

Output Current into Outputs (Low) ..... 50 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1623HD		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −1.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	µA
I_{CCx16}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}$, $\overline{UB}$, & $\overline{LB}$ = V_{IL}		240	mA
I_{CCx8}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}		120	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		70	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		20	mA

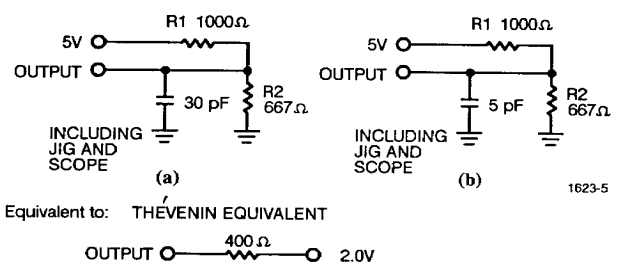
Capacitance [3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		40	pF

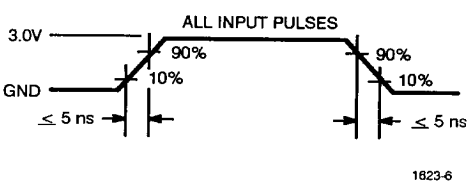
Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [4]

Parameters	Description	1623HD-70		1623HD-85		1623HD-100		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	70		85		100		ns
t_{AA}	Address to Data Valid		70		85		100	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		70		85		100	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		40		50		60	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		35		35		40	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [6]	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [5, 6]		35		35		40	ns
WRITE CYCLE [7]								
t_{WC}	Write Cycle Time	70		85		100		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	65		75		90		ns
t_{AW}	Address Set-Up to Write End	65		75		90		ns
t_{HA}	Address Hold from Write End	10		15		15		ns
t_{SA}	Address Set-Up to Write Start	25		25		30		ns
t_{PWE}	$\overline{WE}$ Pulse Width	60		70		80		ns
t_{SD}	Data Set-Up to Write End	30		35		35		ns
t_{HD}	Data Hold from Write End	10		10		15		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [6]	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [5, 6]	0	30	0	35	0	40	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.

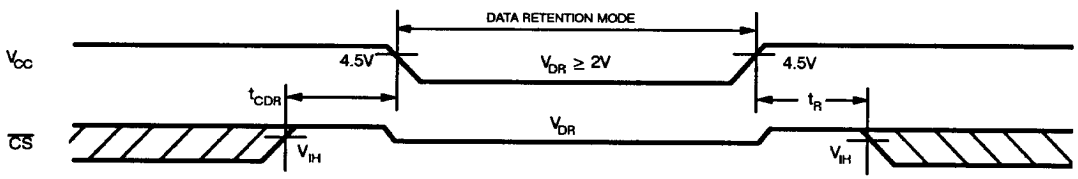
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1623		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			250	mA
t_{CDR} [13]	Chip Deselect to Data Retention Time		0		ns
t_R [13]	Operation Recovery Time		t_{RC} [12]		ns

Notes:

12. t_{RC} = Read Cycle Time.
13. Guaranteed, not tested.
14. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

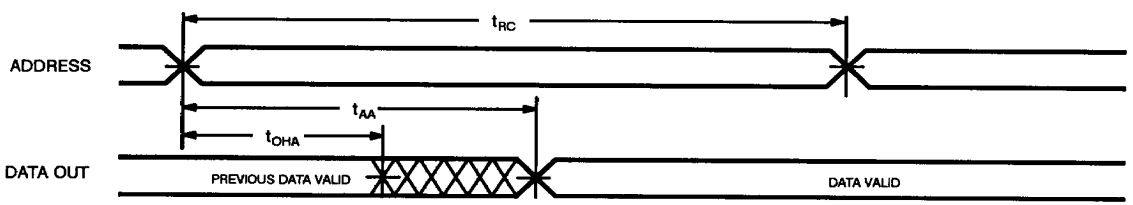
Data Retention Waveform



1623-7

Switching Waveforms [10]

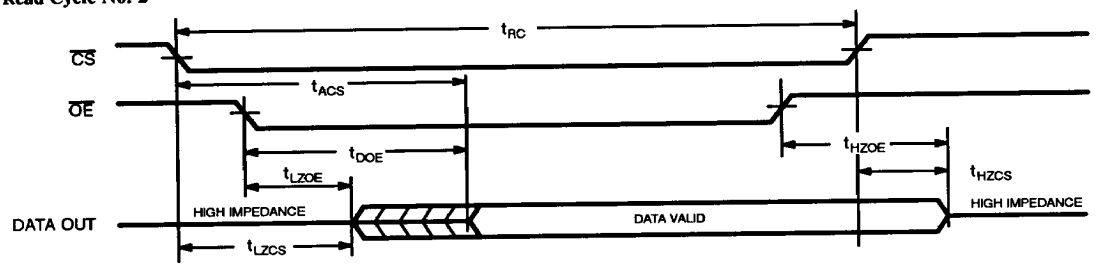
Read Cycle No. 1 [8, 9]



1623-8

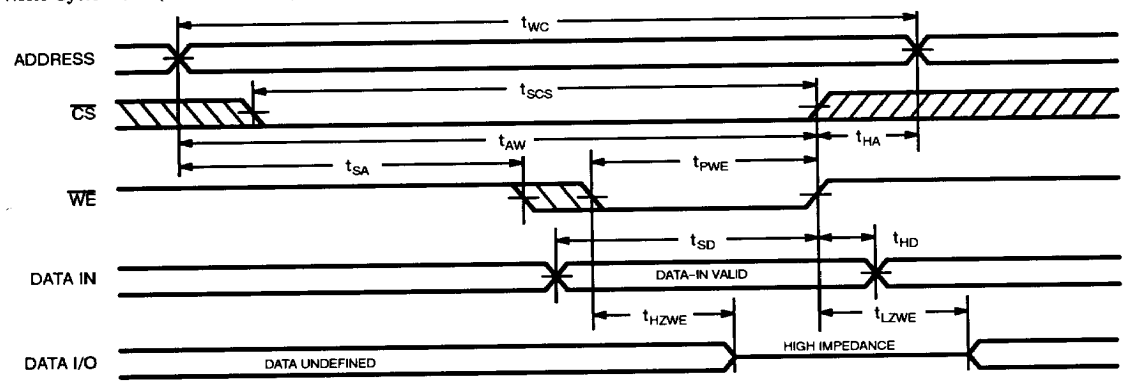
Switching Waveforms (continued)

Read Cycle No. 2[8, 10]



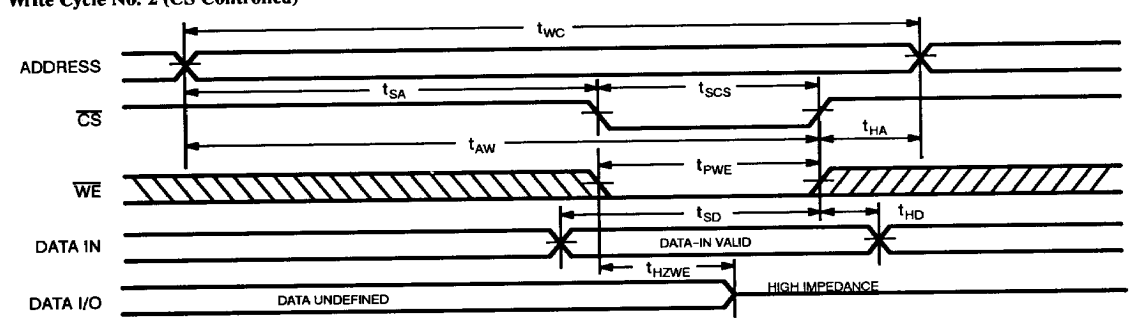
1623-9

Write Cycle No. 1 ($\overline{WE}$ Controlled)[7, 11]



1623-10

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11, 14]



1623-11

Truth Table

$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	Input/Outputs	Mode
H	X	X	X	X	High Z	Deselect/Power-Down
L	H	H	X	X	High Z	Deselect/Power-Down
L	L	L	L	H	Data Out_{0-15}	Read
L	H	L	L	H	Data Out_{0-7}	Read Lower Byte
L	L	H	L	H	Data Out_{8-15}	Read Upper Byte
L	L	L	X	L	Data In_{0-15}	Write
L	H	L	X	L	Data In_{0-7}	Write Lower Byte
L	L	H	X	L	Data In_{8-15}	Write Upper Byte
L	L	L	H	H	High Z	Deselect
L	H	L	H	H	High Z	Deselect
L	L	H	H	H	High Z	Deselect

Document #: 38-M-00011-A

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
70	CYM1623HD-70C	HD03	Commercial
	CYM1623LHD-70C	HD03	
85	CYM1623HD-85C	HD03	Commercial
	CYM1623LHD-85C	HD03	
100	CYM1623HD-100C	HD03	Commercial
	CYM1623LHD-100C	HD03	