HN29W6411 Series

More than 16,057-sector (67,824,768-bit) CMOS AND Flash Memory (Mostly Good Memory)

HITACHI

ADE-203-637C (Z)
Rev. 3.0
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Description

The Hitachi HN29W6411 Series is a CMOS Flash Memory with AND type memory cells. It has fully automatic programming and erase capabilities with a single 3.3 V and 5 V power supply. The functions are controlled by simple external commands. To fit the I/O card applications, the unit of programming and erase is as small as (512 + 16) bytes. Available sectors of HN29W6411 are more than 16,057 (98% of all sector address) and less than 16,384 sectors.

Features

- On-board single power supply (V_{CC})
  - V_{CC} = 3.3 V ± 0.3 V
  - V_{CC} = 5.0 V ± 0.5 V
- Organization
  - AND Flash Memory: (512 + 16) bytes × (More than 16,057 sectors)
  - Data register: (512 + 16) bytes
- Automatic programming
  - Sector program time: 1 ms (typ)
  - Address, data latch function
  - Internal automatic program verify function
  - Status data polling function
- Automatic erase
  - Single sector erase time: 1 ms (typ)
  - Block erase time: 1 ms (typ)
  - System bus free
  - Internal automatic erase verify function
  - Status data polling function
- Erase mode
  - Single sector erase ((512 + 16) byte unit)
  - Block erase ((4096 + 128) byte unit)

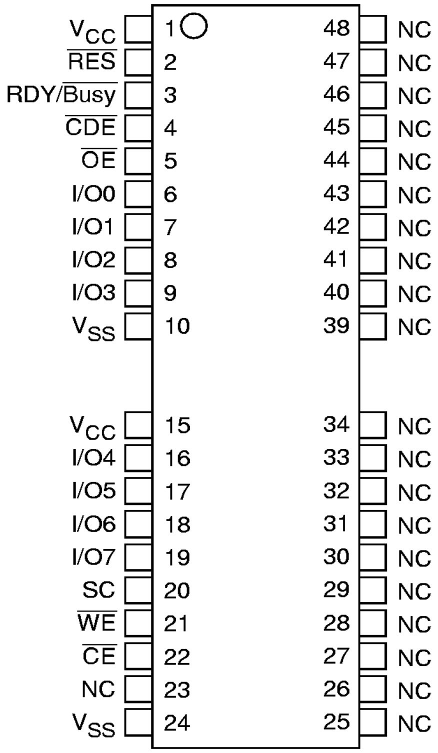
- Fast serial read access time:
  - — First access time: 5 µs (max)
  - — Serial access time: 50 ns (max)
- Low power dissipation:
  - — I_{CC} = 50 mA (max) (Read) (V_{CC} = 3.3 V)
  - — I_{CC} = 70 mA (max) (Read) (V_{CC} = 5 V)
  - — I_{CC} = 50 µA (max) (Standby) (V_{CC} = 3.3 V)
  - — I_{CC} = 100 µA (max) (Standby) (V_{CC} = 5 V)
  - — I_{CC} = 40 mA (max) (Erase/Program) (V_{CC} = 3.3 V)
  - — I_{CC} = 60 mA (max) (Erase/Program) (V_{CC} = 5 V)
  - — I_{CC} = 5 µA (max) (Deep standby) (V_{CC} = 3.3 V)
  - — I_{CC} = 10 µA (max) (Deep standby) (V_{CC} = 5 V)
- Error correction (more than 1 bit error correction per each sector read) is required for data reliability.

Ordering Information

Type No.	Available sector	Package
HN29W6411TT-50	More than 16,057 sectors	12.7 × 19.68 mm^2 0.8 mm pitch 48-pin plastic TSOP II (TTP-48/40D)

Pin Arrangement

HN29W6411TT Series



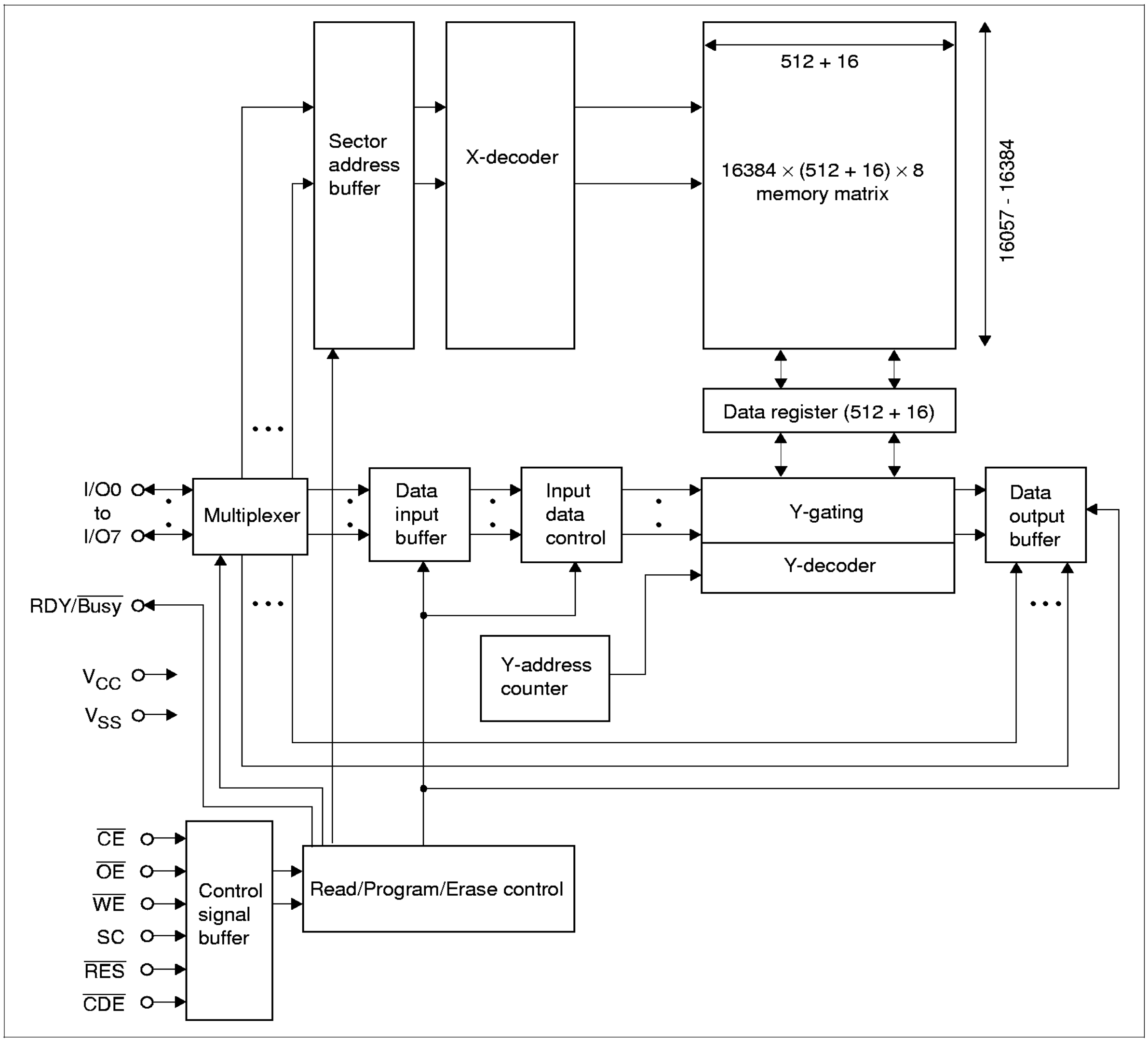
(Top view)

Pin Description

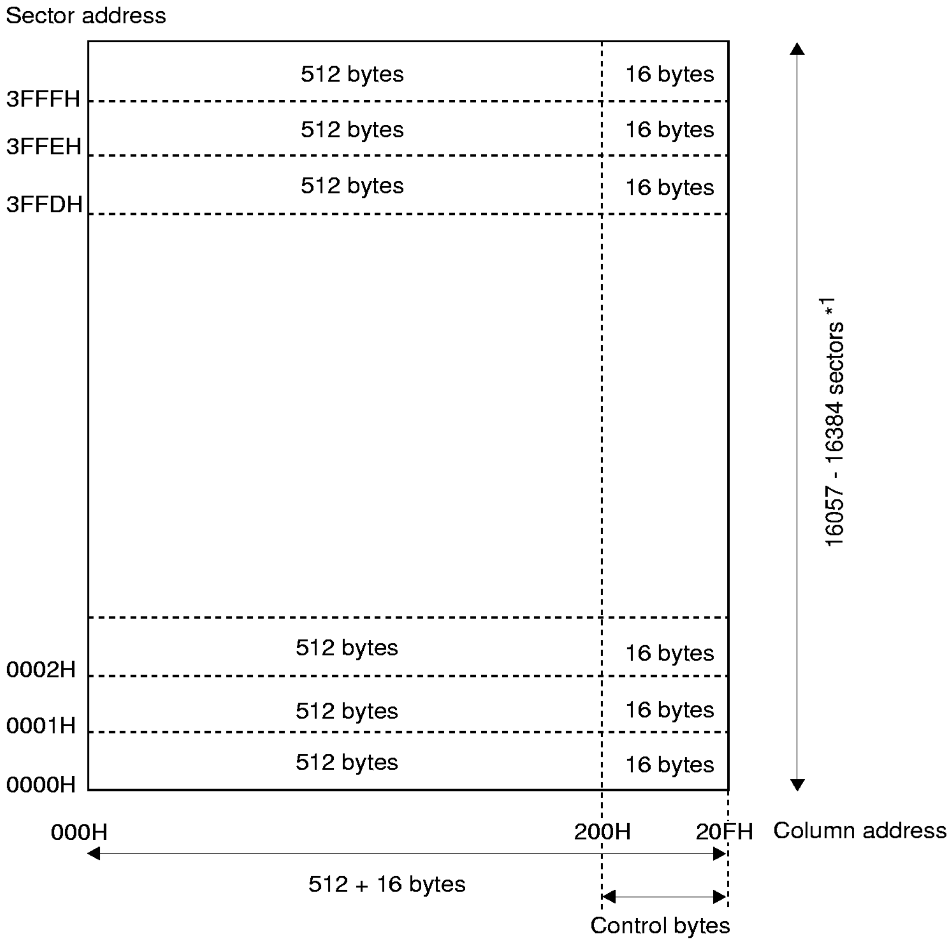
Pin name	Function
I/O0 to I/O7	Input/output
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable
$\overline{\text{WE}}$	Write enable
$\overline{\text{CDE}}$	Command data enable
V_{CC}*1	Power supply
V_{SS}*1	Ground
RDY/$\overline{\text{Busy}}$	Ready/$\overline{\text{Busy}}$
$\overline{\text{RES}}$	Reset
SC	Serial clock
NC	No connection

Note: 1. All V_{CC} and V_{SS} pins should be connected to a common power supply and a ground, respectively.

Block Diagram



Memory Map and Address



Address	Cycles	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
Sector address	SA (1): First cycle	A0	A1	A2	A3	A4	A5	A6	A7
	SA (2): Second cycle	A8	A9	A10	A11	A12	A13	×	×
Block address	BA (1): First cycle	×[*2]	×	×	A3	A4	A5	A6	A7
	BA (2): Second cycle	A8	A9	A10	A11	A12	A13	×	×

Notes: 1. Some failed sectors may exist in the device. The failed sectors can be recognized by reading the sector valid data written in a part of the column address 200 to 20F (The specific address is TBD). The sector valid data must be read and kept outside of the sector before the sector erase. When the sector is programmed, the sector valid data should be written back to the sector.

2. An × means "Don't care". The pin level can be set to either V_{IL} or V_{IH}, referred to DC characteristics.

Mode Selection

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	SC	$\overline{RES}$	$\overline{CDE}$	$R\overline{B}$[*3]	I/O0 to I/O7
Deep standby	×[*4]	×	×	×	V_{ILR}	×	V_{OH}	High-Z
Standby	V_{IH}	×	×	×	V_{IHR}	×	V_{OH}	High-Z
Output disable	V_{IL}	V_{IH}	V_{IH}	×	V_{IHR}	×	V_{OH}	High-Z
Status register read[*1]	V_{IL}	V_{IL}	V_{IH}	×	V_{IHR}	×	V_{OH}	Status register outputs
Command write[*2]	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IHR}	V_{IL}	V_{OH}	Din

Notes: 1. Default mode after the power on is the status register read mode (refer to status transition). From I/O0 to I/O7 pins output the status, when $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$ (conventional read operation condition).

2. Refer to the command definition. Data can be read, programmed and erased after commands are written in this mode.

3. The RDY/$\overline{\text{Busy}}$ bus should be pulled up to V_{CC} to maintain the V_{OH} level while the RDY/$\overline{\text{Busy}}$ pin outputs a high impedance.

4. An × means "Don't care". The pin level can be set to either V_{IL} or V_{IH} referred to DC characteristics.

Command Definition*1, 2

Command		Bus cycles	First bus cycle Operation mode*3	First bus cycle Data in	Second bus cycle Operation mode	Second bus cycle Data in	Second bus cycle Data out	Third bus cycle Operation mode*3	Third bus cycle Data in	Fourth bus cycle Operation mode	Fourth bus cycle Data in
Serial read (1)		3	Write	00H	Write	SA (1)*4		Write	SA (2)*4		
Serial read (2)		3	Write	F0H	Write	SA (1)*4		Write	SA (2)*4		
Read identifier codes		1	Write	90H	Read		ID*7, 8				
Auto erase	Single sector	4	Write	20H	Write	SA (1)*4		Write	SA (2)*4	Write	B0H*10
	Block	4	Write	7FH	Write	BA (1)*5		Write	BA (2)*5	Write	B0H*10
Auto program	Program (1)*6	4	Write	10H	Write	SA (1)*4		Write	SA (2)*4	Write	40H*10,11
	Program (2)*9	4	Write	1FH	Write	SA (1)*4		Write	SA (2)*4	Write	40H*10,11
	Program (3) (Control bytes)*6	4	Write	0FH	Write	SA (1)*4		Write	SA (2)*4	Write	40H*10,11
Erase verify		4	Write	A0H	Write	SA (1)*4		Write	SA (2)*4	Write	A0H
Reset		1	Write	FFH							
Read status register		1	Write	70H	Read		SRD*7				
Clear status register		1	Write	50H							

Notes:
1. Commands and sector address are latched at rising edge of $\overline{WE}$ pulses. Program data is latched at rising edge of SC pulses.
2. The chip is in the read status register mode when $\overline{RES}$ is set to V_{IHR} first time after the power up.
3. Refer to the command read and write mode in mode selection.
4. SA (1) = Sector address (A0 to A7), SA (2) = Sector address (A8 to A13).
5. BA (1) = Block address (A3 to A7), BA (2) = Block address (A8 to A13). Address inputs of A0 to A2 are not necessary.
6. By using program (1) and (3), data can additionally be programmed maximum 15 times for each sector before erase.
7. ID = Identifier code; Manufacturer code (07H), Device code (91H). SRD = Status register data.
8. The manufacturer identifier code is output when $\overline{CDE}$ is low and the device identifier code is output when $\overline{CDE}$ is high.
9. Before program (2) operations, data in the programmed sector must be erased.
10. No commands can be written during auto program and erase (when the RDY/$\overline{Busy}$ pin outputs a V_{OL}).
11. The fourth cycle of the auto program comes after the program data input is complete.

Mode Description

Read

Serial Read (1): Memory data D0 to D527 in the sector of address SA is sequentially read. The mode turns back to the status register read mode at any time when $\overline{\mathrm{CE}}$ is reset. Output data is not valid after the number of the SC pulse exceeds 528.

Serial Read (2): Memory data D512 to D527 in the sector of address SA is sequentially read. The mode turns back to the status register read mode at any time when $\overline{\mathrm{CE}}$ is reset. Output data is not valid after the number of the SC pulse exceeds 16.

Automatic Erase

Single Sector Erase: Memory data D0 to D527 in the sector of address SA is erased automatically by internal control circuits. After the sector erase starts, the erasure completion can be checked through the RDY/$\overline{\mathrm{Busy}}$ signal and status data polling. All the bits in the sector are "1" after the erase. The sector valid data stored in a part of memory data D512 to D527 must be read and kept outside of the sector before the sector erase.

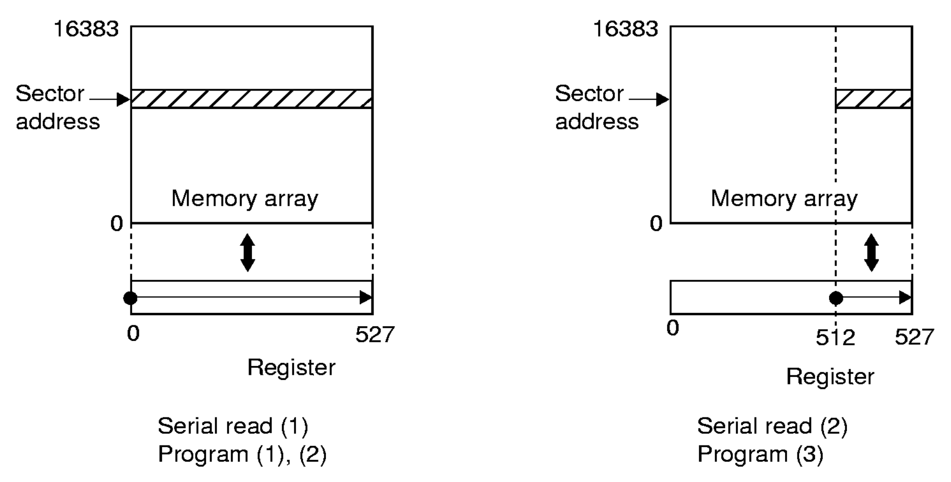
Block Erase: Memory data D0 to D527 in the 8 sectors of block address BA is erased automatically by internal control circuits. After the block erase starts, the erasure completion can be checked through the RDY/$\overline{\mathrm{Busy}}$ signal and status data polling. All the bits in the sectors are "1" after the erase. The sector valid data stored in a part of memory data D512 to D527 must be read and kept outside of the sectors before the sector erase.

Automatic Program

Program (1): Program data PD0 to PD527 is programmed into the sector of address SA automatically by internal control circuits. By using program (1), data can additionally be programmed 15 times for each sector before the following erase. After the programming starts, the program completion can be checked through the RDY/$\overline{\mathrm{Busy}}$ signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector valid data should be included in the program data PD512 to PD527.

Program (2): Program data PD0 to PD527 is programmed into the sector of address SA automatically by internal control circuits. After the programming starts, the program completion can be checked through the RDY/$\overline{\mathrm{Busy}}$ signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector must be erased before programming. The sector valid data should be included in the program data PD512 to PD527.

Program (3): Program data PD512 to PD527 is programmed into the sector of address SA automatically by internal control circuits. By using program (3), data can additionally be programmed 15 times for each sector before the following erase. After the programming starts, the program completion can be checked through the RDY/$\overline{\mathrm{Busy}}$ signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed.



Erase Verify

In the erase verify mode, I/O3 pin outputs a V_{OL} level if data in the selected sector are all "1". Otherwise, the I/O3 pin outputs a V_{OH} level .

Status Register Read

In the status register read mode , I/O pins output the same operation status as in the status data polling defined in the function description.

Identifier Read

The manufacturer and device identifier code can be read in the identifier read mode. The manufacturer and device identifier code is selected with $\overline{\text{CDE}}$ low and high, respectively.

Function Description

Status Register: The HN29W6411 outputs the operation status data as follows: I/O7 pin outputs a V_{OL} to indicate that the memory is in either erase or program operation. The level of I/O7 pin turns to a V_{OH} when the operation finishes. I/O5 and I/O4 pins output V_{OL}s to indicate that the erase and program operations complete in a finite time, respectively. If these pins output V_{OH}s, it indicates that these operations have timed out. To execute other erase and program operation, the status data must be cleared after a time out occurs. I/O3 pin outputs a V_{OL} to indicate that the result of the erase verify is a "pass". I/O6 pin outputs a V_{OH} if V_{CC} level is lower than a limit during the previous program and erase operation. If the erase verify fails, I/O3 pin outputs a V_{OH}. From I/O0 to I/O2 pins are reserved for future use. The pins output V_{OL}s and should be masked out during the status data read mode. The function of the status register is summarized in the following table.

I/O	Flag definition	Definition
I/O7	Ready/$\overline{\mathrm{Busy}}$	V_{OH} = Ready, V_{OL} = Busy
I/O6	V_{CC} check	V_{OH} = Fail, V_{OL} = Pass
I/O5	Erase check	V_{OH} = Fail, V_{OL} = Pass
I/O4	Program check	V_{OH} = Fail, V_{OL} = Pass
I/O3	Erase verify	V_{OH} = Fail (not erased), V_{OL} = Pass (erased)
I/O2	Reserved	Outputs a V_{OL} and should be masked out during the status data poling mode.
I/O1	Reserved	
I/O0	Reserved	

RDY/$\overline{\mathbf{Busy}}$: The RDY/$\overline{\mathrm{Busy}}$ signal also indicates the program/erase status of the flash memory. The RDY/$\overline{\mathrm{Busy}}$ signal is initially at a high impedance state. It turns to a V_{OL} level after the fourth command for either an erase or programming operation is input. After the erase or programming operation finishes, the RDY/$\overline{\mathrm{Busy}}$ signal turns back to the high impedance state.

$\overline{\mathbf{WE}}$: Commands and address are latched at the rising edge of $\overline{\mathrm{WE}}$.

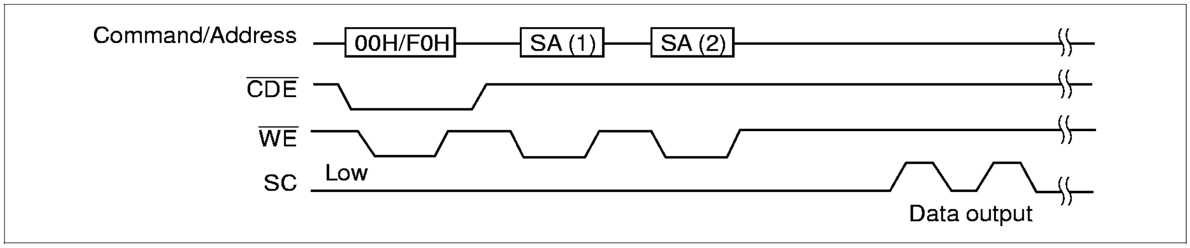
SC: Programming data is latched at the rising edge of SC.

$\overline{\mathbf{CDE}}$: Commands and data are latched when $\overline{\mathrm{CDE}}$ is V_{IL} and Address is latched when $\overline{\mathrm{CDE}}$ is V_{IH}.

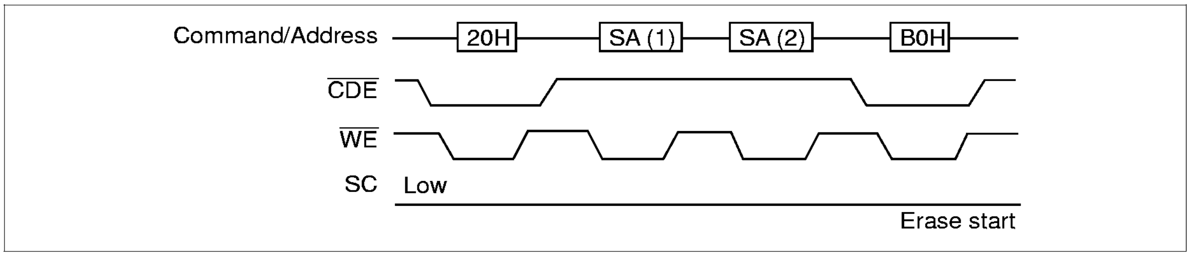
$\overline{\mathbf{RES}}$: $\overline{\mathrm{RES}}$ pin must be kept at the V_{ILR} (V_{SS} ± 0.2 V) level when V_{CC} is turned on and off. In this way, data in the memory is protected against unintentional erase and programming. $\overline{\mathrm{RES}}$ must be kept at the V_{IHR} (V_{CC} ± 0.2 V) level during any operations such as programming, erase and read.

Command/Address/Data Input Sequence

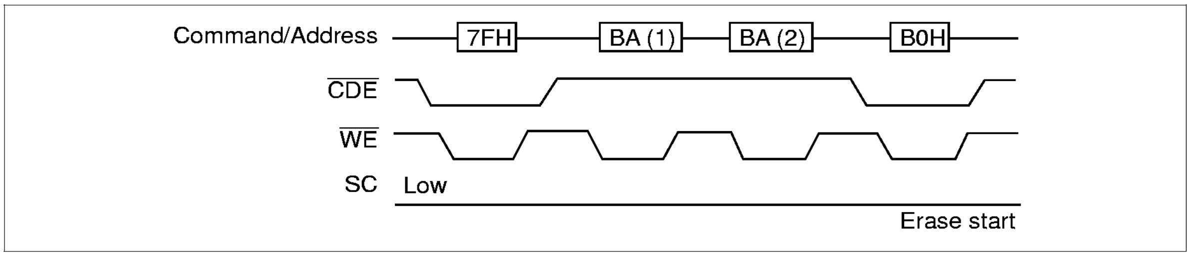
Serial Read (1) (2)



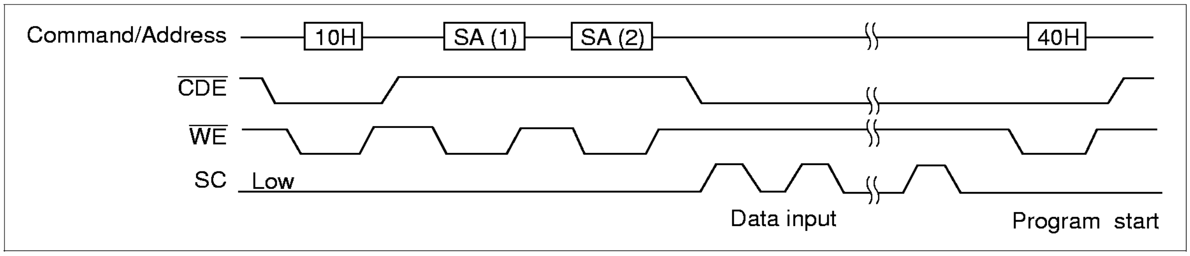
Single Sector Erase



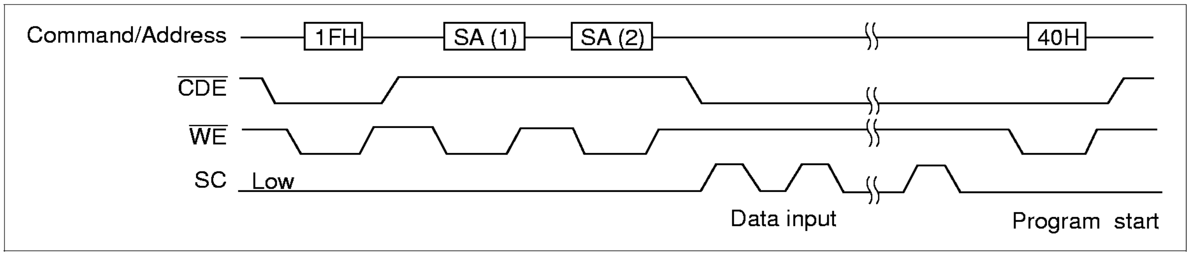
Block Erase



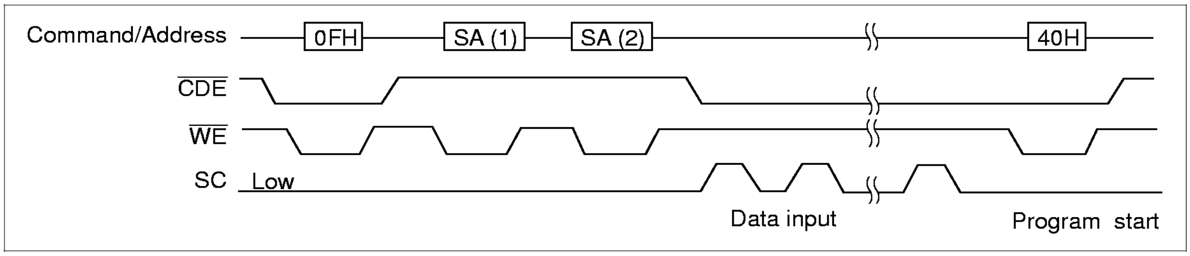
Program (1)



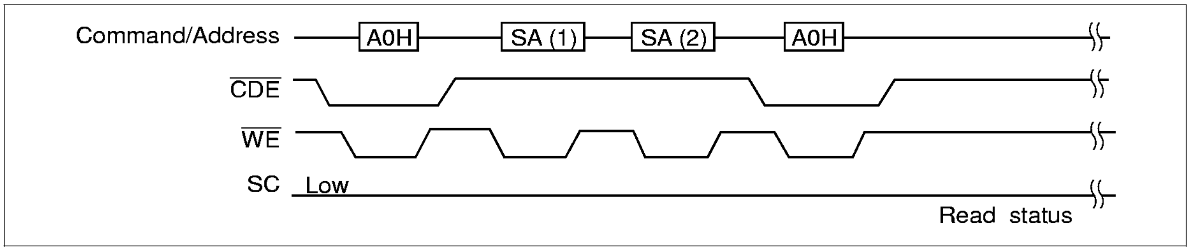
Program (2)



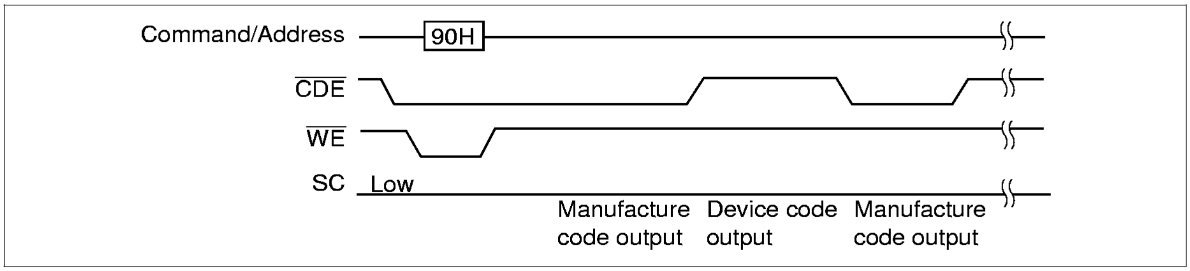
Program (3)



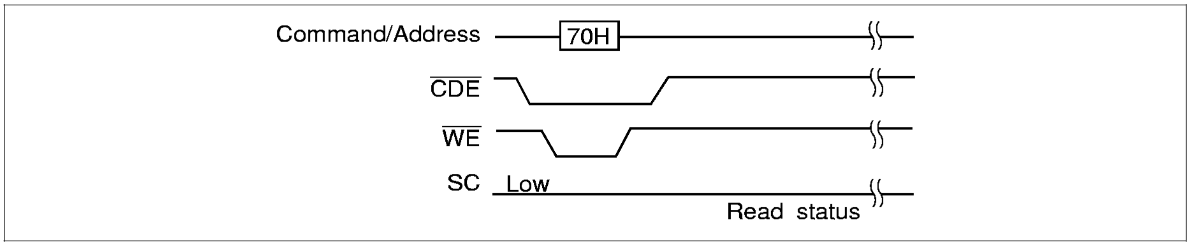
Erase Verify Mode



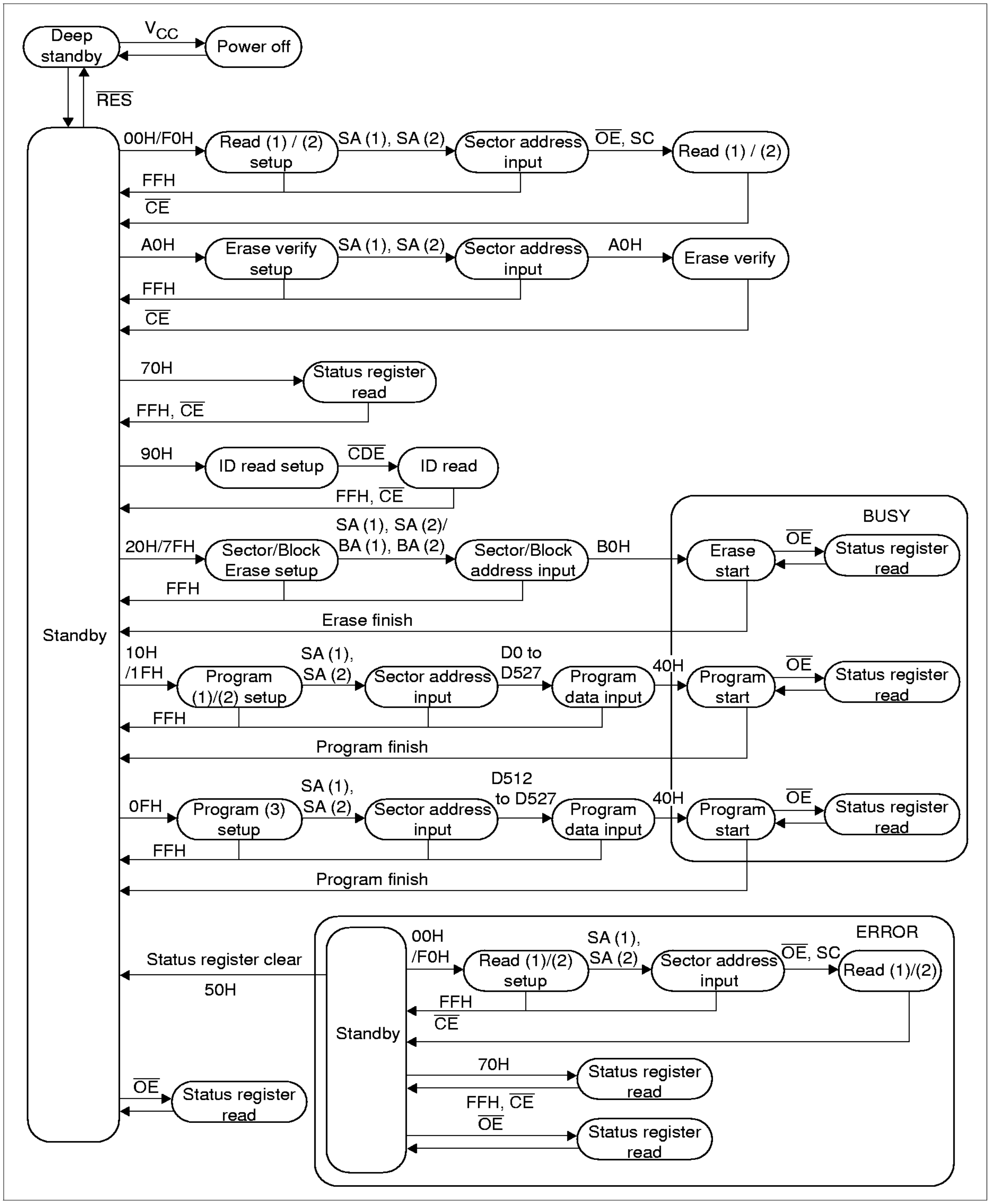
ID Read Mode



Status Register Read Mode



Status Transition



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
V_{CC} voltage	V_{CC}	–0.6 to +7	V	1
All input and output voltages	Vin, Vout	–0.6 to +7	V	1, 2
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–65 to +125	°C	3
Storage temperature under bias	Tbias	–10 to +80	°C	

Notes:
1. Relative to V_{SS}.
2. Vin, Vout = –2.0 V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	12	pF	Vout = 0 V

DC Characteristics-1 (V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	—	—	2	µA	Vout = V_{SS} to V_{CC}
Standby V_{CC} current	I_{SB1}	—	0.3	1	mA	$\overline{\text{CE}} = V_{IH}$
	I_{SB2}	—	30	50	µA	$\overline{\text{CE}} = V_{CC} \pm 0.2$ V, $\overline{\text{RES}} = V_{CC} \pm 0.2$V
Deep standby V_{CC} current	I_{SB3}	—	1	5	µA	$\overline{\text{RES}} = V_{SS} \pm 0.2$V
Operating V_{CC} current	I_{CC1}	—	—	25	mA	Iout = 0 mA, f = 0.2 MHz
	I_{CC2}	—	30	50	mA	Iout = 0 mA, f = 20 MHz
Operating V_{CC} current (Program)	I_{CC3}	—	—	40	mA	In programming
Operating V_{CC} current (Erase)	I_{CC4}	—	—	40	mA	In erase
Input voltage	V_{IL}	$-0.3^{*1,2}$	—	0.8	V	
	V_{IH}	2.0	—	$V_{CC} + 0.3^{*3}$	V	
Input voltage ($\overline{\text{RES}}$ pin)	V_{ILR}	–0.2	—	0.2	V	
	V_{IHR}	$V_{CC} - 0.2$	—	$V_{CC} + 0.2$	V	
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –2 mA

Notes:
1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns in the read operation. V_{IL} min = –2.0 V for pulse width ≤ 20 ns in the read operation.
2. V_{IL} min = –0.6 V for pulse width ≤ 20 ns in the erase/data programming operation.
3. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns. If V_{IH} is over the specified maximum value, the operations are not guaranteed.

DC Characteristics-2 (V_{CC} = 5 V ± 0.5 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	—	—	2	µA	Vout = V_{SS} to V_{CC}
Standby V_{CC} current	I_{SB2}	—	—	100	µA	$\overline{\text{CE}}$ = V_{CC} ± 0.2 V, $\overline{\text{RES}}$ = V_{CC} ± 0.2V
Deep standby V_{CC} current	I_{SB3}	—	—	10	µA	$\overline{\text{RES}}$ = V_{SS} ± 0.2V
Operating V_{CC} current	I_{CC1}	—	—	50	mA	Iout = 0 mA, f = 0.2 MHz
	I_{CC2}	—	—	70	mA	Iout = 0 mA, f = 20 MHz
Operating V_{CC} current (Program)	I_{CC3}	—	—	60	mA	In programming
Operating V_{CC} current (Erase)	I_{CC4}	—	—	60	mA	In erase
Input voltage	V_{IL}	$-0.3^{*1,2}$	—	0.2	V	
	V_{IH}	V_{CC} – 0.2	—	$V_{CC} + 0.3^{*3}$	V	
Input voltage ($\overline{\text{RES}}$ pin)	V_{ILR}	–0.2	—	0.2	V	
	V_{IHR}	V_{CC} – 0.2	—	V_{CC} + 0.2	V	
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –2 mA

Notes: 1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns in the read operation. V_{IL} min = –2.0 V for pulse width ≤ 20 ns in the read operation.

2. V_{IL} min = –0.6 V for pulse width ≤ 20 ns in the erase/data programming operation.

3. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns. If V_{IH} is over the specified maximum value, the operations are not guaranteed.

AC Characteristics (V_{CC} = 3.3 V ± 0.3 V/V_{CC} = 5 V ± 0.5 V, Ta = 0 to +70°C)

Test Conditions-1 (V_{CC} = 3.3 V ± 0.3 V)

- Input pulse levels: 0.4 V/2.4 V
- Input rise and fall time: ≤ 10 ns
- Output load: 1 TTL gate +50 pF (Including scope and jig.)
- Reference levels for measuring timing: 0.8 V, 1.8 V

Test Conditions-2 (V_{CC} = 5 V ± 0.5 V)

- Input pulse levels: 0.2 V/V_{CC} – 0.2 V
- Input rise and fall time: ≤ 10 ns
- Output load: 1 TTL gate +50 pF (Including scope and jig.)
- Reference levels for measuring timing: 0.8 V, 1.8 V

Power on and off, Serial Read Mode (1) and (2)

Parameter	Symbol	Min	Max	Unit	Test conditions	Note
Write cycle time	t_{CWC}	120	—	ns		
Serial clock cycle time	t_{SCC}	50	—	ns		
$\overline{\mathrm{CE}}$ setup time	t_{CES}	0	—	ns		
$\overline{\mathrm{CE}}$ hold time	t_{CEH}	0	—	ns		
Write pulse time	t_{WP}	60	—	ns	$\overline{\mathrm{CE}} = V_{IL}$, $\overline{\mathrm{OE}} = V_{IH}$	
Write pulse high time	t_{WPH}	40	—	ns		
Address setup time	t_{AS}	50	—	ns		
Address hold time	t_{AH}	10	—	ns		
Data setup time	t_{DS}	50	—	ns		
Data hold time	t_{DH}	10	—	ns		
SC to output delay	t_{SAC}	—	50	ns	$\overline{\mathrm{CE}} = \overline{\mathrm{OE}} = V_{IL}$, $\overline{\mathrm{WE}} = V_{IH}$	
$\overline{\mathrm{OE}}$ setup time for SC	t_{OES}	0	—	ns		
$\overline{\mathrm{OE}}$ low to output low-Z	t_{OEL}	0	—	ns		
$\overline{\mathrm{OE}}$ setup time before read	t_{OEPS}	40	—	ns		
SC to output hold	t_{SH}	15	—	ns	$\overline{\mathrm{CE}} = \overline{\mathrm{OE}} = V_{IL}$, $\overline{\mathrm{WE}} = V_{IH}$	
$\overline{\mathrm{OE}}$ high to output float	t_{DF}	—	40	ns	$\overline{\mathrm{CE}} = V_{IL}$, $\overline{\mathrm{WE}} = V_{IH}$	1
$\overline{\mathrm{WE}}$ to SC delay time	t_{WSD}	5	—	µs		
$\overline{\mathrm{RES}}$ to $\overline{\mathrm{CE}}$ setup time	t_{RP}	4	—	ms		
SC to $\overline{\mathrm{CE}}$, $\overline{\mathrm{OE}}$ hold time	t_{SCH}	50	—	ns		
SC pulse width	t_{SP}	20	—	ns		
SC pulse low time	t_{SPL}	20	—	ns		
SC setup time for $\overline{\mathrm{CE}}$	t_{SCS}	0	—	ns		
$\overline{\mathrm{CDE}}$ setup time for $\overline{\mathrm{WE}}$	t_{CDS}	0	—	ns		
$\overline{\mathrm{CDE}}$ hold time for $\overline{\mathrm{WE}}$	t_{CDH}	20	—	ns		
V_{CC} to $\overline{\mathrm{RES}}$ setup time	t_{RES}	1	—	µs	$\overline{\mathrm{CE}} = V_{IH}$	
$\overline{\mathrm{CE}}$ setup time for $\overline{\mathrm{RES}}$	t_{CESR}	1	—	µs		
RDY/$\overline{\mathrm{Busy}}$ undefined for V_{CC} off	t_{DFP}	0	—	ns		
$\overline{\mathrm{RES}}$ high to device ready	t_{BSY}	—	4	ms		
$\overline{\mathrm{CE}}$ pulse high time	t_{CPH}	200	—	ns		
$\overline{\mathrm{CE}}$, $\overline{\mathrm{WE}}$ setup time for $\overline{\mathrm{RES}}$	t_{CWRS}	0	—	ns		
$\overline{\mathrm{RES}}$ to $\overline{\mathrm{CE}}$, $\overline{\mathrm{WE}}$ hold time	t_{CWRH}	0	—	ns		

Note: 1. t_{DF} is a time after which the I/O pins become open.

Program, Erase and Erase Verify

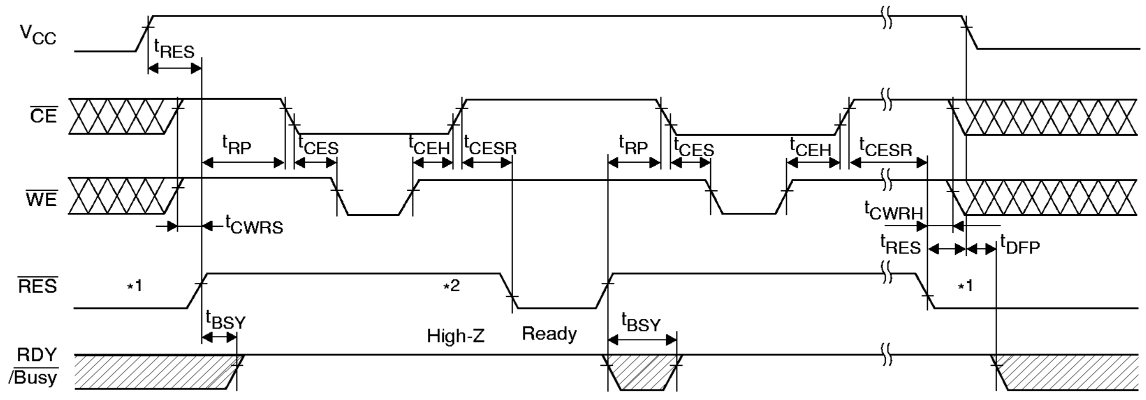
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Write cycle time	t_{CWC}	120	—	—	ns		
Serial clock cycle time	t_{SCC}	50	—	—	ns		
$\overline{\text{CE}}$ setup time	t_{CES}	0	—	—	ns		
$\overline{\text{CE}}$ hold time	t_{CEH}	0	—	—	ns		
Write pulse time	t_{WP}	60	—	—	ns	$\overline{\text{CE}} = V_{IL}$, $\overline{\text{OE}} = V_{IH}$	
Write pulse high time	t_{WPH}	40	—	—	ns		
Address setup time	t_{AS}	50	—	—	ns		
Address hold time	t_{AH}	10	—	—	ns		
Data setup time	t_{DS}	50	—	—	ns		
Data hold time	t_{DH}	10	—	—	ns		
$\overline{\text{OE}}$ setup time before command write	t_{OEWS}	0	—	—	ns		
$\overline{\text{OE}}$ setup time before read	t_{OEPS}	40	—	—	ns		
Time to device busy	t_{DB}	—	—	150	ns		
Auto erase time (Sector)	t_{ASE}	—	1	20	ms		
Auto erase time (Block)	t_{ABE}	—	1	20	ms		
Auto program time	t_{ASP}	—	1	20	ms		
$\overline{\text{CE}}$ pulse high time	t_{CPH}	200	—	—	ns		
Write cycle time for control byte program	t_{CWCC}	2.5	—	—	µs		
SC pulse width	t_{SP}	20	—	—	ns		
SC pulse low time	t_{SPL}	20	—	—	ns		
Data setup time for SC	t_{SDS}	0	—	—	ns		
Data hold time for SC	t_{SDH}	30	—	—	ns	$\overline{\text{CDE}} = V_{IL}$	
SC setup for $\overline{\text{WE}}$	t_{SW}	20	—	—	ns	$\overline{\text{CDE}} = V_{IL}$	
SC setup for $\overline{\text{CE}}$	t_{SCS}	0	—	—	ns		
SC hold time for $\overline{\text{WE}}$	t_{SCHW}	20	—	—	ns		
$\overline{\text{CE}}$ to output delay	t_{CE}	—	—	120	ns		
$\overline{\text{OE}}$ to output delay	t_{OE}	—	—	60	ns		
$\overline{\text{OE}}$ high to output float	t_{DF}	—	—	40	ns	$\overline{\text{CE}} = V_{IL}$, $\overline{\text{WE}} = V_{IH}$	1
$\overline{\text{RES}}$ to write setup time	t_{RP}	4	—	—	ms		

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
$\overline{\text{CDE}}$ setup time for $\overline{\text{WE}}$	t_{CDS}	0	—	—	ns		
$\overline{\text{CDE}}$ hold time for $\overline{\text{WE}}$	t_{CDH}	20	—	—	ns		
$\overline{\text{WE}}$ to erase verify	t_{OEV}	20	—	—	µs		
$\overline{\text{CDE}}$ setup time for SC	t_{CDSS}	100	—	—	ns		
Next cycle ready time	t_{RDY}	0	—	—	ns		
$\overline{\text{CDE}}$ to $\overline{\text{CE}}$, $\overline{\text{OE}}$ hold time	t_{CDCH}	50	—	—	ns		
$\overline{\text{CDE}}$ to output delay	t_{CDAC}	—	—	50	ns		
$\overline{\text{CDE}}$ to output invalid	t_{CDF}	0	—	—	ns		

Note: 1. t_{DF} is a time after which the I/O pins become open.

Timing Waveforms

Power on and off Sequence

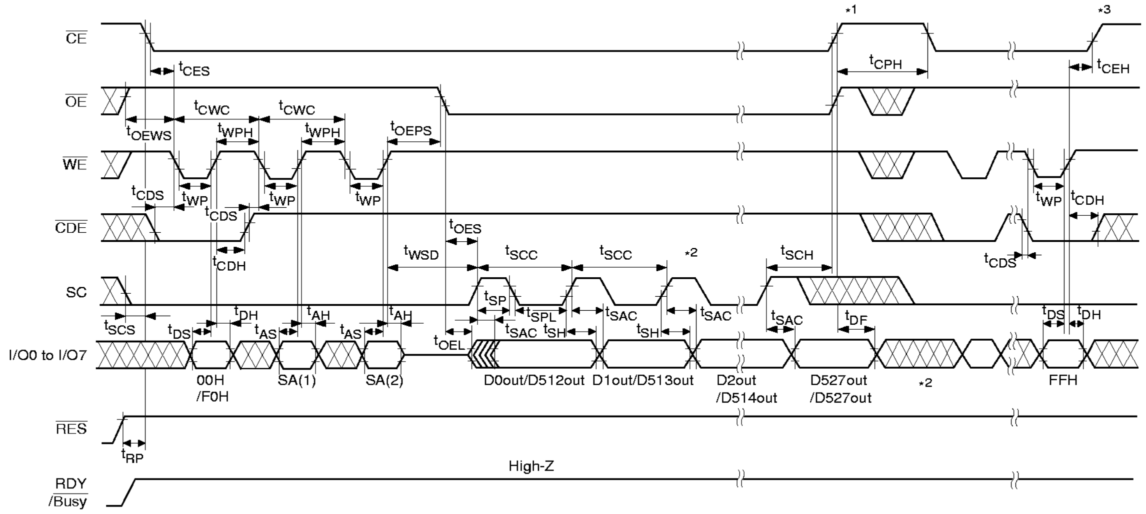


Notes: 1. $\overline{\text{RES}}$ must be kept at the V_{ILR} (V_{SS} ± 0.2 V) level referred to DC characteristics at the rising and falling edges of V_{CC} to guarantee data stored in the chip.

2. $\overline{\text{RES}}$ must be kept at the V_{IHR} (V_{CC} ± 0.2 V) level referred to DC characteristics while I/O7 outputs the V_{OL} level in the status data polling and RDY/$\overline{\text{Busy}}$ outputs the V_{OL} level.

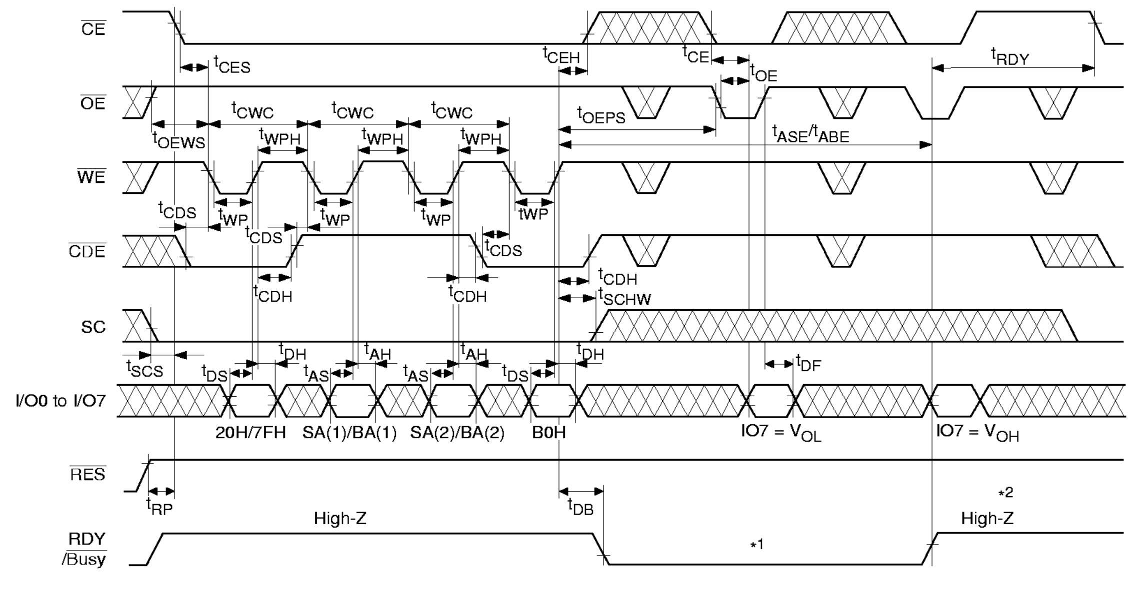
3. ▨ : Undefined

Serial Read (1) (2) Timing Waveform



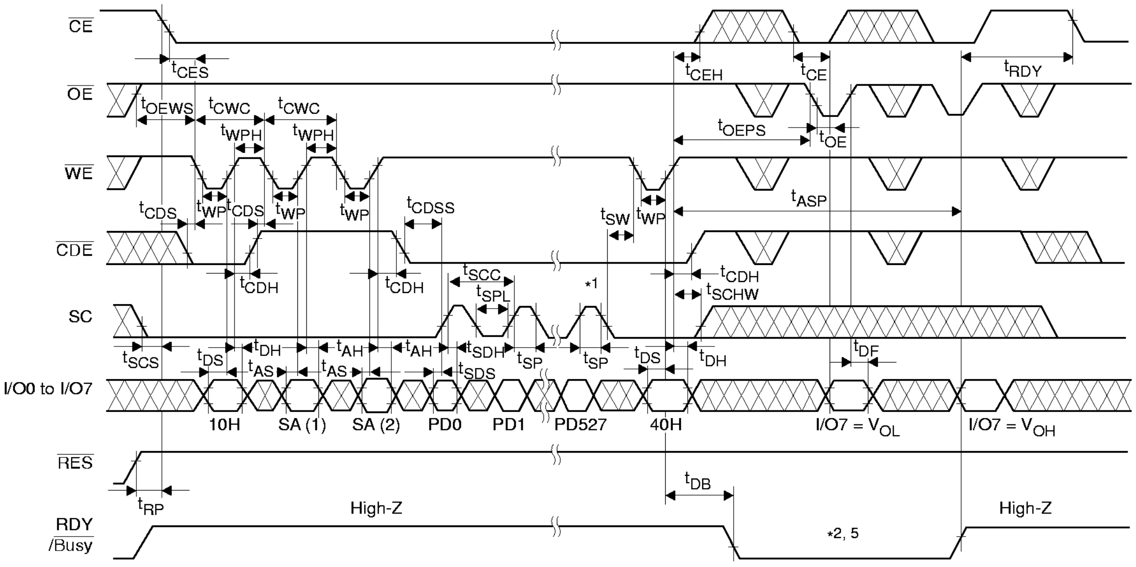
Notes:
1. The status returns to the standby at the rising edge of $\overline{\text{CE}}$.
2. Output data is not valid after the number of the SC pulse exceeds 528 and 16 in the serial read mode (1)and (2), respectively.
3. After any commands are written, the status can return to the standby after the command FFH is input and $\overline{\text{CE}}$ turns to the V_{IH} level.

Erase and Status Data Polling Timing Waveform (Sector Erase/Block Erase)



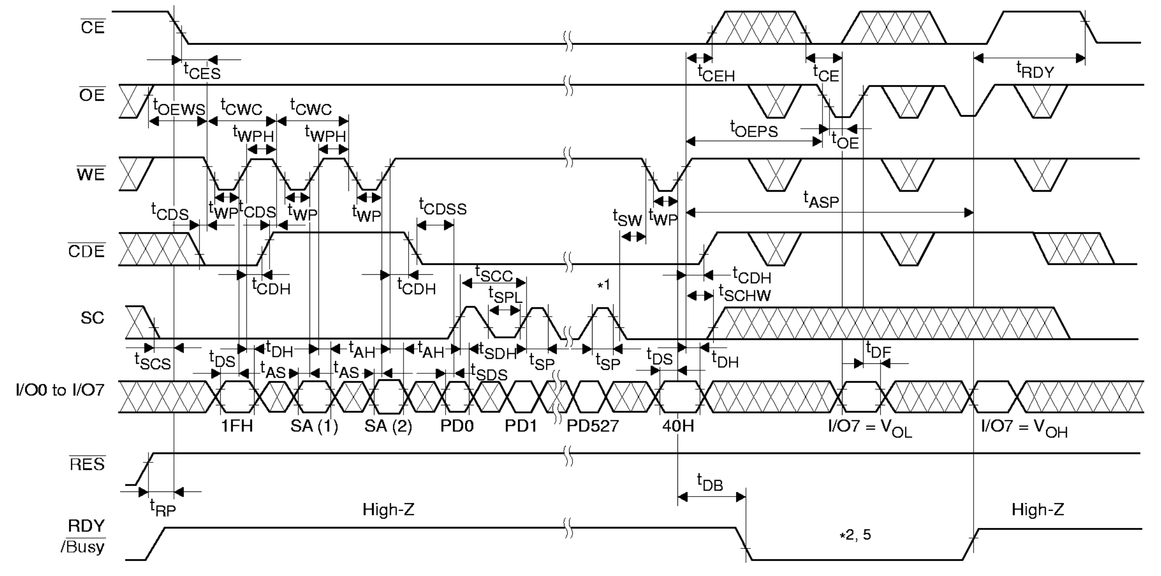
Notes:
1. Any commands,including reset command FFH, cannot be input while RDY/$\overline{\text{Busy}}$ outputs a V_{OL}.
2. The status returns to the standby status after RDY/$\overline{\text{Busy}}$ returns to High-Z.
3. When V_{CC} is lower than 3.0 V and the erase operation is not complete, V_{CC} fail flag turns to "1" and can be read out through I/O3 pin.

Program (1) and Status Data Polling Timing Waveform



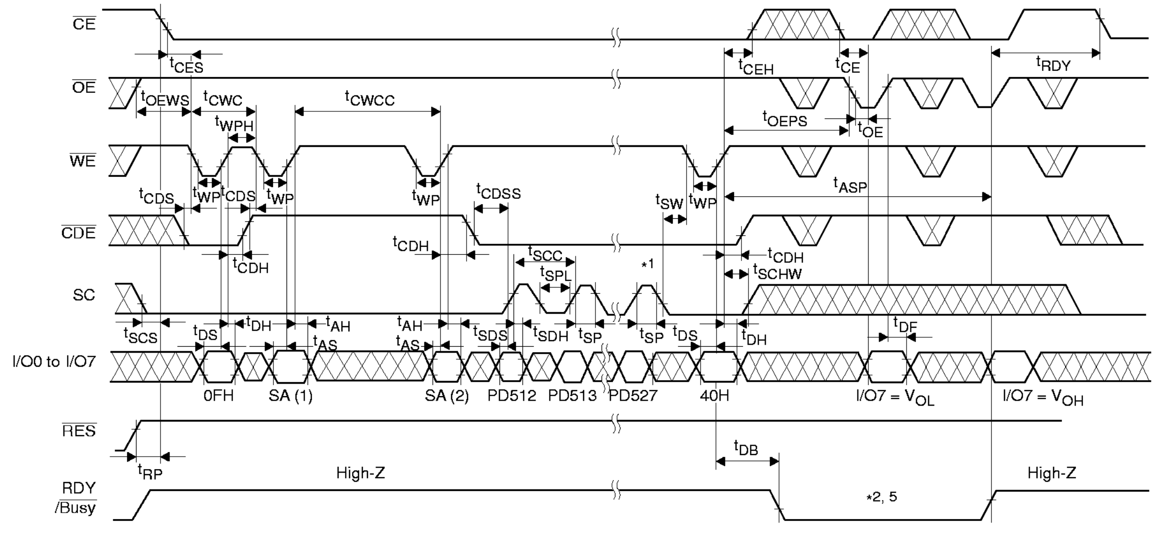
Notes:
1. The programming operation is not guranteed when the number of the SC pulse exceeds 528.
2. Any commands, including reset command FFH, cannot be input while RDY/$\overline{\text{Busy}}$ is V_{OL}.
3. The status returns to the standby status after RDY/$\overline{\text{Busy}}$ returns to High-Z.
4. By using program (1), data can be programmed additionally maximum 15 times for each sector before erase.
5. When V_{CC} is lower than 3.0 V and the erase operation is not complete, V_{CC} fail flag turns to "1" and can be read out through I/O6 pin.

Program (2) and Status Data Polling Timing Waveform



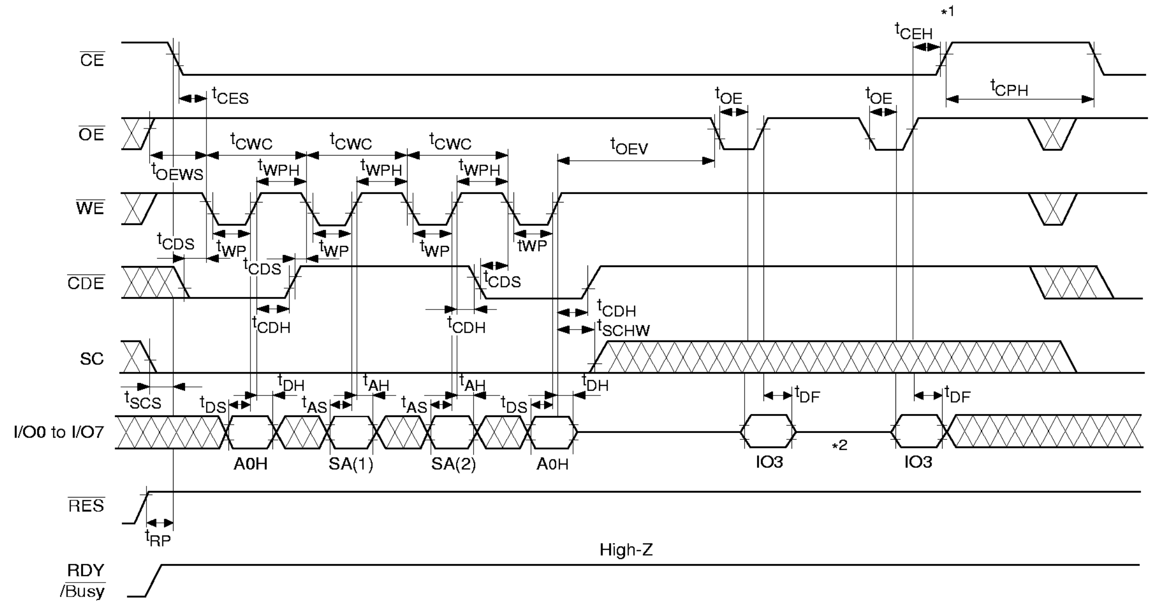
Notes:
1. The programming operation is not guranteed when the number of the SC pulse exceeds 528.
2. Any commands, including reset command FFH, cannot be input while RDY/$\overline{\text{Busy}}$ is V_{OL}.
3. The status returns to the standby status after RDY/$\overline{\text{Busy}}$ returns to High-Z.
4. By using program (2), the programmed data of each sector must be erased before programming next data.
5. When V_{CC} is lower than 3.0 V and the erase operation is not complete, V_{CC} fail flag turns to "1" and can be read out through I/O6 pin.

Program (3) and Status Data Polling Timing Waveform



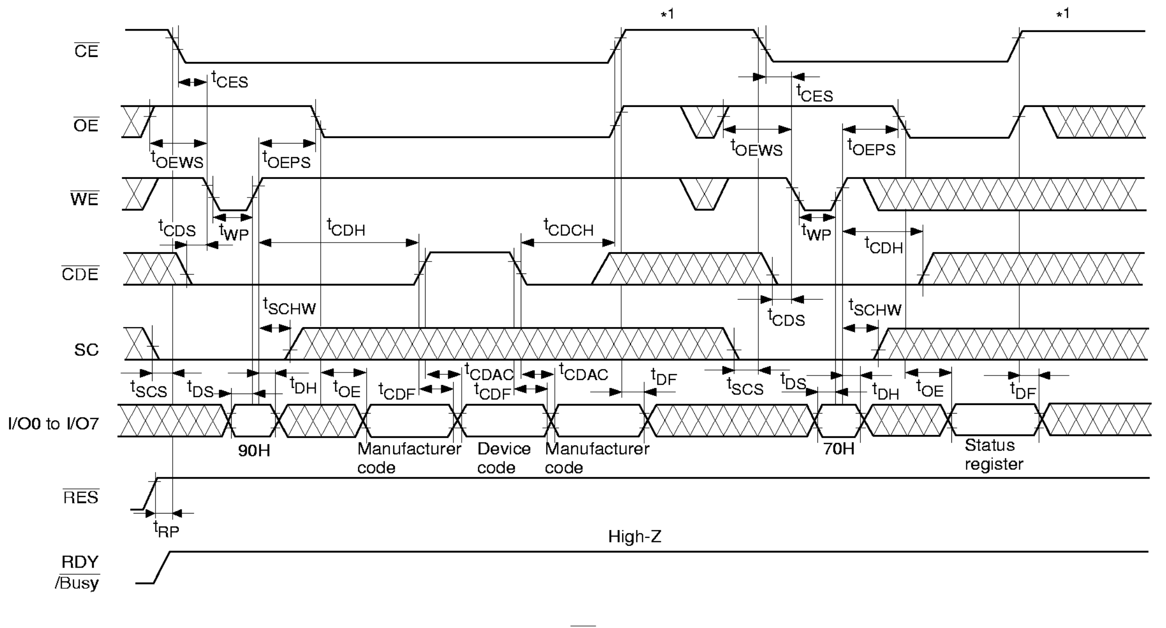
Notes: 1. The programming operation is not guranteed when the number of the SC pulse exceeds 16.
2. Any commands, including reset command FFH, cannot be input while RDY/$\overline{\text{Busy}}$ is V_{OL}.
3. The status returns to the standby status after RDY/$\overline{\text{Busy}}$ returns to High-Z.
4. By using program (3), data can be programmed additionally maximum 15 times for each sector before erase.
5. When V_{CC} is lower than 3.0 V and the erase operation is not complete, V_{CC} fail flag turns to "1" and can be read out through I/O6 pin.

Erase Verify Timing Waveform



Notes: 1. The status returns to the standby at the rising edge of $\overline{CE}$.
2. V_{OH}: Not erased, V_{OL}: Erased.

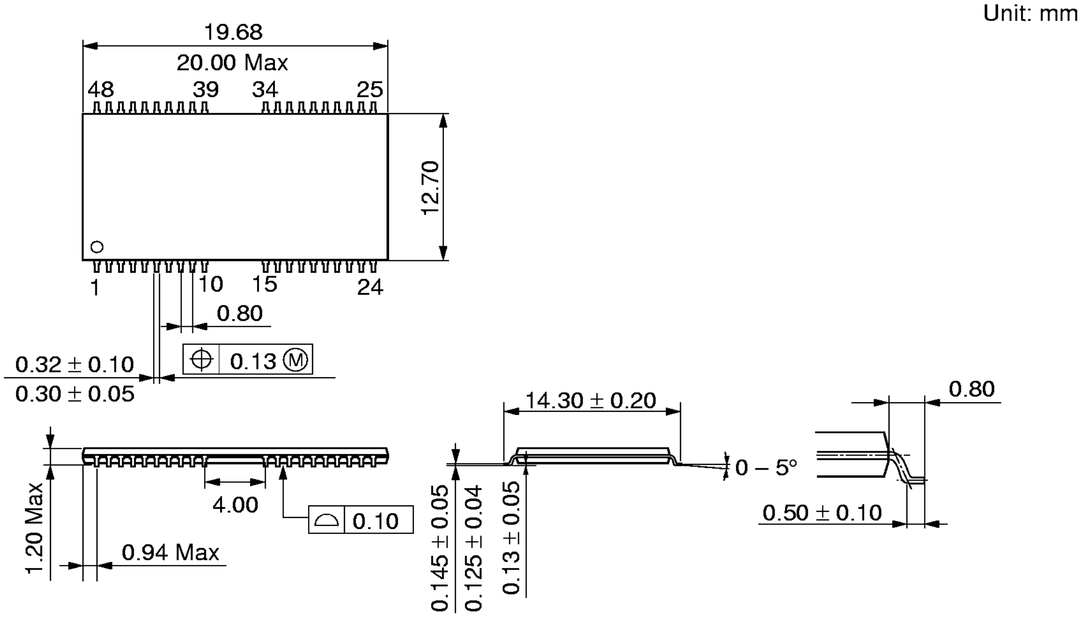
ID and Status Register Read Timing Waveform



Note: 1. The status returns to the standby at the rising edge of $\overline{\text{CE}}$.

Package Dimensions

HN29W6411TT Series (TTP-48/40D)



Dimension including the plating thickness

Base material dimension

Hitachi Code	TTP-48/40D
JEDEC Code	—
EIAJ Code	—
Weight (reference value)	0.60 g

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Sep. 20, 1996	Initial issue	H. Uchida	Y. Nakamura
2.0	Jan. 20, 1997	Addition of specifications for V_{CC} = 5 V Features: Addition of Automatic erase Absolute Maximum Ratings V_{CC}, Vin, Vout: –0.6 to +4.6 V to –0.6 to +7 V	H. Uchida	Y. Nakamura
3.0	Jul. 3, 1997	Change of figure for Status Transition AC Characteristics t_{OEL} max: 40 ns to — t_{DF} min: 0 ns to — t_{CDF} max: 100 ns to — Deletion of note2 for Power on and off, Serial Read Mode (1) and (2) Timing Waveforms Addition of note3 for Erase and Status Data Polling Timing Waveform (Sector Erase/Block Erase) Change of Package Dimension (TTP-48/40D)		