Integrated Device Technology, Inc.

16K x 32 CMOS STATIC RAM MODULE

IDT7MC4032

FEATURES:

- High density separate I/0, 512K CMOS static RAM module
- Fast access time: 15ns (max.)
- Available in low profile 88-pin sidebraze ceramic dual SIP (Dual Single In-line Package)
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- High impedance outputs during write mode
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible
- Multiple GND pins for maximum noise immunity

DESCRIPTION:

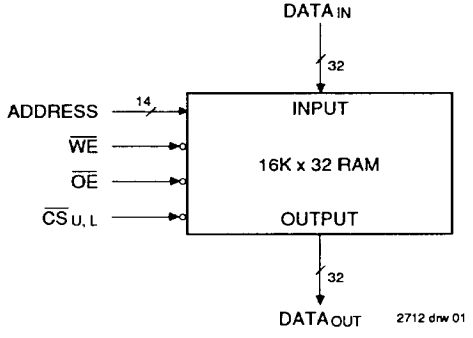
The IDT7MC4032 is a 16K x 32 static RAM module with separate I/0 constructed on a co-fired ceramic substrate using eight IDT71982 16K x 4 static RAMs in leadless chip carriers. Extremely fast speeds can be achieved due to the use of 64K static RAMs Fabricated in IDT's High-performance, high-reliability CEMOS™ technology. The IDT7MC4032 is available with access time as fast as 15ns with minimal power consumption.

The 7MC family of ceramic DSIPs offers the optimum in packing density and profile height. The IDT7MC4032 is packaged in a 88-pin ceramic dual SIP. The dual row configuration allow 88 pins to be placed on a package less than 4.5 inches long and .27 inches wide. At only 520 mils high, this low profile package is ideal for systems with minimum board spacing. Extremely high packing density can also be achieved allowing four IDT7MC4032 modules to be stacked per inch of board space.

All inputs and outputs of the IDT7MC4032 are TTL-compatible and operate from a single 5V power supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured on compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited for applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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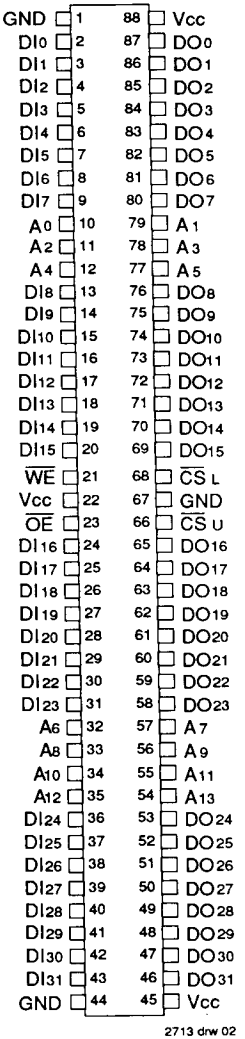
PIN CONFIGURATION[1]



2713 drw 02

DSIP
TOP VIEW

NOTE:
1. For module dimension, please refer to module drawing M43 in the packaging section.

PIN NAMES

A_0–A_{13}	Addresses
DI_0–DI_{31}	Data Input
DO_0–DO_{31}	Data Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}_L$	Chip Select (Lower)
$\overline{CS}_U$	Chip Select (Upper)
Vcc	Power
GND	Ground

2712 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	HighZ	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	High Z	Active
Read	L	H	H	High Z	Active

2712 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2712 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	15	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	80	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

2712 tbl 04

NOTE:
1. This parameter is guaranteed by design, but not tested.

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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

2712 tbl 05

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C + 125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2712 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V

2712 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	IDT7MC4032 15, 20ns Max.		IDT7MC4032 25ns Max.		IDT7MC4032 30, 40, 50ns Max.		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Current	f = 0, $\overline{CS} \le V_{IL}$, V_{CC} = Max., Output Open	960	—	960	1000	800	800	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \le V_{IL}$, f = f_{MAX}, Output Open	1200	—	1200	1200	1000	1120	mA
I_{SB}	Standby Supply Current	$\overline{CS} \ge V_{IH}$, V_{CC} = Max., f = f_{MAX}, Ouputs Open	600	—	480	480	400	440	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \ge V_{CC}$ -0.2V, $V_{IN} \ge V_{CC}$ -0.2V or ≤ 0.2V	200	—	160	160	120	160	mA

2712 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2712 tbl 10

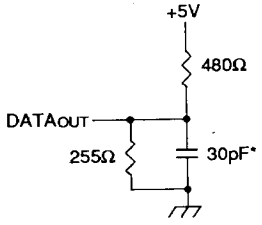

Figure 1. Output Load

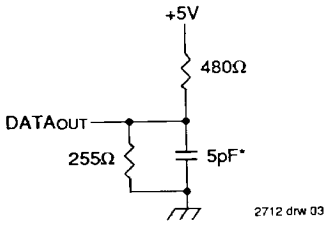

Figure 2. Output Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%, TA = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameters	7MC4032S15 Com'l Only		7MC4032S20 Com'l Only		7MC4032S25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	15	—	20	—	25	—	ns
tAA	Address Access Time	—	15	—	20	—	25	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	ns
tCLZ(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	15	—	15	ns
tOLZ(1)	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
tCHZ(1)	Chip Deselect to Output in High Z	—	7	—	8	—	10	ns
tOHZ(1)	Output Disable to Output in High Z	—	7	—	8	—	15	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	ns
tPU(1)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
tPD(1)	Chip Deselect to Power Down Time	—	15	—	20	—	25	ns
Write Cycle								
tWC	Write Cycle Time	14	—	17	—	20	—	ns
tCW	Chip Selection to End of Write	14	—	17	—	20	—	ns
tAW	Address Valid to End of Write	14	—	17	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14	—	17	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tWHZ(1)	Write Enable to Ouput in High Z	—	5	—	7	—	7	ns
tDW	Data to Write Time Overlap	8	—	10	—	13	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	ns
tOW(1)	Output Active from End of Write	5	—	5	—	5	—	ns

2712 tbl 08

NOTE:
1. This parameter is guaranteed by design, but not tested.

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AC ELECTRICAL CHARACTERISTICS (Continued)

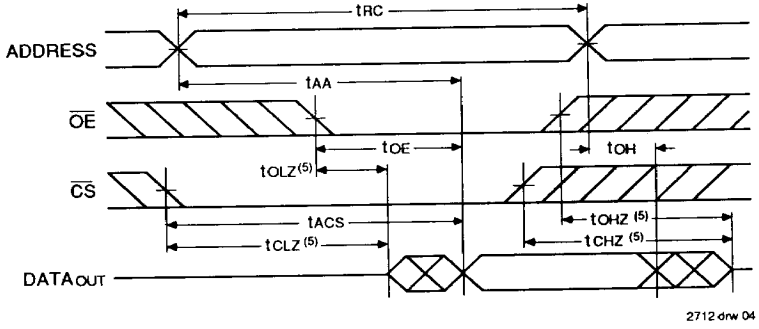
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameters	7MC4032S30		7MC4032S40		7MC4032S50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	30	—	40	—	50	—	ns
t_{AA}	Address Access Time	—	30	—	40	—	50	ns
t_{ACS}	Chip Select Access Time	—	30	—	40	—	50	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	20	—	22	—	30	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	13	—	17	—	18	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	17	—	17	—	18	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}(1)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power Down Time	—	30	—	40	—	50	ns
Write Cycle								
t_{WC}	Write Cycle Time	25	—	35	—	45	—	ns
t_{CW}	Chip Selection to End of Write	25	—	28	—	38	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	2	—	2	—	ns
t_{WP}	Write Pulse Width	25	—	28	—	38	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Ouput in High Z	—	10	—	12	—	17	ns
t_{DW}	Data to Write Time Overlap	15	—	17	—	23	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End of Write	5	—	5	—	5	—	ns

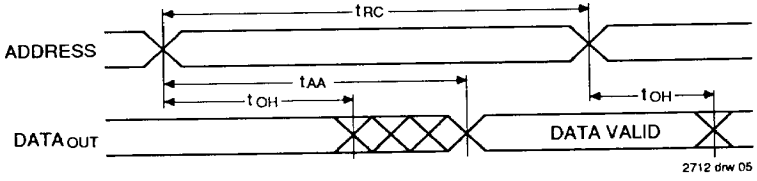
NOTE:
1. This parameter is guaranteed by design, but not tested.

2712 tbl 09

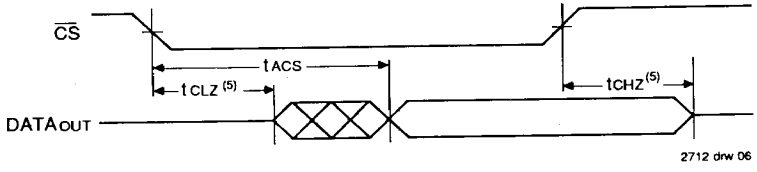
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±500mV from steady state. This parameter is guaranteed by design but not tested.

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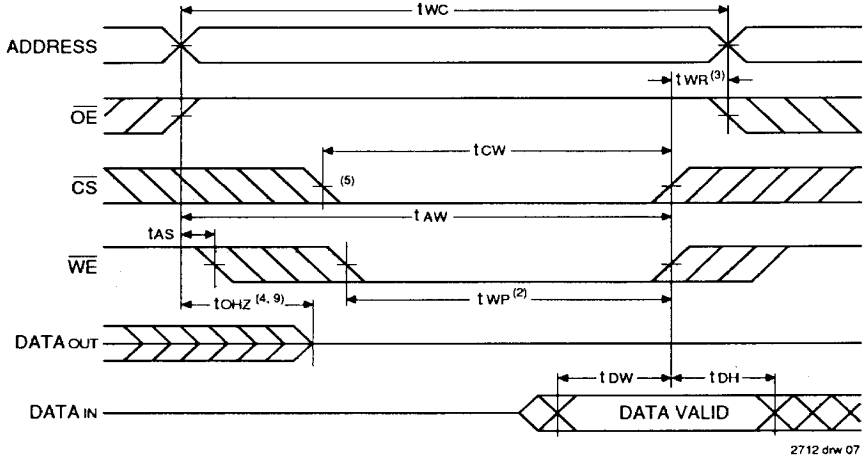
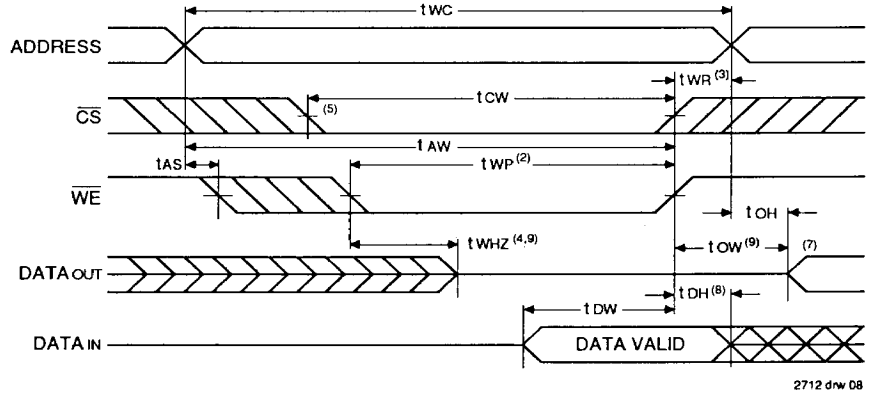
TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)

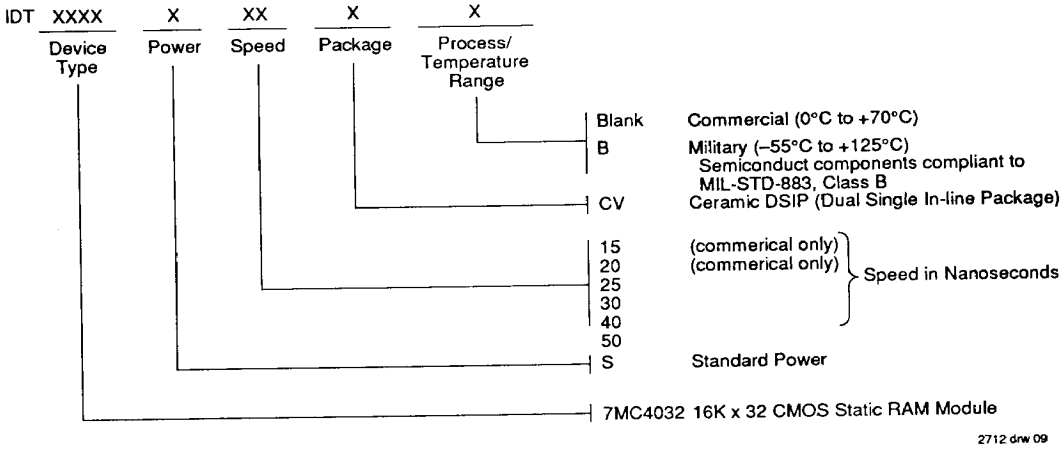


TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CS CONTROLLED TIMING)(1, 6)



NOTES:
1. WE or CS must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low CS.
3. tWR is measured from the earlier of CS or WE going High to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CS Low transition occurs simultaneously with or after the WE Low transitions or after the WE transition, the outputs remain in a high impedance state.
6. OE is continuously low (OE = VIL).
7. DATAOUT is the same phase of write data of this write cycle.
8. If CS is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase must not be applied to them.
9. Transition is measured ±500mV from steady state. This parameter is graranteed by design, but not tested.

ORDERING INFORMATION



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