M37702M4AXXXFP, M37702M4BXXXFP

M37702M4-XXXFP and
M37702S4FP are respectively
unified into M37702M4AXXXFP
and M37702S4AFP.

M37702S4AFP, M37702S4BFP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37702M4AXXXFP is a single-chip microcomputer designed with high-performance CMOS silicon gate technology. This is housed in a 80-pin plastic molded QFP. This single-chip microcomputer has a large 16M bytes address space, three instruction queue buffers, and two data buffers for high-speed instruction execution. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. This microcomputer is suitable for office, business and industrial equipment controller that require high-speed processing of large data.

The differences between M37702M4AXXXFP, M37702M4BXXXFP, M37702S4AFP and M37702S4BFP are the ROM size and the external clock input frequency as shown below. Therefore, the following descriptions will be for the M37702M4AXXXFP unless otherwise noted.

Type name	ROM size	External clock input frequency
M37702M4AXXXFP	32K bytes	16MHz
M37702M4BXXXFP	32K bytes	25MHz
M37702S4AFP	External	16MHz
M37702S4BFP	External	25MHz

The M37702M4AXXXFP has the same functions as the M37702M2AXXXFP except for the memory size.

FEATURES

● Number of basic instructions ·····························103
● Memory size   ROM ·····························32K bytes
            RAM····························· 2048 bytes
● Instruction execution time
    M37702M4AXXXFP, M37702S4AFP
    (The fastest instruction at 16 MHz frequency)······ 250ns
    M37702M4BXXXFP, M37702S4BFP
    (The fastest instruction at 25 MHz frequency)······ 160ns
● Single power supply ·····························5V±10%
● Low power dissipation (at 16 MHz frequency)
    ·· 60mW (Typ.)
● Interrupts ·····························19 types 7 levels
● Multiple function 16-bit timer ·····························5+3
● UART (may also be synchronous) ·····························2
● 8-bit A-D converter ·····························8-channel inputs
● 12-bit watchdog timer
● Programmable input/output
    (ports P0, P1, P2, P3, P4, P5, P6, P7, P8) ··············· 68

APPLICATION

Control devices for office equipment such as copiers, printers, typewriters, facsimiles, word processors and personal computers

Control devices for industrial equipment such as ME, NC, communication, and measuring instruments

NOTE

Refer to "Chapter 5 PRECAUTIONS" when using this microcomputer.

The M37702M4AXXXFP and M37702S4AFP satisfy the timing requirements and the switching characteristics of the former M37702M4-XXXFP and M37702S4FP.
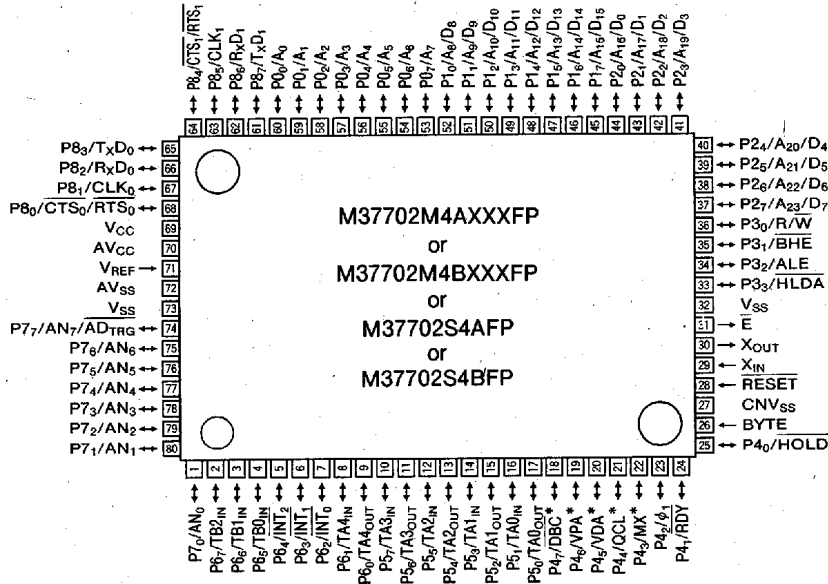
M37702M4AXXXFP, M37702M4BXXXFP
M37702S4AFP, M37702S4BFP

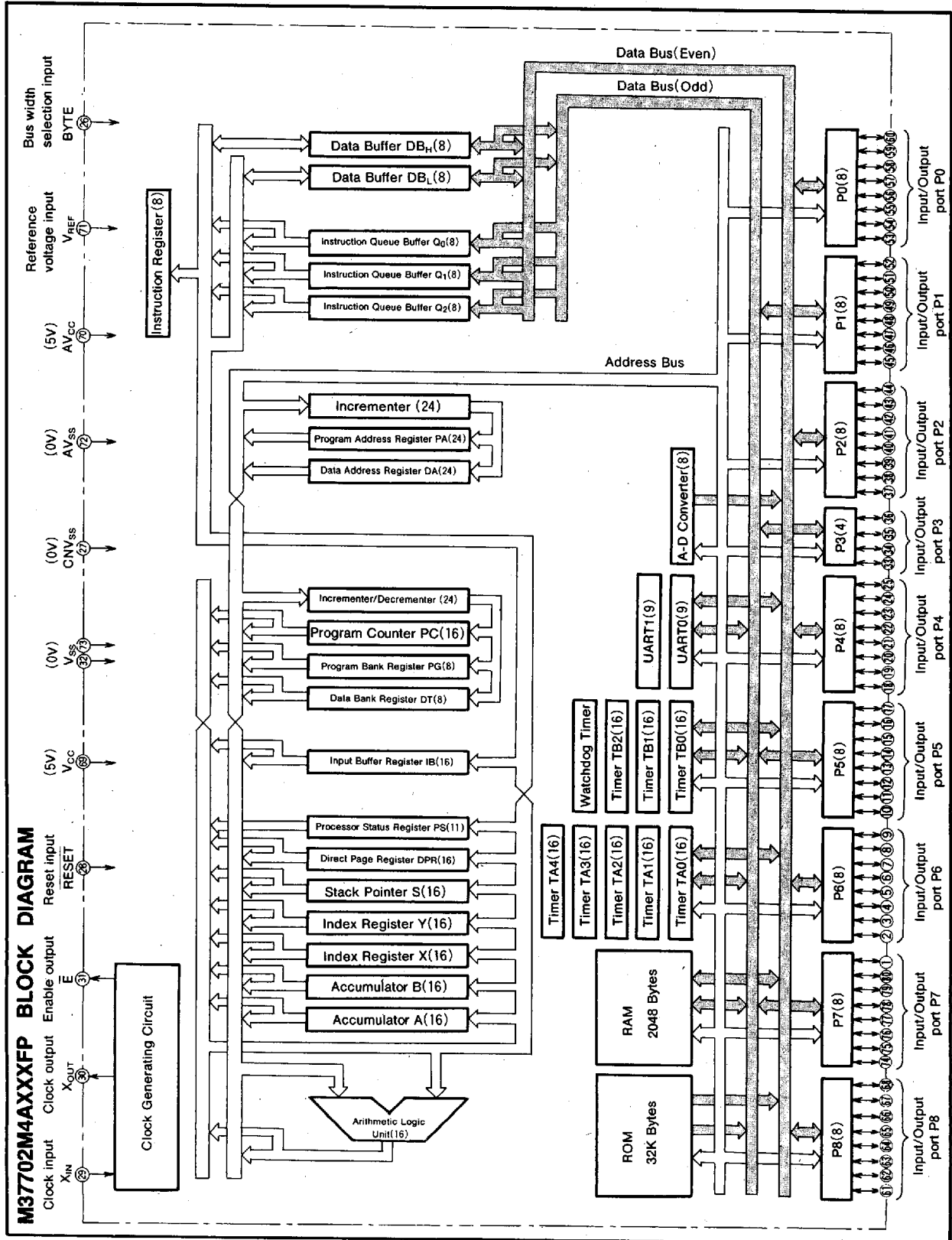## SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

PIN CONFIGURATION (TOP VIEW)

Top pins (left to right):
P8$_4$/CTS$_1$/RTS$_1$, P8$_5$/CLK$_1$, P8$_6$/RxD$_1$, P8$_7$/TxD$_1$, P0$_0$/A$_0$, P0$_1$/A$_1$, P0$_2$/A$_2$, P0$_3$/A$_3$, P0$_4$/A$_4$, P0$_5$/A$_5$, P0$_6$/A$_6$, P0$_7$/A$_7$, P1$_0$/A$_8$/D$_8$, P1$_1$/A$_9$/D$_9$, P1$_2$/A$_{10}$/D$_{10}$, P1$_3$/A$_{11}$/D$_{11}$, P1$_4$/A$_{12}$/D$_{12}$, P1$_5$/A$_{13}$/D$_{13}$, P1$_6$/A$_{14}$/D$_{14}$, P1$_7$/A$_{15}$/D$_{15}$, P2$_0$/A$_{16}$/D$_0$, P2$_1$/A$_{17}$/D$_1$, P2$_2$/A$_{18}$/D$_2$, P2$_3$/A$_{19}$/D$_3$

Left pins (top to bottom):
- 65 P8$_3$/TxD$_0$
- 66 P8$_2$/RxD$_0$
- 67 P8$_1$/CLK$_0$
- 68 P8$_0$/CTS$_0$/RTS$_0$
- 69 V$_{CC}$
- 70 AV$_{CC}$
- 71 V$_{REF}$
- 72 AV$_{SS}$
- 73 V$_{SS}$
- 74 P7$_7$/AN$_7$/AD$_{TRG}$
- 75 P7$_6$/AN$_6$
- 76 P7$_5$/AN$_5$
- 77 P7$_4$/AN$_4$
- 78 P7$_3$/AN$_3$
- 79 P7$_2$/AN$_2$
- 80 P7$_1$/AN$_1$

Right pins (top to bottom):
- 40 P2$_4$/A$_{20}$/D$_4$
- 39 P2$_5$/A$_{21}$/D$_5$
- 38 P2$_6$/A$_{22}$/D$_6$
- 37 P2$_7$/A$_{23}$/D$_7$
- 36 P3$_0$/R/W
- 35 P3$_1$/BHE
- 34 P3$_2$/ALE
- 33 P3$_3$/HLDA
- 32 V$_{SS}$
- 31 E
- 30 X$_{OUT}$
- 29 X$_{IN}$
- 28 RESET
- 27 CNV$_{SS}$
- 26 BYTE
- 25 P4$_0$/HOLD

Center label:
M37702M4AXXXFP
or
M37702M4BXXXFP
or
M37702S4AFP
or
M37702S4BFP

Bottom pins (left to right, 1–24):
P7$_0$/AN$_0$, P6$_7$/TB2$_{IN}$, P6$_6$/TB1$_{IN}$, P6$_5$/TB0$_{IN}$, P6$_4$/INT$_2$, P6$_3$/INT$_1$, P6$_2$/INT$_0$, P6$_1$/TA4$_{IN}$, P6$_0$/TA4$_{OUT}$, P5$_7$/TA3$_{IN}$, P5$_6$/TA3$_{OUT}$, P5$_5$/TA2$_{IN}$, P5$_4$/TA2$_{OUT}$, P5$_3$/TA1$_{IN}$, P5$_2$/TA1$_{OUT}$, P5$_1$/TA0$_{IN}$, P5$_0$/TA0$_{OUT}$, P4$_7$/DBC*, P4$_6$/VPA*, P4$_5$/VDA*, P4$_4$/QCL*, P4$_3$/MX*, P4$_2$/ϕ_1, P4$_1$/RDY

Outline 80P6N-A

*: Used in the evaluation chip mode only

MITSUBISHI ELECTRIC

M37702M4AXXXFP BLOCK DIAGRAM

M37702M4AXXXFP,M37702M4BXXXFP
M37702S4AFP,M37702S4BFP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37702M4AXXXFP

Parameter		Functions
Number of basic instructions		103
Instruction execution time	M37702M4AXXXFP, M37702S4AFP	250ns (the fastest instruction at external clock 16MHz frequency)
	M37702M4BXXXFP, M37702S4BFP	160ns (the fastest instruction at external clock 25MHz frequency)
Memory size	ROM	32K bytes
	RAM	2048 bytes
Input/Output ports	P0~P2, P4~P8	8 -bit× 8
	P3	4 -bit× 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit× 5
	TB0, TB1, TB2	16-bit× 3
Serial I/O		(UART or clock synchronous serial I/O)×2
A-D converter		8 -bit× 1 (8 channels)
Watchdog timer		12-bit× 1
Interrupts		3 external types, 16 internal types (Each interrupt can be set the priority levels to 0 ~ 7.)
Clock generating circuit		Built-in(externally connected to a ceramic resonator or quartz crystal resonator)
Supply voltage		5 V±10%
Power dissipation		60mW(at external clock 16MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 16M bytes
Operating temperature range		−20~85℃
Device structure		CMOS high-performance silicon gate process
Package		80-pin plastic molded QFP

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PIN DESCRIPTION

Pin	Name	Input/Output	Functions
V_{CC}, V_{SS}	Power supply		Supply 5 V±10% to V_{CC} and 0 V to V_{SS}.
CNV_{SS}	CNV_{SS} input	Input	This pin controls the processor mode. Connect to V_{SS} for single-chip mode, and to V_{CC} for external ROM types.
RESET	Reset input	Input	To enter the reset state, this pin must be kept at a "L" condition which should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz crystal resonator between X_{IN} and X_{OUT}. When an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
E	Enable output	Output	Data or instruction read and data write are performed when output from this pin is "L".
BYTE	Bus width selection input	Input	In memory expansion mode or microprocessor mode, this pin determines whether the external data bus is 8-bit width or 16-bit width. The width is 16 bits when "L" signal inputs and 8 bits when "H" signal inputs.
AV_{CC}, AV_{SS}	Analog supply input		Power supply for the A-D converter. Connect AV_{CC} to V_{CC} and AV_{SS} to V_{SS} externally.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
$P0_0 \sim P0_7$	I/O port P0	I/O	In single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in input mode when reset. Address($A_7 \sim A_0$) is output in memory expansion mode or microprocessor mode.
$P1_0 \sim P1_7$	I/O port P1	I/O	In single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in memory expansion mode or microprocessor mode and external data bus is 16-bit width, high-order data ($D_{15} \sim D_8$) is input or output when E output is "L" and an address ($A_{15} \sim A_8$) is output when E output is "H". If the BYTE pin is "H" that is an external data bus is 8-bit width, only address($A_{15} \sim A_8$) is output.
$P2_0 \sim P2_7$	I/O port P2	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode low-order data($D_7 \sim D_0$) is input or output when E output is "L" and an address($A_{23} \sim A_{16}$) is output when E output is "H".
$P3_0 \sim P3_3$	I/O port P3	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, R/W, BHE, ALE, and HLDA signals are output.
$P4_0 \sim P4_7$	I/O port P4	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, $P4_0$ and $P4_1$ become HOLD and RDY input pin respectively. Functions of other pins are the same as in single-chip mode. In single-chip mode or memory expansion mode, port $P4_2$ can be programmed for ϕ_1 output pin divided the clock to X_{IN} pin by 2. In microprocessor mode, $P4_2$ always has the function as ϕ_1 output pin.
$P5_0 \sim P5_7$	I/O port P5	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A0, timer A1, timer A2 and timer A3.
$P6_0 \sim P6_7$	I/O port P6	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A4, external interrupt input $\overline{INT_0}$, $\overline{INT_1}$ and $\overline{INT_2}$ pins, and input pins for timer B0, timer B1 and timer B2.
$P7_0 \sim P7_7$	I/O port P7	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as analog input $AN_0 \sim AN_7$ input pins. $P7_7$ also has an A-D conversion trigger input function.
$P8_0 \sim P8_7$	I/O port P8	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as R_xD, T_xD, CLK, $\overline{CTS}/\overline{RTS}$ pins for UART 0 and UART 1.

M37702M4AXXXFP, M37702M4BXXXFP
M37702S4AFP, M37702S4BFP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

BASIC FUNCTION BLOCKS

The M37702M4AXXXFP has the same functions as the M37702M2AXXXFP except for the following.
(1) The ROM size is 32K bytes.
(2) The RAM size is 2048 bytes.
Therefore, refer to the section on the M37702M2AXXXFP.

MEMORY

The memory map is shown in Figure 1.

ADDRESSING MODES

The M37702M4AXXXFP has 28 powerful addressing modes. Refer to the 7700 Family addressing mode description for the details of each addressing mode.

MACHINE INSTRUCTION LIST

The M37702M4AXXXFP has 103 machine instructions. Refer to the 7700 Family machine instruction list for details.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) Mask ROM order confirmation form
(2) 80P6N mark specification form
(3) ROM data (EPROM 3 sets)

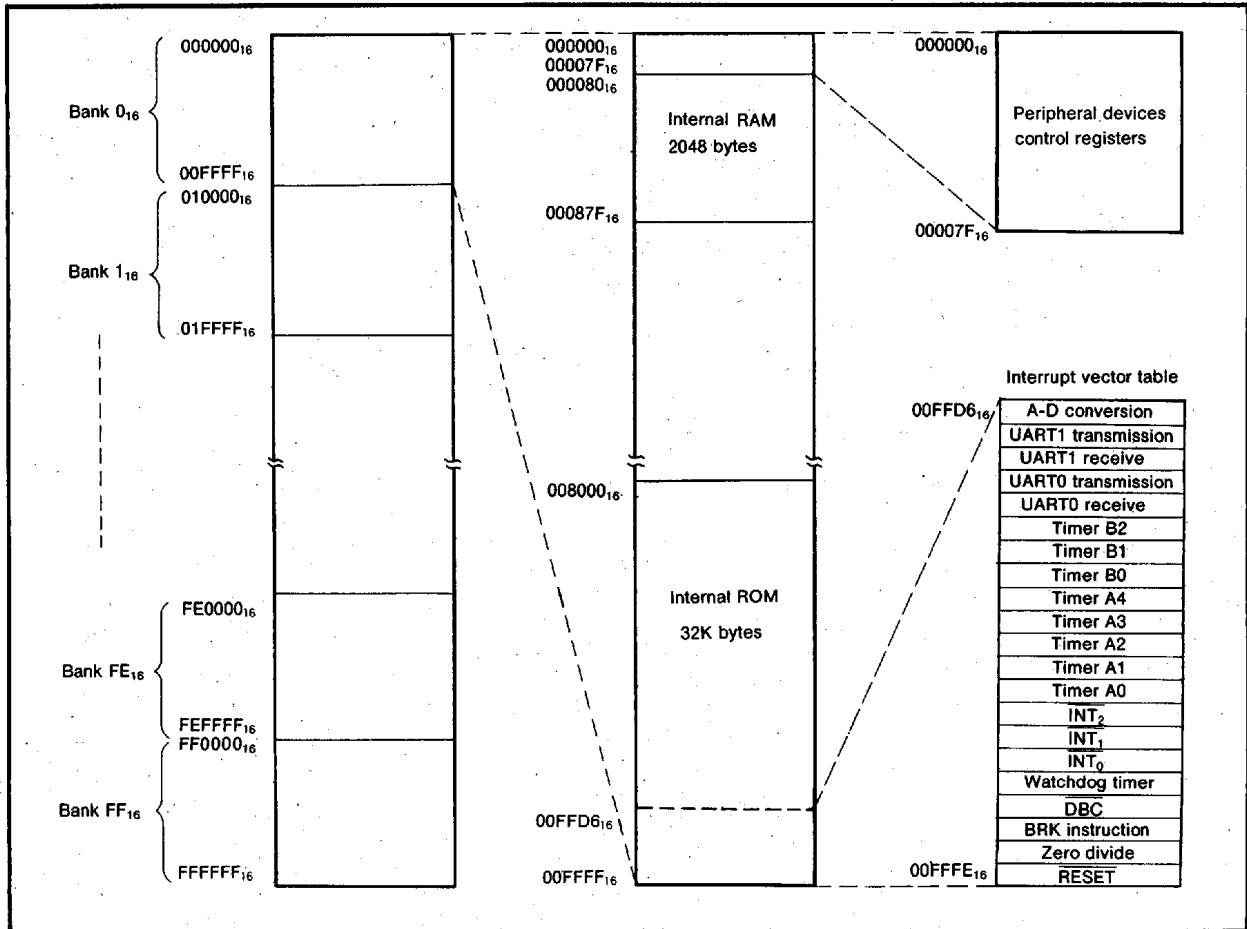Fig. 1   Memory map

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.3 \sim 7$	V
AV_{CC}	Analog supply voltage		$-0.3 \sim 7$	V
V_I	Input voltage $\overline{RESET}$, CNV_{SS}, BYTE		$-0.3 \sim 12$	V
V_I	Input voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$, V_{REF}, X_{IN}		$-0.3 \sim V_{CC}+0.3$	V
V_O	Output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$, X_{OUT}, $\overline{E}$		$-0.3 \sim V_{CC}+0.3$	V
P_d	Power dissipation	$T_a=25°C$	300	mW
T_{opr}	Operating temperature		$-20 \sim 85$	°C
T_{stg}	Storage temperature		$-40 \sim 150$	°C

RECOMMENDED OPERATING CONDITIONS ($V_{CC}=5V \pm 10\%$, $T_a=-20 \sim 85°C$, unless otherwise noted)

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
AV_{CC}	Analog supply voltage		V_{CC}		V
V_{SS}	Supply voltage		0		V
AV_{SS}	Analog supply voltage		0		V
V_{IH}	High-level input voltage $P0_0 \sim P0_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	$0.8V_{CC}$		V_{CC}	V
V_{IH}	High-level input voltage $P1_0 \sim P1_7$, $P2_0 \sim P2_7$ (in single-chip mode)	$0.8V_{CC}$		V_{CC}	V
V_{IH}	High-level input voltage $P1_0 \sim P1_7$, $P2_0 \sim P2_7$ (in memory expansion mode and microprocessor mode)	$0.5V_{CC}$		V_{CC}	V
V_{IL}	Low-level input voltage $P0_0 \sim P0_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0		$0.2V_{CC}$	V
V_{IL}	Low-level input voltage $P1_0 \sim P1_7$, $P2_0 \sim P2_7$ (in single-chip mode)	0		$0.2V_{CC}$	V
V_{IL}	Low-level input voltage $P1_0 \sim P1_7$, $P2_0 \sim P2_7$ (in memory expansion mode and microprocessor mode)	0		$0.16V_{CC}$	V
$I_{OH(peak)}$	High-level peak output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$			-10	mA
$I_{OH(avg)}$	High-level average output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$			-5	mA
$I_{OL(peak)}$	Low-level peak output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$			10	mA
$I_{OL(avg)}$	Low-level average output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$			5	mA
$f(X_{IN})$	External clock frequency input — M37702M4AXXXFP, M37702S4AFP			16	MHz
	External clock frequency input — M37702M4BXXXFP, M37702S4BFP			25	MHz

Note 1. Average output current is the average value of a 100ms interval.
 2. The sum of $I_{OL(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80mA or less,
 the sum of $I_{OH(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80mA or less,
 the sum of $I_{OL(peak)}$ for ports P4, P5, P6, and P7 must be 80mA or less, and
 the sum of $I_{OH(peak)}$ for ports P4, P5, P6, and P7 must be 80mA or less.

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MITSUBISHI ELECTRIC

M37702M4AXXXFP

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25°C, f(X_{IN})=16MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	High-level output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0$, $P3_1$, $P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$	I_{OH}=−10mA		3	~		V
V_{OH}	High-level output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0$, $P3_1$, $P3_3$	I_{OH}=−400μA		4.7			V
V_{OH}	High-level output voltage $P3_2$	I_{OH}=−10mA		3.1			V
		I_{OH}=−400μA		4.8			
V_{OH}	High-level output voltage $\overline{E}$	I_{OH}=−10mA		3.4			V
		I_{OH}=−400μA		4.8			
V_{OL}	Low-level output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0$, $P3_1$, $P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$	I_{OL}=10mA				2	V
V_{OL}	Low-level output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0$, $P3_1$, $P3_3$	I_{OL}=2mA				0.45	V
V_{OL}	Low-level output voltage $P3_2$	I_{OL}=10mA				1.9	V
		I_{OL}=2mA				0.43	
V_{OL}	Low-level output voltage $\overline{E}$	I_{OL}=10mA				1.6	V
		I_{OL}=2mA				0.4	
$V_{T+} - V_{T-}$	Hysteresis $\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN} \sim TA4_{IN}$, $TB0_{IN} \sim TB2_{IN}$, $\overline{INT_0} \sim \overline{INT_2}$, AD_{TRG}, $\overline{CTS_0}$, $\overline{CTS_1}$, CLK_0, CLK_1			0.4		1	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{RESET}$			0.2		0.5	V
$V_{T+} - V_{T-}$	Hysteresis X_{IN}			0.1		0.3	V
I_{IH}	High-level input current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5V				5	μA
I_{IL}	Low-level input current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_7$, $P5_0 \sim P5_7$, $P6_0 \sim P6_7$, $P7_0 \sim P7_7$, $P8_0 \sim P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V				−5	μA
V_{RAM}	RAM hold voltage	When clock is stopped.		2			V
I_{CC}	Power supply current	In single-chip mode output only pin is open and other pins are V_{SS} during reset.	f(X_{IN})=16MHz, square waveform		12	24	mA
			T_a=25°C when clock is stopped.			1	μA
			T_a=85°C when clock is stopped.			20	

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25°C, f(X_{IN})=16MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time		14.25			μs
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog Input voltage		0		V_{REF}	V

MITSUBISHI ELECTRIC

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

M37702M4BXXXFP

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25°C, $f(X_{IN})$=25MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	High-level output voltage $P0_0{\sim}P0_7$, $P1_0{\sim}P1_7$, $P2_0{\sim}P2_7$, $P3_0$, $P3_1$, $P3_3$, $P4_0{\sim}P4_7$, $P5_0{\sim}P5_7$, $P6_0{\sim}P6_7$, $P7_0{\sim}P7_7$, $P8_0{\sim}P8_7$	I_{OH}=−10mA		3			V
V_{OH}	High-level output voltage $P0_0{\sim}P0_7$, $P1_0{\sim}P1_7$, $P2_0{\sim}P2_7$, $P3_0$, $P3_1$, $P3_3$	I_{OH}=−400μA		4.7			V
V_{OH}	High-level output voltage $P3_2$	I_{OH}=−10mA		3.1			V
		I_{OH}=−400μA		4.8			
V_{OH}	High-level output voltage $\overline{E}$	I_{OH}=−10mA		3.4			V
		I_{OH}=−400μA		4.8			
V_{OL}	Low-level output voltage $P0_0{\sim}P0_7$, $P1_0{\sim}P1_7$, $P2_0{\sim}P2_7$, $P3_0$, $P3_1$, $P3_3$, $P4_0{\sim}P4_7$, $P5_0{\sim}P5_7$, $P6_0{\sim}P6_7$, $P7_0{\sim}P7_7$, $P8_0{\sim}P8_7$	I_{OL}=10mA				2	V
V_{OL}	Low-level output voltage $P0_0{\sim}P0_7$, $P1_0{\sim}P1_7$, $P2_0{\sim}P2_7$, $P3_0$, $P3_1$, $P3_3$	I_{OL}=2mA				0.45	V
V_{OL}	Low-level output voltage $P3_2$	I_{OL}=10mA				1.9	V
		I_{OL}=2mA				0.43	
V_{OL}	Low-level output voltage $\overline{E}$	I_{OL}=10mA				1.6	V
		I_{OL}=2mA				0.4	
$V_{T+}-V_{T-}$	Hysteresis $\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}{\sim}TA4_{IN}$, $TB0_{IN}{\sim}TB2_{IN}$, $\overline{INT_0}{\sim}\overline{INT_2}$, $\overline{AD_{TRG}}$, $\overline{CTS_0}$, $\overline{CTS_1}$, CLK_0, CLK_1			0.4		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$			0.2		0.5	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}			0.1		0.3	V
I_{IH}	High-level input current $P0_0{\sim}P0_7$, $P1_0{\sim}P1_7$, $P2_0{\sim}P2_7$, $P3_0{\sim}P3_3$, $P4_0{\sim}P4_7$, $P5_0{\sim}P5_7$, $P6_0{\sim}P6_7$, $P7_0{\sim}P7_7$, $P8_0{\sim}P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5V				5	μA
I_{IL}	Low-level input current $P0_0{\sim}P0_7$, $P1_0{\sim}P1_7$, $P2_0{\sim}P2_7$, $P3_0{\sim}P3_3$, $P4_0{\sim}P4_7$, $P5_0{\sim}P5_7$, $P6_0{\sim}P6_7$, $P7_0{\sim}P7_7$, $P8_0{\sim}P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V				−5	μA
V_{RAM}	RAM hold voltage	When clock is stopped.		2			V
I_{CC}	Power supply current	In single-chip mode output only pin is open and other pins are V_{SS} during reset.	$f(X_{IN})$=25MHz, square waveform		19	38	mA
			T_a=25°C when clock is stopped.			1	μA
			T_a=85°C when clock is stopped.			20	

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25°C, $f(X_{IN})$=25MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time		9.12			μs
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

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TIMING REQUIREMENTS (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, unless otherwise noted)
External clock input

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
t_C	External clock input cycle time	62		40		ns
$t_{W(H)}$	External clock input high-level pulse width	25		15		ns
$t_{W(L)}$	External clock input low-level pulse width	25		15		ns
t_r	External clock rise time		10		8	ns
t_f	External clock fall time		10		8	ns

Single-chip mode

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{SU(P0D—E)}$	Port P0 input setup time	100		60		ns
$t_{SU(P1D—E)}$	Port P1 input setup time	100		60		ns
$t_{SU(P2D—E)}$	Port P2 input setup time	100		60		ns
$t_{SU(P3D—E)}$	Port P3 input setup time	100		60		ns
$t_{SU(P4D—E)}$	Port P4 input setup time	100		60		ns
$t_{SU(P5D—E)}$	Port P5 input setup time	100		60		ns
$t_{SU(P6D—E)}$	Port P6 input setup time	100		60		ns
$t_{SU(P7D—E)}$	Port P7 input setup time	100		60		ns
$t_{SU(P8D—E)}$	Port P8 input setup time	100		60		ns
$t_{h(E—P0D)}$	Port P0 input hold time	0		0		ns
$t_{h(E—P1D)}$	Port P1 input hold time	0		0		ns
$t_{h(E—P2D)}$	Port P2 input hold time	0		0		ns
$t_{h(E—P3D)}$	Port P3 input hold time	0		0		ns
$t_{h(E—P4D)}$	Port P4 input hold time	0		0		ns
$t_{h(E—P5D)}$	Port P5 input hold time	0		0		ns
$t_{h(E—P6D)}$	Port P6 input hold time	0		0		ns
$t_{h(E—P7D)}$	Port P7 input hold time	0		0		ns
$t_{h(E—P8D)}$	Port P8 input hold time	0		0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{SU(P1D—E)}$	Port P1 input setup time	45		30		ns
$t_{SU(P2D—E)}$	Port P2 input setup time	45		30		ns
$t_{SU(RDY—\phi_1)}$	RDY input setup time	60		55		ns
$t_{SU(HOLD—\phi_1)}$	HOLD input setup time	60		55		ns
$t_{h(E—P1D)}$	Port P1 input hold time	0		0		ns
$t_{h(E—P2D)}$	Port P2 input hold time	0		0		ns
$t_{h(\phi_1—RDY)}$	RDY input hold time	0		0		ns
$t_{h(\phi_1—HOLD)}$	HOLD input hold time	0		0		ns

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Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(TA)}$	TAi$_{IN}$ input cycle time	125		80		ns
$t_{W(TAH)}$	TAi$_{IN}$ input high-level pulse width	62		40		ns
$t_{W(TAL)}$	TAi$_{IN}$ input low-level pulse width	62		40		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(TA)}$	TAi$_{IN}$ input cycle time	500		320		ns
$t_{W(TAH)}$	TAi$_{IN}$ input high-level pulse width	250		160		ns
$t_{W(TAL)}$	TAi$_{IN}$ input low-level pulse width	250		160		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(TA)}$	TAi$_{IN}$ input cycle time	250		160		ns
$t_{W(TAH)}$	TAi$_{IN}$ input high-level pulse width	125		80		ns
$t_{W(TAL)}$	TAi$_{IN}$ input low-level pulse width	125		80		ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{W(TAH)}$	TAi$_{IN}$ input high-level pulse width	125		80		ns
$t_{W(TAL)}$	TAi$_{IN}$ input low-level pulse width	125		80		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(UP)}$	TAi$_{OUT}$ input cycle time	2500		2000		ns
$t_{W(UPH)}$	TAi$_{OUT}$ input high-level pulse width	1250		1000		ns
$t_{W(UPL)}$	TAi$_{OUT}$ input low-level pulse width	1250		1000		ns
$t_{SU(UP-T_{IN})}$	TAi$_{OUT}$ input setup time	500		400		ns
$t_{h(T_{IN}-UP)}$	TAi$_{OUT}$ input hold time	500		400		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(TB)}$	TBi$_{IN}$ input cycle time (one edge count)	125		80		ns
$t_{W(TBH)}$	TBi$_{IN}$ input high-level pulse width (one edge count)	62		40		ns
$t_{W(TBL)}$	TBi$_{IN}$ input low-level pulse width (one edge count)	62		40		ns
$t_{C(TB)}$	TBi$_{IN}$ input cycle time (both edges count)	250		160		ns
$t_{W(TBH)}$	TBi$_{IN}$ input high-level pulse width (both edges count)	125		80		ns
$t_{W(TBL)}$	TBi$_{IN}$ input low-level pulse width (both edges count)	125		80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(TB)}$	TBi$_{IN}$ input cycle time	500		320		ns
$t_{W(TBH)}$	TBi$_{IN}$ input high-level pulse width	250		160		ns
$t_{W(TBL)}$	TBi$_{IN}$ input low-level pulse width	250		160		ns

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(TB)}$	TBi$_{IN}$ input cycle time	500		320		ns
$t_{W(TBH)}$	TBi$_{IN}$ input high-level pulse width	250		160		ns
$t_{W(TBL)}$	TBi$_{IN}$ input low-level pulse width	250		160		ns

A-D trigger input

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(AD)}$	AD$_{TRG}$ input cycle time (minimum allowable trigger)	1000		1000		ns
$t_{W(ADL)}$	AD$_{TRG}$ input low-level pulse width	125		125		ns

Serial I/O

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(CK)}$	CLK$_i$ input cycle time	250		200		ns
$t_{W(CKH)}$	CLK$_i$ input high-level pulse width	125		100		ns
$t_{W(CKL)}$	CLK$_i$ input low-level pulse width	125		100		ns
$t_{d(C-Q)}$	TxD$_i$ output delay time		90		80	ns
$t_{h(C-Q)}$	TxD$_i$ hold time	0		0		ns
$t_{su(D-C)}$	RxD$_i$ input setup time	30		20		ns
$t_{h(C-D)}$	RxD$_i$ input hold time	90		90		ns

External interrupt $\overline{INT_i}$ input

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{W(INH)}$	INT$_i$ input high-level pulse width	250		250		ns
$t_{W(INL)}$	INT$_i$ input low-level pulse width	250		250		ns

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SWITCHING CHARACTERISTICS (V$_{CC}$=5V±10%, V$_{SS}$=0V, T$_a$=25℃, unless otherwise noted)
Single-chip mode

Symbol	Parameter	Test conditions	Limits				Unit
			16MHz		25MHz		
			Min.	Max.	Min.	Max.	
t$_{d(E-P0Q)}$	Port P0 data output delay time			100		80	ns
t$_{d(E-P1Q)}$	Port P1 data output delay time			100		80	ns
t$_{d(E-P2Q)}$	Port P2 data output delay time			100		80	ns
t$_{d(E-P3Q)}$	Port P3 data output delay time			100		80	ns
t$_{d(E-P4Q)}$	Port P4 data output delay time	Fig. 2		100		80	ns
t$_{d(E-P5Q)}$	Port P5 data output delay time			100		80	ns
t$_{d(E-P6Q)}$	Port P6 data output delay time			100		80	ns
t$_{d(E-P7Q)}$	Port P7 data output delay time			100		80	ns
t$_{d(E-P8Q)}$	Port P8 data output delay time			100		80	ns

Memory expansion mode and microprocessor mode (when wait bit = "1")

Symbol	Parameter	Test conditions	Limits				Unit
			16MHz		25MHz		
			Min.	Max.	Min.	Max.	
t$_{d(P0A-E)}$	Port P0 address output delay time		30		12		ns
t$_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")			70		45	ns
t$_{PXZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")			5		5	ns
t$_{d(P1A-E)}$	Port P1 address output delay time		30		12		ns
t$_{d(P1A-ALE)}$	Port P1 address output delay time		24		5		ns
t$_{d(E-P2Q)}$	Port P2 data output delay time			70		45	ns
t$_{PXZ(E-P2Z)}$	Port P2 floating start delay time			5		5	ns
t$_{d(P2A-E)}$	Port P2 address output delay time		30		12		ns
t$_{d(P2A-ALE)}$	Port P2 address output delay time		24		5		ns
t$_{d(\phi_1-HLDA)}$	HLDA output delay time			50		50	ns
t$_{d(ALE-E)}$	ALE output delay time		4		4		ns
t$_{W(ALE)}$	ALE pulse width	Fig. 2	35		22		ns
t$_{d(BHE-E)}$	BHE output delay time		30		20		ns
t$_{d(R/W-E)}$	R/W output delay time		30		20		ns
t$_{d(E-\phi_1)}$	ϕ_1 output delay time		0	20	0	18	ns
t$_{h(E-P0A)}$	Port P0 address hold time		25		18		ns
t$_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9		9		ns
t$_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		25		18		ns
t$_{PZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		25		18		ns
t$_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		25		18		ns
t$_{h(ALE-P2A)}$	Port P2 address hold time		9		9		ns
t$_{h(E-P2Q)}$	Port P2 data hold time		25		18		ns
t$_{PZX(E-P2Z)}$	Port P2 floating release delay time		25		18		ns
t$_{h(E-BHE)}$	BHE hold time		18		18		ns
t$_{h(E-R/W)}$	R/W hold time		18		18		ns
t$_{W(EL)}$	E pulse width		95		50		ns

Memory expansion mode and microprocessor mode (when wait bit = "0", and external memory area accessed)

| Symbol	Parameter	Test conditions	Limits				Unit
			16MHz		25MHz		
			Min.	Max.	Min.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time		30		12		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")			70		45	ns
$t_{PXZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")			5		5	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		30		12		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time		24		5		ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			70		45	ns
$t_{PXZ(E-P2Z)}$	Port P2 floating start delay time			5		5	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		30		12		ns
$t_{d(P2A-ALE)}$	Port P2 address output delay time		24		5		ns
$t_{d(\phi_1-HLDA)}$	HLDA output delay time			50		50	ns
$t_{d(ALE-E)}$	ALE output delay time	Fig. 2	4		4		ns
$t_{W(ALE)}$	ALE pulse width		35		22		ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time		30		20		ns
$t_{d(R/W-E)}$	R/W output delay time		30		20		ns
$t_{d(E-\phi_1)}$	ϕ_1 output delay time		0	20	0	18	ns
$t_{h(E-P0A)}$	Port P0 address hold time		25		18		ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9		9		ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		25		18		ns
$t_{PZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		25		18		ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		25		18		ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		9		9		ns
$t_{h(E-P2Q)}$	Port P2 data hold time		25		18		ns
$t_{PZX(E-P2Z)}$	Port P2 floating release delay time		25		18		ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		18		18		ns
$t_{h(E-R/W)}$	R/W hold time		18		18		ns
$t_{W(EL)}$	$\overline{E}$ pulse width		220		130		ns
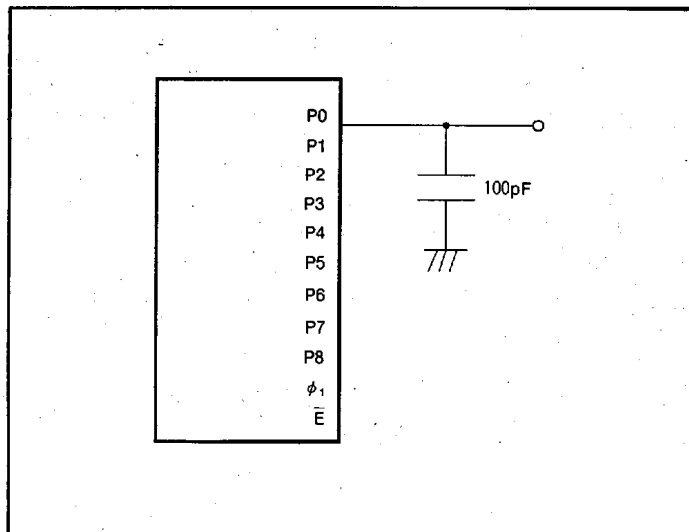
Fig. 2 Testing circuit for ports P0~P8, ϕ_1

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