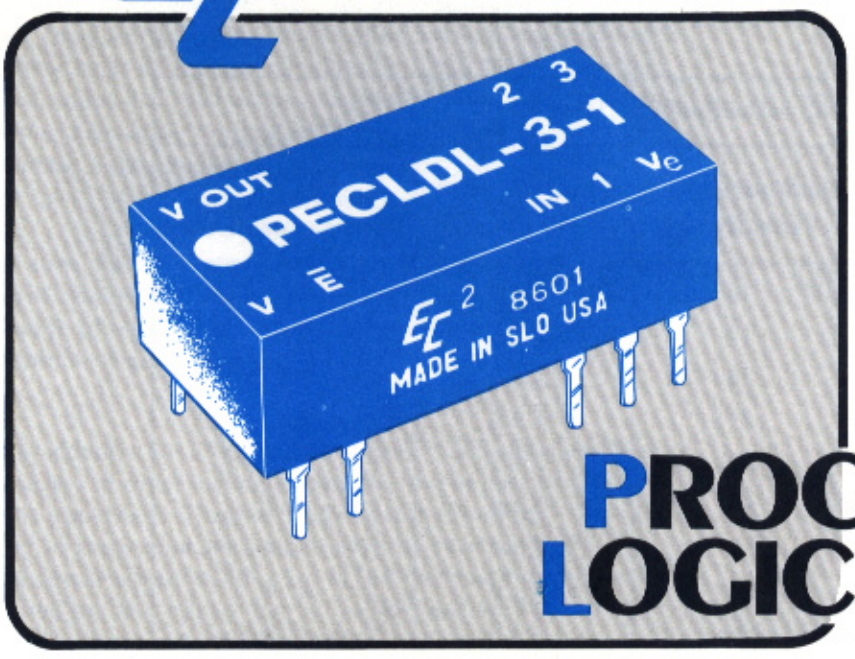

low profile

ECL COMPATIBLE 3-BIT PROGRAMMABLE LOGIC DELAY LINE

- ECL input and output levels
- Delays stable and precise
- 16-pin DIP package (.250 high)
- Available in delays up to 353ns
- Available in 18 delay steps with resolution from 1 to 50ns
- Propagation delays fully compensated
- All delays digitally programmable
- 70 ECL DC fan-out capacity

design notes

The "DIP Series" of Programmable Logic Delay Lines developed by Engineered Components Company have been designed to allow for final delay adjustment during or after installation in a circuit. These Logic Delay Lines incorporate required driving and pick-off circuitry and are contained in a 16-pin DIP package compatible with ECL "10,000 Series" circuits. The design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the required delay.

The Logic Delay Lines are digitally programmable by the presence of either a "1" or a "0" at each of the programming pins. Since the input and the output terminals are fixed and the programming is accomplished only by DC voltage levels, programming may be accomplished by remote switching or permanent termination of the appropriate programming pins of the Logic Delay Line to Vcc; the Logic Delay Line may also be programmed automatically by computer generated data. MUX set-up time is 2ns typical. When no need exists in the application to change delay time during normal use, the desired delay is most conveniently established by use of a Vcc pad around each programming pin; programming is accomplished by cutting off those pins which are to remain at state "0" before insertion of the Logic Delay Line into the printed circuit board.

The PECLDL is designed for use with positive input pulses and will reproduce these at the output without inversion. On modules with delay change of 1 to 8ns/step, input impedance is approximately 900 ohms; on modules with delay change of 9ns/step and greater, input impedance is approximately 100 ohms. All modules can be driven from a standard ECL gate with an external pulldown resistor of 100 ohms to −2V or 470 ohms to −5.2V. Output is standard ECL 10,000 open emitter; programming inputs are standard ECL 10,000 single fan-in. These Logic Delay Lines have the capability of driving up to 70 ECL DC loads.

engineered components company
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Phone: (805) 544-3800

DESIGN NOTES (continued)

The PECLDL is offered in 18 models with time delays to a maximum of 353ns and with step resolution as shown in the Part Number Table. Programming of maximum delays is accomplished in 8 delay steps in accordance with the Truth Table examples shown on page 3. Tolerances on minimum delay, delay change per step and deviation from programmed delay are shown in the Part Number Table on page 3.

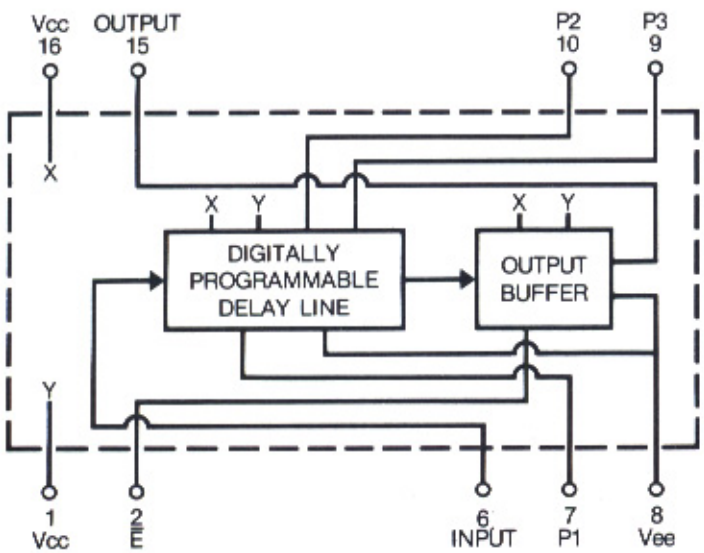
Rise time for all Logic Delay Lines is 5ns maximum, when measured from 20% to 80% pulse amplitude. Temperature coefficient of delay is less than 150ppm/°C over the operating temperature range of −30° to +85°C.

These modules are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are burned-in to Level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 2 million hours.

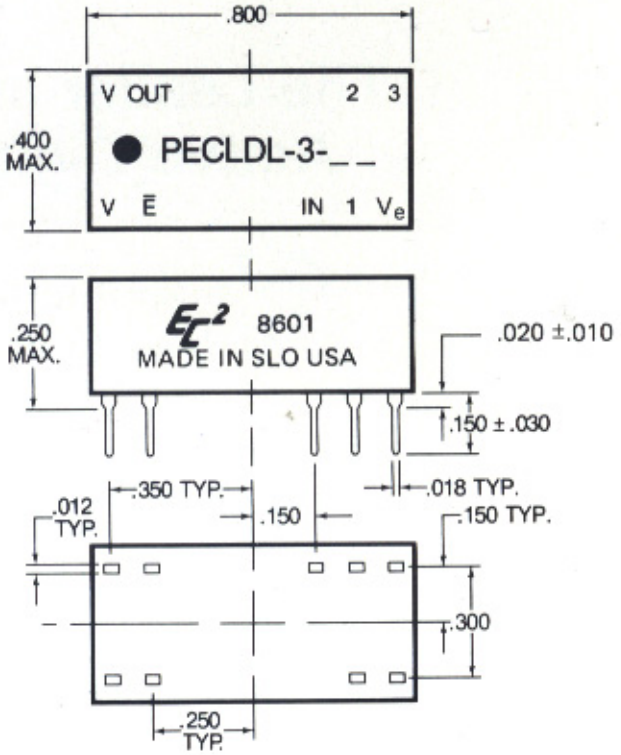
The "DIP Series" Programmable Logic Delay Lines are packaged in a 16-pin DIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, Type SDG-F, and are fully encapsulated in epoxy resin. Flat metal leads meet the solderability requirements of MIL-STD-202, Method 208. Leads provide positive standoff from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

Marking consists of manufacturer's name, logo (EC^2), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



TEST CONDITIONS

1. All measurements are made at 25°C.
2. Vee supply voltage is maintained at −5.2V DC.
3. All units are tested using a positive input pulse provided by a standard open emitter ECL 10,000 gate. The input and output utilize a 100 ohm pulldown resistor to −2V; the output is also loaded with one ECL 10,000 gate.

ϕ4. Input pulse width used is 20ns for units with delay change of 1 to 5ns/step and 150ns for units with delay change of 6ns/step and greater. Pulse period for all units is 1000ns.

OPERATING SPECIFICATIONS

Supply Voltage: . . . . . −5.2V ±5% to Vee (Can be operated on +5V to Vcc)
Supply Current: . . . . . 50ma typical
Logic 1 Input at 25°C.
  Voltage . . . . . −.98V min.
  Current:
    3-1 through 3-8 . . . . 750ua typical
    3-9 through 3-50 . . . 16ma typical
Logic 0 Input at 25°C.
  Voltage . . . . . −1.63V max.
  Current:
    3-1 through 3-8 . . . . −750ua typical
    3-9 through 3-50 . . . −6ma typical
Logic 1 Output at 25°C. . . . . −.96V min.
Logic 0 Output at 25°C. . . . . −1.65V max.
Operating teperature range: . . . −30° to +85°C.
Storage temperature range: . . . −55° to +125°C.

PART NUMBER TABLE

ϕ DELAYS AND TOLERANCES (in ns)				
Part Number	*Step Zero Delay Time	Maximum Delay Time (Nom)	Delay Change Per Step	* *Maximum Deviation From Programmed Delay
PECLDL-3-1	2.6 ±.6	10	1 ±.3	±.4
PECLDL-3-2	2.6 ±.6	17	2 ±.4	±.6
PECLDL-3-3	2.6 ±.6	24	3 ±.5	±.8
PECLDL-3-4	2.6 ±.6	31	4 ±.5	±.9
PECLDL-3-5	2.6 ±.6	38	5 ±.5	±1
PECLDL-3-6	2.6 ±.6	45	6 ±.6	±1.2
PECLDL-3-7	2.6 ±.6	52	7 ±.7	±1.4
PECLDL-3-8	2.6 ±.6	59	8 ±.8	±1.6
PECLDL-3-9	2.6 ±.6	66	9 ±.9	±1.8
PECLDL-3-10	2.6 ±.6	73	10 ±1	±2
PECLDL-3-15	2.6 ±.6	108	15 ±1	±3
PECLDL-3-20	2.6 ±.6	143	20 ±1.5	±4
PECLDL-3-25	2.6 ±.6	178	25 ±1.5	±5
PECLDL-3-30	2.6 ±.6	213	30 ±2	±6
PECLDL-3-35	2.6 ±.6	248	35 ±2	±7
PECLDL-3-40	2.6 ±.6	283	40 ±2.5	±8
PECLDL-3-45	2.6 ±.6	318	45 ±2.5	±9
PECLDL-3-50	2.6 ±.6	353	50 ±2.5	±10

For part number, maximum delay time (nom) tabulation and truth table examples below, a step zero delay time of 3ns was assumed.

TRUTH TABLE EXAMPLES

Programming Pins / Part Number	3	0	0	0	0	1	1	1	1
	2	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0	1
PECLDL-3-1		3	1	2	3	4	5	6	7
PECLDL-3-2		3	2	4	6	8	10	12	14
PECLDL-3-3		3	3	6	9	12	15	18	21
ETC.									

* Delay at step zero is referenced to the input pin.

* * All delay times after step zero are referenced to step zero.

ϕ All modules can be operated with a minimum input pulse width of 40% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified delay times for specific applications.