

LINEAR INTEGRATED CIRCUIT**TV HORIZONTAL AND VERTICAL PROCESSOR**

The TCA 511 is a silicon monolithic integrated circuit in a 16-lead dual in-line plastic package. It incorporates the following functions: high stability horizontal oscillator, horizontal APC circuit with high noise immunity and large pull-in range, high stability vertical oscillator and sawtooth generator.

It is intended for driving TV horizontal and vertical transistorized output stages.

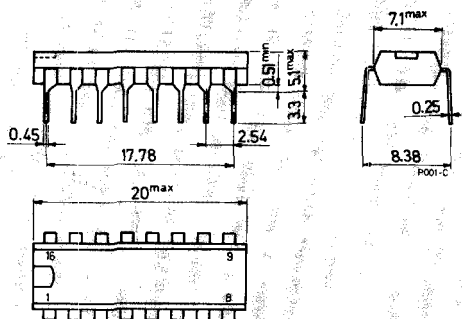
ABSOLUTE MAXIMUM RATINGS

V_s	Vertical section supply voltage (between pins 3 and 13)	15	V
V_s	Horizontal section supply voltage (between pins 4 and 13)	15	V
V_7, V_{12}, V_{15}	Pin 7, 12, 15 voltage (collector to ground)	15	V
V_i	Vertical sync. input voltage (between pins 2 and 13 - see note)	-5	V
V_i	Horizontal sync. input voltage (between pins 6 and 13 - see note)	-5	V
I_B	DC current (from pin 8)	30	mA
I_{12}, I_{14}, I_{15}	Peak current (into pins 12, 14 and 15)	50	mA
P_{tot}	Total power dissipation at $T_{amb} \leq 60^\circ\text{C}$	500	mW
T_{stg}	Storage temperature	-55 to 125	$^\circ\text{C}$
T_{op}	Operating temperature	0 to 60	$^\circ\text{C}$

NOTE: The positive input voltage at pin 2 and pin 6 must not be greater than the voltage at pin 3 and pin 4 respectively.

MECHANICAL DATA

Dimensions in mm



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ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
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VERTICAL SECTION

I_3	Quiescent current	$V_s = 12\text{ V}$ $f = 50\text{ Hz}$	4		mA	2
V_3^*	Supply voltage		9		V	
V_1	Peak to peak oscillator sawtooth voltage	$V_s = 12\text{ V}$ $f = 50\text{ Hz}$	2.6		V	
V_2	Peak sync. input voltage	$V_s = 12\text{ V}$ $f = 50\text{ Hz}$	3		V	
V_{14}	Low level output voltage	$V_s = 12\text{ V}$		1.5	V	3
V_{15}	Low level output voltage	$I_{15} = 15\text{ mA}$		0.5	V	
R_2	Parallel input resistance at pin 2	$V_s = 12\text{ V}$ $V_2 = 3\text{ V}$	50		k Ω	—
t^{**}	Output pulse width at pin 15	$V_s = 12\text{ V}$ $f = 50\text{ Hz}$ $R_{10} = 15\text{ k}\Omega$	0.75		ms	2
Δf	Locking range	$V_s = 12\text{ V}$ $f = 50\text{ Hz}$	-17		%	
$\frac{\Delta f}{\Delta T_{amb}}$	Frequency/temperature coefficient	$V_s = 12\text{ V}$ $T_{amb} = 20\text{ to }70^{\circ}\text{C}$	-0.015		$\frac{\text{Hz}}{^{\circ}\text{C}}$	

HORIZONTAL SECTION

I_4	Quiescent current	$V_s = 12\text{ V}$ $f = 15625\text{ Hz}$ $R_{11-13} = 0$	19		mA	2
V_4^*	Supply voltage		9		V	
V_6	Peak sinc. input voltage	$V_s = 12\text{ V}$ $f = 15625\text{ Hz}$	3		V	

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
V_8 Regulated output voltage	$V_s = 12\text{ V}$ $f = 15625\text{ Hz}$	7.5			V	2
V_{10} Peak to peak oscillator sawtooth voltage		3.3			V	
V_{12} Low level output voltage	$V_s = 12\text{ V}$ $I_{12} = 15\text{ mA}$	0.45			V	3
R_6 Parallel input resistance at pin 6	$V_s = 12\text{ V}$ $V_6 = 3\text{ V}$	50			k Ω	—
t^{***} Output pulse width at pin 12	$V_s = 12\text{ V}$ $f = 15625\text{ Hz}$ a) $R_{11-13} = 0$ b) $R_{11-13} = \infty$	13			μs	2
		35			μs	
t_d Leading edge of output pulse to leading edge of sync. pulse phasing	$V_s = 12\text{ V}$ $f = 15625\text{ Hz}$	4			μs	
Δf Pull-in range		± 1.3			kHz	
Δf Hold-in range		± 1.4			kHz	
$\frac{\Delta f}{\Delta V_9}$ Oscillator control sensitivity	$V_s = 12\text{ V}$	10			$\frac{\text{kHz}}{\text{V}}$	
$\frac{\Delta f}{\Delta t_d}$ APC loop gain		2			$\frac{\text{kHz}}{\mu\text{s}}$	
$\frac{\Delta f}{\Delta V_s}$ Oscillator frequency drift	$V_s = 9\text{ to }14\text{ V}$	+ 0.7			$\frac{\%}{\text{V}}$	
$\frac{\Delta f}{\Delta T_{\text{amb}}}$ Frequency/temperature coefficient	$V_s = 12\text{ V}$ $T_{\text{amb}} = 20\text{ to }70\text{ }^\circ\text{C}$	+ 5			$\frac{\text{Hz}}{^\circ\text{C}}$	

NOTES: * Minimum supply voltage for correct operation of the device.

** The output pulse width can be adjusted by means of the external resistance connected between pins 1 and 6.

*** The output pulse width can be adjusted by means of the external resistance or by a voltage $\leq 5.3\text{ V}$, connected between pin 11 and pin 13.

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Fig. 1 - Functional block diagram

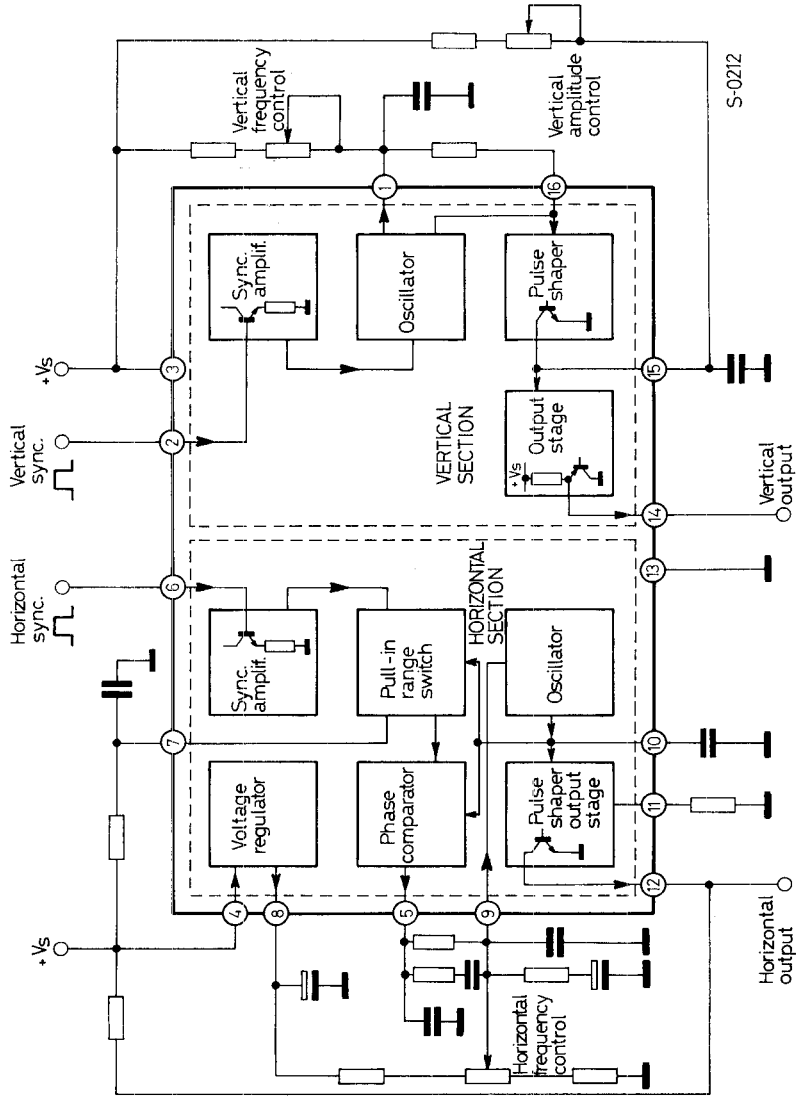


Fig. 2 - Test circuit

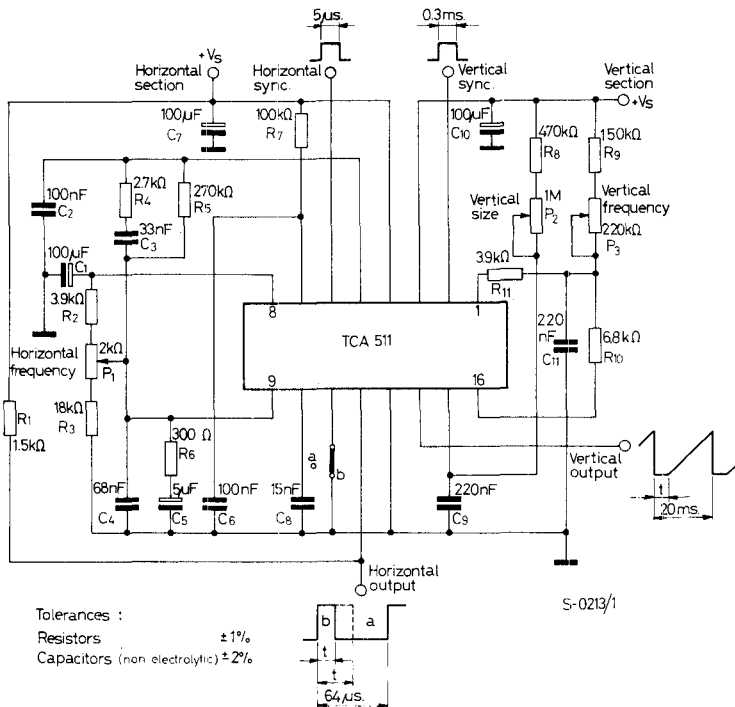
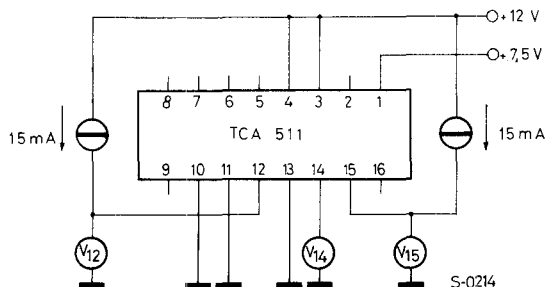


Fig. 3 - V_{12} , V_{14} and V_{15} test circuit



APPLICATION INFORMATION

Power Supply

The circuit can work with stabilized supply voltage having a value from 9 to 15 V. A dropping resistor and a filter capacitor may be used to obtain the supply from higher voltages; however, the voltage on pins 3 and 4 must never exceed the maximum permitted voltage.

Synchronization

Pins 2 and 6 can be DC driven if the reference level of the synchronization pulses is less than 1 V. With reference levels greater than this value, a coupling capacitor must be inserted in series with the input, and pins 2 and 6 must be connected to ground via a resistor.

Vertical Oscillator

The capacitor connected to pin 1 must be selected with regard to the frequency tolerance, to the thermal stability and to the capacitor's ageing.

The width of the output pulse, to be chosen according to the needs of the output stages, is defined by the resistor connected between pin 1 and pin 16.

Vertical Output

The vertical output is taken from pin 14, which is a buffered output of the sawtooth voltage generated at pin 15.

The output current from pin 14 is defined by an internal resistor in the integrated circuit. If a greater current is needed, a resistor may be connected between pin 14 and pin 3.

The oscillator output pulse is available at pin 15 if the capacitor C9 is not connected. This configuration is used for driving output stages in which the sawtooth is generated by Miller effect.

Horizontal Oscillator

The capacitor connected between pin 10 and ground must be selected with regard to the frequency tolerance, to the thermal stability and to the capacitor's ageing.

In multistandard receivers, the oscillation frequency may be changed by switching the value of the capacitor connected to pin 10.

APPLICATION INFORMATION (continued)

Phase Comparator

The phase comparator's output consists of current pulses acting on the oscillator control voltage.

The external components C2, C3, C4, C5, R4, R5 and R6 (fig. 2) define the circuit performance with respect to the pull-in range, the hold-in range and the frequency variations that occur on switching-on and switching-off.

Moreover the pull-in range depends on the absolute value of the voltage divider R2, P1 and R3.

A coincidence detector is connected to pin 7; this modifies the pull-in range and the noise immunity, depending on whether the system is synchronised or is searching for synchronization. The time constant applied to pin 7 avoids uncertainty during the switch from one state to the other.

Horizontal Output

The collector of the output transistor is connected to pin 12; its load resistor, externally connected between pin 12 and pin 4, defines the amplitude of the output current pulse.

The width of the output pulse can be varied between 13 and 35 μs by means of the resistor connected between pin 11 and ground, or else by means of a voltage ≤ 5.3 V applied between pin 11 and ground. This control acts upon the trailing edge of the pulse, hence the phase advance of the leading edge stays constant with respect to the synchronism.