VITELIC

V61C01 & V61C02 FAMILY HIGH PERFORMANCE LOW POWER 512 x 9 & 1024 x 9 BIT CMOS PARALLEL FIFO MEMORY

Features

- First-In/First-Out Memory
- 512 x 9 organization (V61C01, V61C01L)
- 1024 x 9 organization (V61C02, V61C02L)
- Dual-Port operation with separate Read/Write ports
- Simultaneous, asynchronous operation of both ports
- FIFO empty and FIFO full flags
- Half-full/Half-empty flag in single device operation
- Fully expandable in width and depth
- Retransmit function for data communication applications
- V61C01 is pinout and functionally compatible to the MK4501 and 7201
- V61C02 is pinout and functionally compatible to the 7202
- CMOS technology gives low power and high performance
  - V61C01/V61C01L
    Cycle Time—45 ns (–35)
    Operating Current—40 mA (typ.)
  - V61C02/V61C02L
    Cycle Time—50 ns (–40)
    Operating Current—40 mA (typ.)
- Standard 28 pin 600 mil DIP and 28 pin 300 mil DIP.

Description

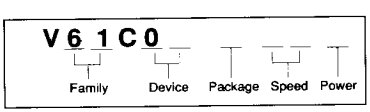
The Vitelic V61C01 and V61C02 are Dual-Port FIFO memory components that accept data to be written on one 9-bit bus and recover the stored data on another 9-bit bus in the same order as written. Addressing is maintained internally by both ports so that data are stored and recovered sequentially by the FIFO without attention from outside logic. An advanced algorithm is utilized in the V61C01 and V61C02 that eliminates the "bubble through" time necessary in some FIFOs.

"Full Flag" ($\overline{FF}$) and "Empty Flag" ($\overline{EF}$) are generated by the device's internal logic and can be used to prevent data underflow and overflow. Expansion capability is built into the FIFOs and allows unlimited expansion in either depth or width with minimal external logic. In addition to the $\overline{FF}$ and $\overline{EF}$ flags, a Half Full or Half Empty flag ($\overline{XO}/\overline{HF}$) indicates the half full or half empty condition when the FIFO is operating in either the unexpanded or the width expanded modes.

Using the internal address pointers, Data (D_0–D_8) is loaded into the device using the Write ($\overline{W}$) pin and read from the device on Data (Q_0–Q_8) using the Read ($\overline{R}$) pin. The minimum Read/Write cycle is 45 ns to support a data rate of over 22 MHz for 9 bits. The 9 bit internal organization of the V61C01 and V61C02 accomodates either internal control or parity bits based on system requirements. If the 9th bit is used for a parity bit, many transmission and reception errors that might be encountered in telecommunications applications can be detected. The retransmission feature of the FIFO can be used to restart an erroneous data transaction by resetting the read address pointer to its inital position with the Retransmit ($\overline{RT}$) signal.

The V61C01 and V61C02 are fabricated using Vitelic's CMOS process for highest speed consistent with best power dissipation characteristics. The FIFO parts are designed for use in applications that require buffering of high-speed asynchronous data channels with simultaneous input and output. Multiprocessor systems and peripheral interface applications are typical of the kinds of requirements that the V61C01 and V61C02 can support.

Package	Sym.	Pin Count
Plastic DIP	P	28
Skinny DIP	S	28



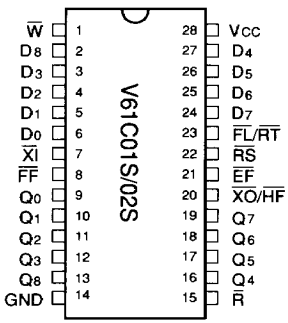
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)					Power	
	P	S	35[1]	40	50	65	80	Low	Std.
0°C to 70°C	•	•	•	•	•	•	•	•	•

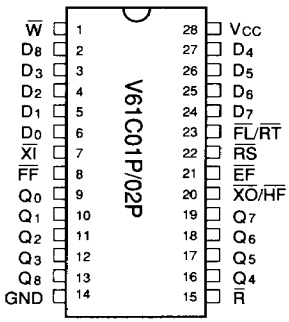
[1] V61C01 and V61C01L only.

V61C01/02 Rev. 01 6/90

Plastic DIP (300 MIL)
PIN CONFIGURATION
Top View

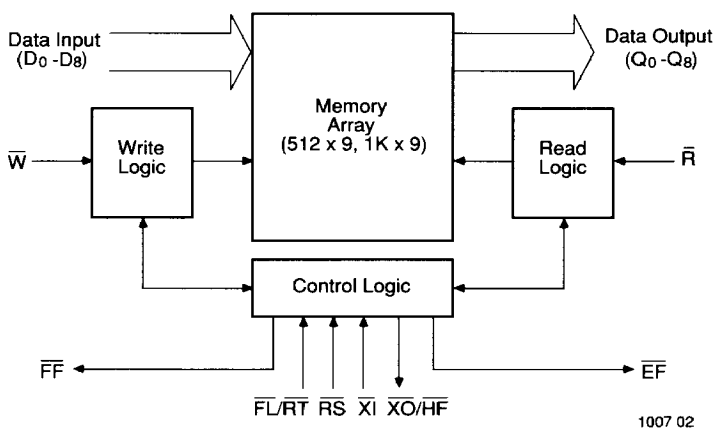


Plastic DIP (600 MIL)
PIN CONFIGURATION
Top View



1007 01

Block Diagram



1007 02

Absolute Maximum Ratings

Ambient Temperature
Under Bias ..... -40°C to +85°C
Storage Temperature
(Plastic) ..... -65°C to +150°C
Voltage on Any Pin
Relative to V_{SS} ..... -0.5 to 7.0Vdc
Data Out Current ..... 50 mA
Power Dissipation ..... 1.0 W

AC Test Conditions

Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5 ns
Input Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

NOTE:
1. Operation at or near absolute maximum ratings can affect device reliability.

Recommended Operating Conditions

(T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Level	2.2	—	6.0	V
V_{IL}	Input Low Level	-1.0	—	0.8	V

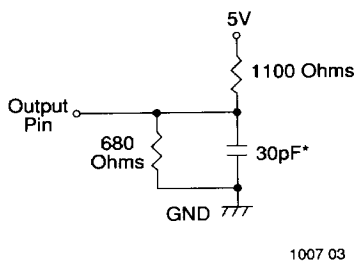


Figure 1.
* Includes test fixture and scope capacitance

Capacitance*

T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Conditions	Max.	Unit	Note
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF	1
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF	

* These parameters are sampled and not 100% tested.

NOTE:
1. Output is deselected.

D.C. Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage	V_{DD} = 5.5V, V_{IN} = 0 to V_{DD}	—	—	10	µA
I_{LO}	Output Leakage	$\overline{R} \geq V_{IH}$, V_{OUT} = 0 to V_{DD}	—	—	10	µA
V_{OH}	Output High Voltage	Logic "1", I_{OUT} = -2 mA	2.4	—	—	V
V_{OL}	Output Low Voltage	Logic "0", I_{OUT} - 8 mA	—	—	0.4	V
I_{DD1}	Operating Current	Outputs Open	—	40	80	mA
I_{DD2}	Standby Current	$\overline{R}$, $\overline{W}$, $\overline{RS}$, $\overline{FL}/\overline{RT} \geq V_{IH}$	—	3	5	mA
I_{DD3L}	Power Down Current (L part only)	All Inputs >V_{DD} - .2 Outputs Open	—	3	100	µA
I_{DD3S}	Power Down Current (standard part)	All Inputs ≥ V_{DD} - .2 Outputs Open	—	2	5	mA

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AC Electrical Characterisitcs Over the Operating Temperature and Supply Voltage Range for V61C01/V61C02

		35[1]		40		50		65		80		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_S	Shift Frequency	—	22.2	—	20	—	15	—	12.5	—	10	MHz
t_{RC}	Read Cycle Time	45	—	50	—	65	—	80	—	100	—	ns
t_A	Access Time	—	35	—	40	—	50	—	65	—	80	ns
t_{RR}	Read Recovery Time	10	—	10	—	15	—	15	—	20	—	ns
t_{RPW}	Read Pulse Width	35	—	40	—	50	—	65	—	80	—	ns
t_{RLZ}	Read Pulse Low to Low-Z	5	—	5	—	10	—	10	—	10	—	ns
t_{DV}	Data Valid From Read Pulse High	5	—	5	—	10	—	10	—	10	—	ns
t_{RHZ}	Read Pulse High to High-Z	—	20	—	25	—	30	—	30	—	30	ns
t_{WC}	Write Cycle Time	45	—	50	—	65	—	80	—	100	—	ns
t_{WPW}	Write Pulse Width	35	—	40	—	50	—	65	—	80	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	15	—	15	—	20	—	ns
t_{DS}	Data Set-Up Time	12	—	15	—	20	—	25	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	5	—	5	—	5	—	ns
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	80	—	100	—	ns
t_{RS}	Reset Pulse Width	35	—	40	—	50	—	65	—	80	—	ns
t_{RSS}	Reset Set-Up Time	35	—	40	—	50	—	65	—	80	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	15	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	80	—	100	—	ns
t_{RT}	Retransmit Pulse Width	35	—	40	—	50	—	65	—	80	—	ns
t_{RTS}	Retransmit Set-Up Time	35	—	40	—	50	—	65	—	80	—	ns
t_{RTR}	Rretransmit Recovery Time	10	—	10	—	15	—	15	—	20	—	ns
t_{EFL}	Reset to Empty Flag Low	—	45	—	50	—	65	—	80	—	100	ns
t_{HFH}, t_{FFH}	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	45	—	50	—	65	—	80	—	100	ns
t_{REF}	Read Low to Empty Flag Low	—	30	—	30	—	35	—	45	—	60	ns
t_{RFF}	Read High to Full Flag High	—	30	—	30	—	35	—	45	—	60	ns
t_{RPE}	Read Pulse Width After $\overline{EF}$ High	35	—	40	—	50	—	65	—	80	—	ns
t_{WEF}	Write High to $\overline{EF}$ High	—	30	—	30	—	35	—	45	—	60	ns
t_{WFF}	Write Low to $\overline{FF}$ Low	—	30	—	30	—	35	—	45	—	60	ns
t_{WHF}	Write Low to $\overline{HF}$ Low	—	45	—	50	—	65	—	80	—	100	ns
t_{RHF}	Read High to $\overline{HF}$ High	—	45	—	50	—	65	—	80	—	100	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	35	—	40	—	50	—	65	—	80	—	ns

[1]V61C01 and V61C01L only.

Table 3. Single Device Configuration/Width Expansion Mode

	Inputs			Internal Status		Outputs		
Mode	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	**Read Pointer**	**Write Pointer**	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	(X)	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	(X)	(X)	(X)
Read/Write	1	1	0	Increment*	Increment*	(X)	(X)	(X)

* Pointer will increment if flag is high. (X) = Don't Care or Undefined.

Figure 2. V61C01 or V61C02 Operating in Single Device Mode with a Capacity of 512 x 9 or 1024 x 9

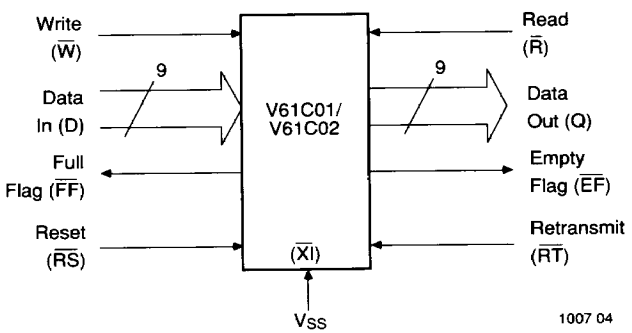

Figure 3. V61C01 or V61C02 in the Width Expansion Mode with a Capacity of 512 X 18 or 1024 X 18

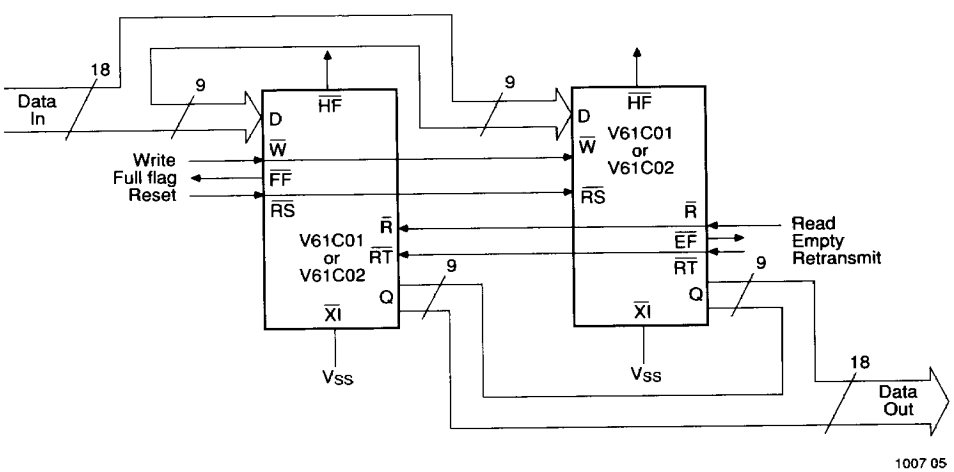

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Table 4. Depth Expansion/Compound Expansion Mode

	Inputs			Internal Status		Outputs	
Mode	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	**Read Pointer**	**Write Pointer**	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	* *	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	* *	Location Zero	Location Zero	0	1
Read/Write	1	(X)	* *	(X)	(X)	(X)	(X)

* * $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
(X) indicates "DON'T CARE" or "UNDEFINED".

Figure 4. V61C01 or V61C02 in the Depth Expansion Mode.

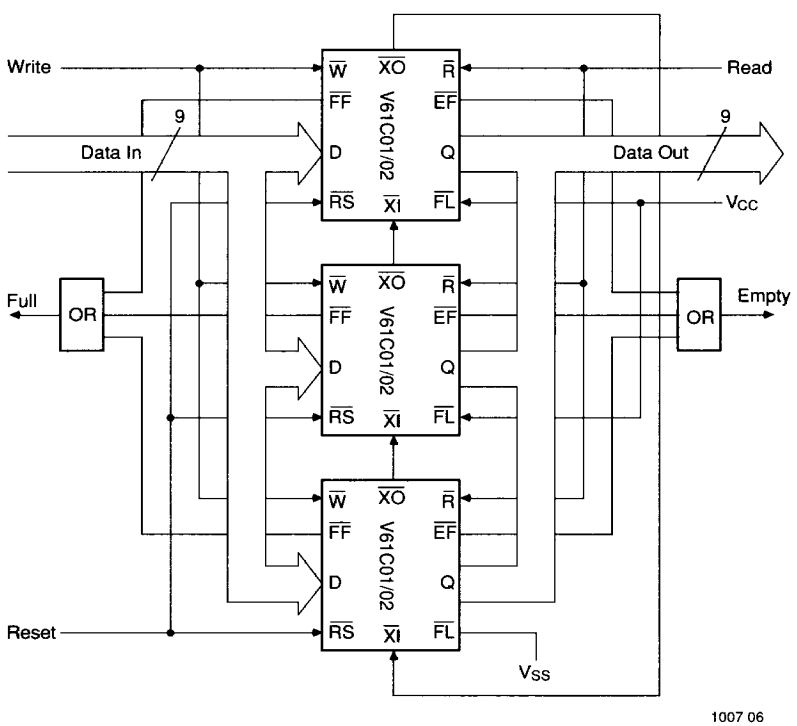


Figure 5. V61C01 or V61C02 in the Compound Expansion Mode.

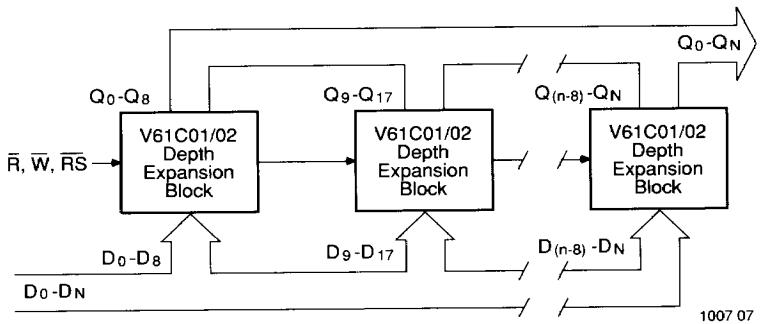


Figure 6. V61C01 or V61C02 in the Bidirectional Mode.

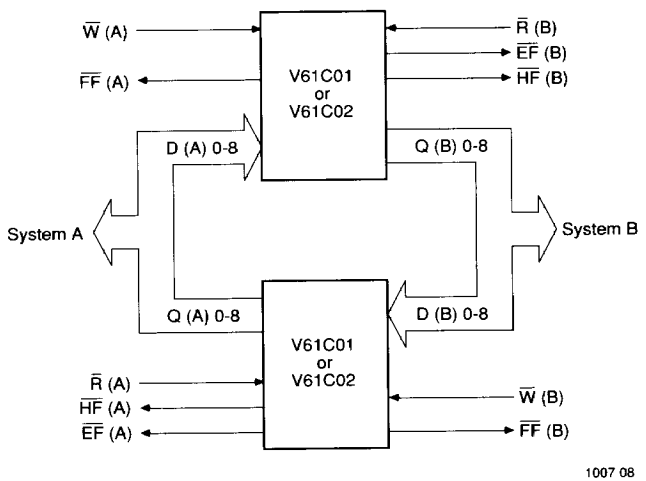


Figure 7. Read Data Flow-Through Mode.

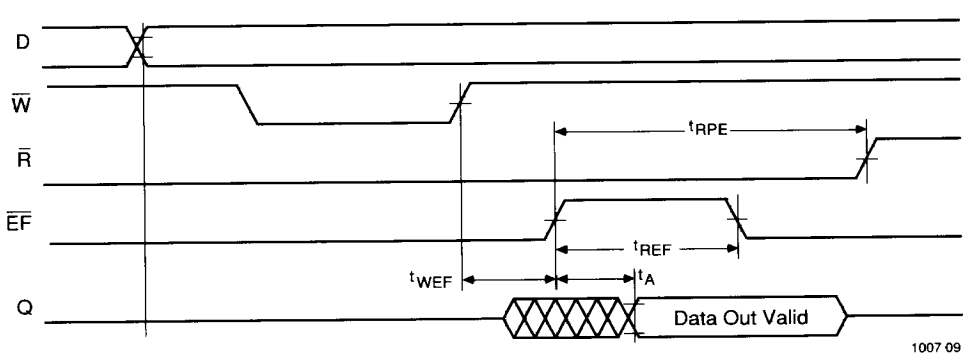
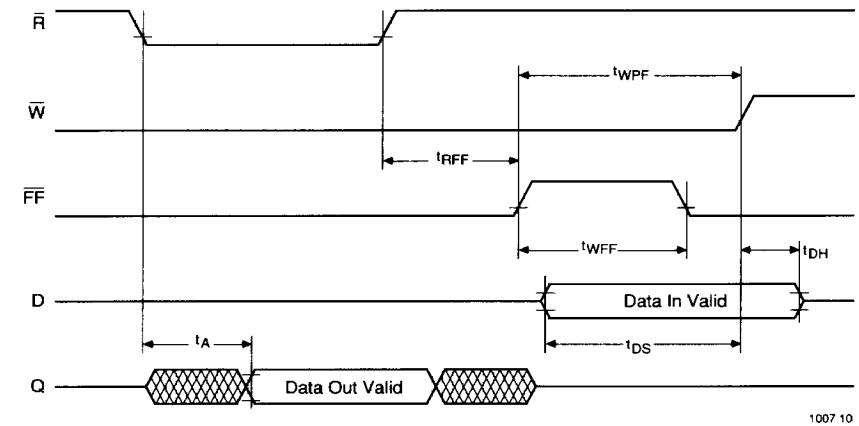
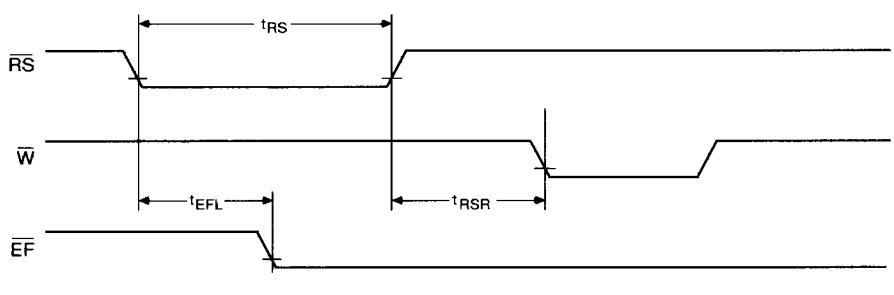


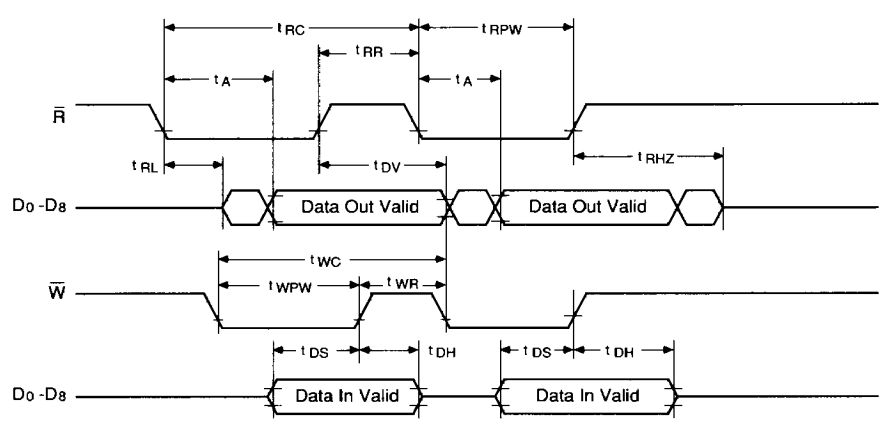
Figure 8. Write Data Flow-Through Mode.



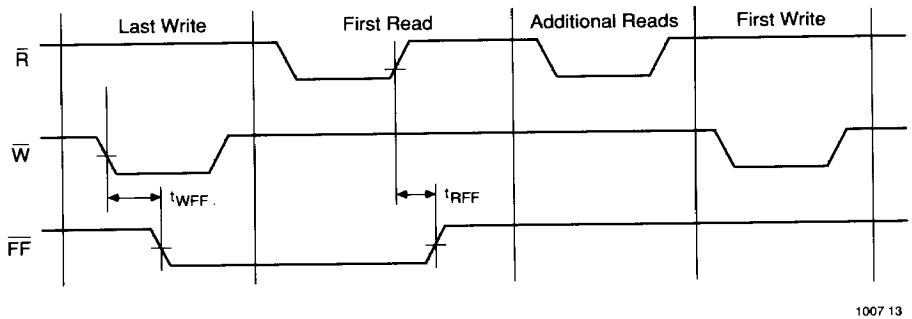
Reset Timing



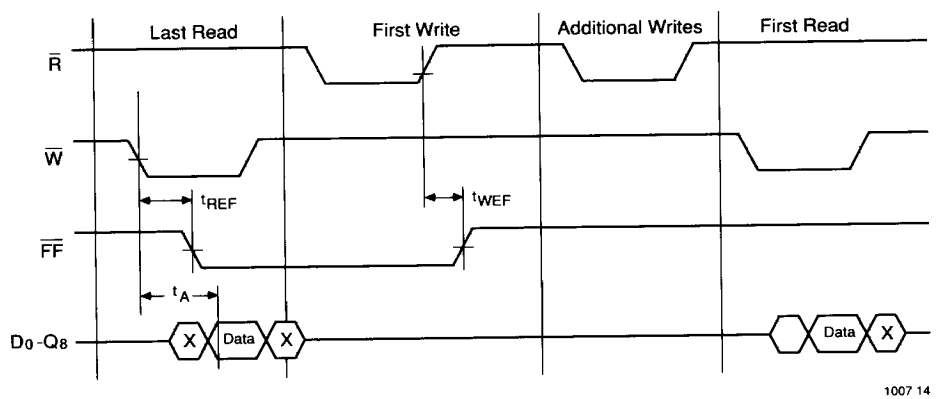
Asynchronous Write/Read Operation



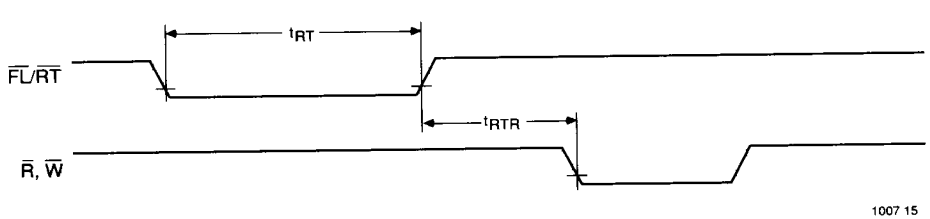
Full Flag from Last Write to First Read



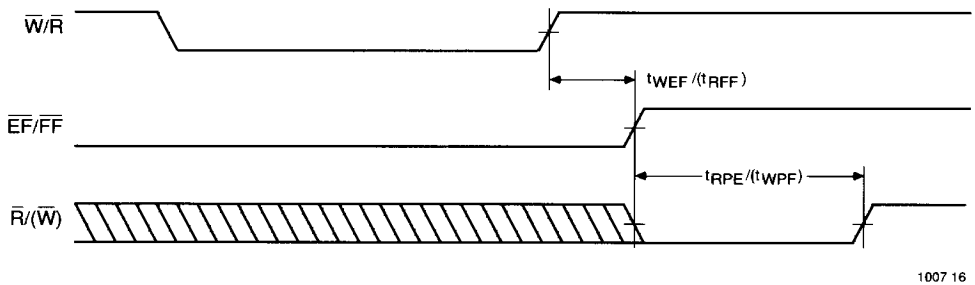
Empty Flag from Last Read to First Write



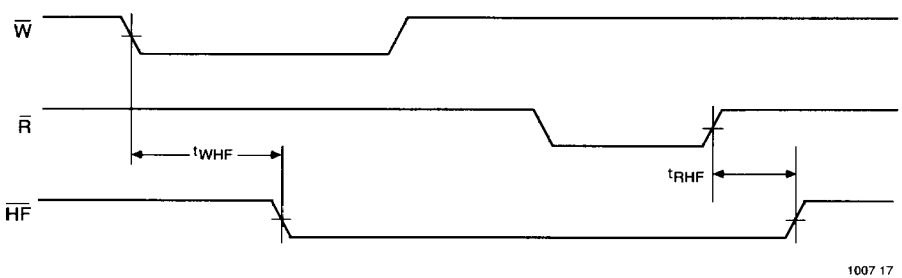
Retransmit Operation



Empty Flag/Full Flag Timing



Half-Full Flag Timing



Application and Functional Information

The V61C01/02 can operate in either single device or expanded mode. Expansion can be accomplished in either width (wider word), depth (more words) or combined width-depth. Because of the extremely versatile control and expansion signals, very little external logic is required to expand the V61C01/02 and minimal performance degradation results.

In the unexpanded or single device mode, a single V61C01 or V61C02 can be used if application requirements are met with either 512 X 9 bit or 1024 X 9 bit organization. In order to place the V61C01/02 in single device mode, the "Expansion In" ($\overline{XI}$) control input must be either grounded or connected to a "low" logic level. The "Expansion Out" ($\overline{XO}$) function is not required in this mode and is shared with the "Half Full Flag" ($\overline{HF}$) to indicate the "Half Full" ("Half Empty") condition of the FIFO. Figure 2 depicts a V61C01/02 connected in the unexpanded or single device mode.

In the width expansion mode, the V61C01/02 can accomodate arbitrarily wide words simply by cascading devices and driving control input lines (Write, Read, Reset, Retransmit, Expansion In) together. The data lines for the wider word are composed of the individual devices' "Data Out" and "Data In" lines concatenated. The status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) are generated at each device and may be sensed at any convenient point. When devices are connected to form wider words, the status flags must not be connected together. Figure 3 depicts two V61C01/02 devices connected to form an 18-bit word. Table 3 indicates the truth table operation of the width expansion mode.

Depth expansion of the V61C01/02 is facilitated by the control signals present on each device. As required by an application, the depth (number of words) can be expanded arbitrarily in 512 or 1024 word increments with a minimum of external logic and performance degradation. It is possible to mix V61C01 and V61C02 devices when expanding in depth.

In order to expand in depth, the following rules and limitations apply:

1. The first device must be designed by grounding the "First Load" ($\overline{FL}$) input.
2. The $\overline{FL}$ input of all other devices must be tied "High".
3. The "Expansion Out" ($\overline{XO}$) pin of each device must be connected to "Expansion In" ($\overline{XI}$) of the next device beginning with the first device and progressing in order.
4. An overall "Full Flag" and "Empty Flag" must be generated by the use of external logic. This is accomplished by producing an "AND" function of the asserted state of the individual flags. The flags are produced in a negative logic sense and therefore, the correct function is produced by a logic "OR" gate as shown in Figure 4. Table 4 contains a truth table for depth expansion.
5. When FIFOs are expanded in depth, "Retransmit" ($\overline{RT}$) and the "Half Full" ($\overline{HF}$) flag are not available.

Using the techniques described in the width and depth expansion modes, the V61C01 and V61C02 can be expanded in both width and depth. A block diagram depicting a compound expansion is shown in Figure 5. Table 4 indicates the truth table operation of the FIFO in the compound expansion mode.

For applications that require buffering of data in both directions, the V61C01 and V61C02 can be connected as a bidirectional FIFO. When the bidirectional mode is mechanized, two systems, each READ/WRITE capable, can be connected and data can be buffered in either direction.

When connecting the V61C01 and V61C02 in the bidirectional FIFO mode, care must be taken to sense the appropriate flags. In all cases, a device that is writing data to the FIFO must monitor the $\overline{FF}$ flag and a device that is reading data must monitor the $\overline{EF}$ flag. The mechanization of a bidirectional FIFO is depicted in Figure 6.

The V61C01 and V61C02 offer two modes where data appear to "flow through." In the read flow-through mode, a single word of data may be read from the FIFO immediately following the writing of the first word of data. In the write flow-through mode, a single word of data may be written into the FIFO immediately following the reading of one data word from a FIFO that is completely filled. These modes are depicted with timing diagrams in figures 7 and 8.

Glossary of Signals and Description

Inputs:

Data In (D_0–D_8)

9-bit wide input data bus

Controls:

Reset ($\overline{RS}$)

The device is asynchronously reset when the $\overline{RS}$ input is asserted (pulled "low"). At reset time, both

the Read and Write Pointers are set to the first FIFO location. After Power-Up, a Reset is required before a Write can take place. Both Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be "high" during Reset. The assertion of $\overline{RS}$ will cause the Half Full Flag ($\overline{HF}$) to assume a "high" logic state.

Write Enable ($\overline{W}$)

The falling edge of ($\overline{W}$) will initiate a write cycle if the Full Flag ($\overline{FF}$) is not set (low). Data setup and hold times must be observed with respect to the rising edge of Write Enable ($\overline{W}$). Data that are written into the FIFO are written into sequential locations in the RAM array regardless of any Read operation that might be underway.

When half of the memory is filled by writing data, and at the next falling edge of $\overline{W}$, the Half Full Flag ($\overline{HF}$) will be set "low" and will remain "low" as long as the FIFO is half or more full. When a Read operation causes the FIFO to be less than half full, the Half Full Flag ($\overline{HF}$) will be reset on the rising edge of Read Enable ($\overline{R}$).

When the FIFO is full and further Write operations would cause a data overflow condition, the Full Flag ($\overline{FF}$) will be asserted "low" and further write operations will be inhibited until space is made available for writing by either a Read operation or a Reset. If a Full condition exists, and a Read operation takes place, the Full Flag ($\overline{FF}$) will go "high" following the rising edge of Read Enable ($\overline{R}$) by t_{RFF}. A write operation can begin after the Full Flag ($\overline{FF}$) rises.

Read Enable ($\overline{R}$)

A falling edge of Read Enable ($\overline{R}$) initiates a Read cycle if the Empty Flag ($\overline{EF}$) is not asserted "low". Data read from the FIFO is on a First-In-First-Out basis regardless of any Write operations that might be underway. The Read Enable ($\overline{R}$) control signal acts as an Output Enable for the Data Out lines, Q_0–Q_8, and will cause the Data Out lines to assume a High-Impedance state when it is "high". When the FIFO has been emptied, the Empty Flag ($\overline{EF}$) will go "low" at t_{REF} following the beginning of the Read Cycle and will inhibit further Read operations until a Write operation has taken place. During the FIFO Empty condition, the Data Out lines will assume a High-Impedance state. Once a Write operation has been accomplished, the Empty Flag ($\overline{EF}$) will return "high" at t_{WEF} after the rising edge of Write Enable ($\overline{W}$) allowing a Read operation to begin.

First Load/Retransmit ($\overline{FL}$/$\overline{RT}$)

In the multiple device mode, this input, when grounded or brought "low", indicates the first device to be loaded. In the single device mode, the input is used to initiate the Retransmit function. The single device mode is indicated by the grounding of the Expansion In ($\overline{XI}$) input.

When the Retransmit ($\overline{RT}$) signal is pulsed "low", the Retransmit function is enabled. The internal Read Pointer is set to the first FIFO location without changing the Write Pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be "high" during initiation of Retransmit. This function is most useful when data transmissions of less than 512 or 1024 words are made and error checking indicates a transmission error. The Retransmit Function cannot be used in the depth expansion mode and will affect the Half Full Flag ($\overline{HF}$) because of the change in the read Pointer that occurs upon initiation of the Retransmit function.

Expansion In ($\overline{XI}$)

This dual purpose input indicates that the device is in the single device mode when it is grounded. In the depth expansion mode it is connected to the Expansion Out ($\overline{XO}$) of a previous device in "daisy chain" fashion.

Outputs:

Empty Flag ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will be asserted "low" when the condition of the Read Pointer and Write Pointer indicates that the device is empty.

Full Flag ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will be asserted "low" when the condition of the Read Pointer and Write Pointer indicates that there is no more room in the FIFO for data to be written.

Expansion Out/Half Full Flag ($\overline{XO}$/$\overline{HF}$)

In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output indicates that the FIFO is half full (see discussion under Write Enable ($\overline{W}$)).

In the multiple device mode and when Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of a previous device, $\overline{XO}$ outputs a signal to the next device in line when the last location is written to enable the writing of the next data word into the next FIFO in line.

Data Outputs (Q0–Q8)

9-bit wide output data bus enabled by Read Enable ($\overline{R}$) in an active (low) state.