



VN920-E VN920B5-E / VN920SO-E

HIGH SIDE DRIVER

Table 1. General Features

Type	R _{DS(on)}	I _{OUT}	V _{CC}
VN920-E VN920B5-E VN920SO-E	16mΩ	30 A	36 V

- CMOS COMPATIBLE INPUT
- PROPORTIONAL LOAD CURRENT SENSE
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUTDOWN
- CURRENT LIMITATION
- PROTECTION AGAINST LOSS OF GROUND AND LOSS OF V_{CC}
- VERY LOW STAND-BY POWER DISSIPATION
- REVERSE BATTERY PROTECTION (*)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

DESCRIPTION

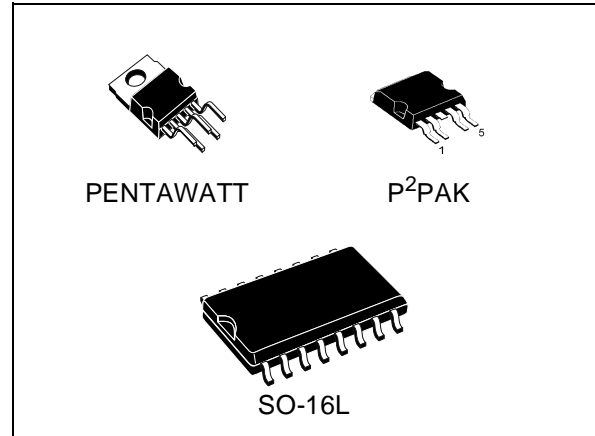
The VN920-E, VN920B5-E, VN920SO-E is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Table 2. Order Codes

Package	Tube	Tape and Reel
PENTAWATT	VN920-E	-
P ² PAK	VN920B5-E	VN920B5TR-E
SO-16L	VN920SO-E	VN920SOTR-E

Note: (*) See application schematic at page 9.

Figure 1. Package



Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. The device integrates an analog current sense output which delivers a current proportional to the load current. Device automatically turns off in case of ground pin disconnection.

Figure 2. Block Diagram

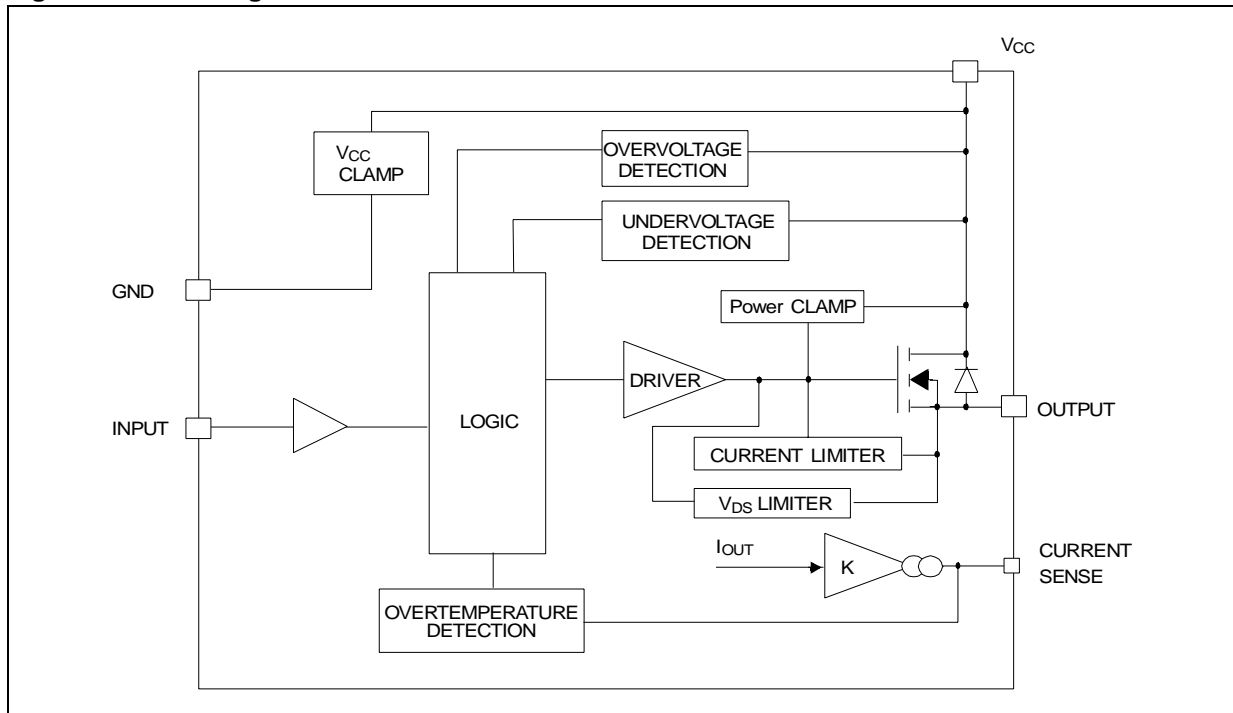


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value			Unit
		PENTAWATT	P ² PAK	SO-16L	
V _{CC}	DC Supply Voltage	41			V
-V _{CC}	Reverse DC Supply Voltage	- 0.3			V
-I _{GND}	DC Reverse Ground Pin Current	- 200			mA
I _{OUT}	DC Output Current	Internally Limited			A
-I _{OUT}	Reverse DC Output Current	- 21			A
I _{IN}	DC Input Current	+/- 10			mA
V _{CSSENSE}	Current Sense Maximum Voltage	-3			V
		+15			V
V _{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF)				
	- INPUT	4000			V
	- CURRENT SENSE	2000			V
	- OUTPUT	5000			V
	- V _{CC}	5000			V
E _{MAX}	Maximum Switching Energy (L=0.25mH; R _L =0Ω; V _{bat} =13.5V; T _{jstart} =150°C; I _L =45A)		364	352	mJ
P _{TOT}	Power Dissipation T _C ≤25°C	96.1	96.1	8.3	W
T _j	Junction Operating Temperature	Internally limited			°C
T _c	Case Operating Temperature	- 40 to 150			°C
T _{STG}	Storage Temperature	- 55 to 150			°C

Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins

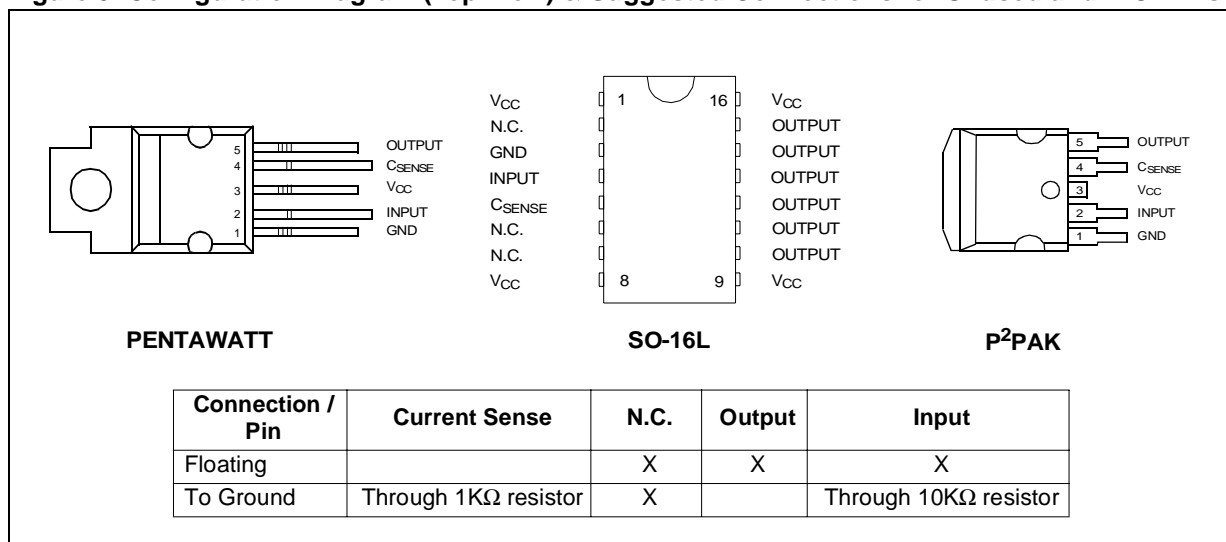


Figure 4. Current and Voltage Conventions

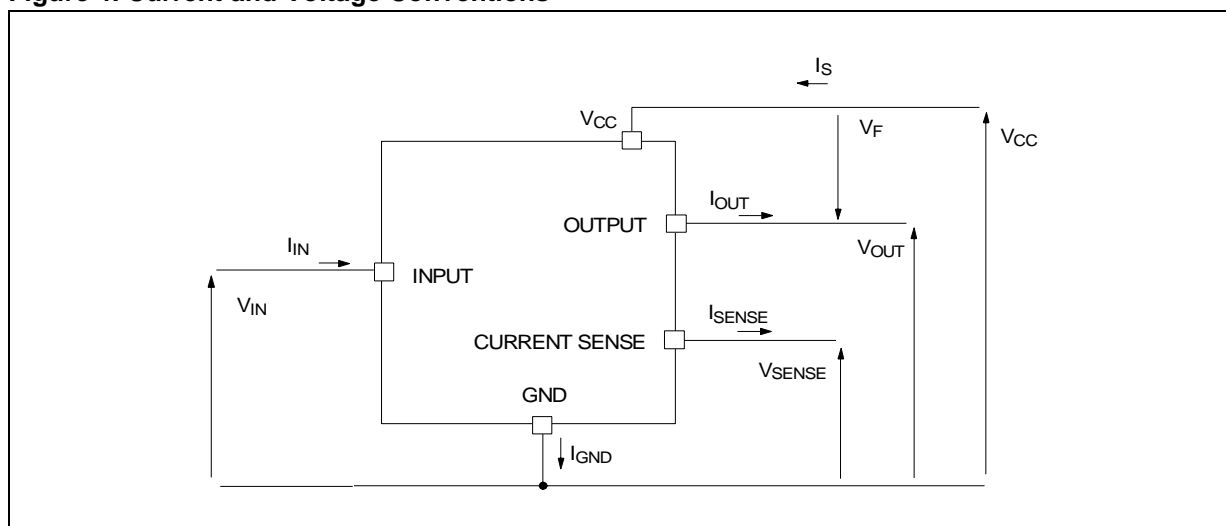


Table 4. Thermal Data

Symbol	Parameter	Max	Value			Unit
			PENTAWATT	P ² PAK	SO-16L	
R _{thj-case}	Thermal Resistance Junction-case	Max	1.3	1.3		°C/W
R _{thj-lead}	Thermal Resistance Junction-lead	Max			15	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	61.3	51.3 ⁽¹⁾	65 ⁽³⁾	°C/W
				37 ⁽²⁾	48 ⁽⁴⁾	°C/W

⁽¹⁾ When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35μm thick).

⁽²⁾ When mounted on a standard single-sided FR-4 board with 6cm² of Cu (at least 35μm thick).

⁽³⁾ When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35μm thick) connected to all V_{CC} pins.

⁽⁴⁾ When mounted on a standard single-sided FR-4 board with 6cm² of Cu (at least 35μm thick) connected to all V_{CC} pins.

ELECTRICAL CHARACTERISTICS ($8V < V_{CC} < 36V$; $-40^{\circ}C < T_j < 150^{\circ}C$ unless otherwise specified)

Table 5. Power

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Supply Voltage		5.5	13	36	V
V_{USD}	Undervoltage Shut-down		3	4	5.5	V
V_{OV}	Overvoltage Shut-down		36			V
R_{ON}	On State Resistance	$I_{OUT}=10A$; $T_j=25^{\circ}C$			16	$m\Omega$
		$I_{OUT}=10A$			32	$m\Omega$
		$I_{OUT}=3A$; $V_{CC}=6V$			55	$m\Omega$
V_{clamp}	Clamp Voltage	$I_{CC}=20mA$ (See note 1)	41	48	55	V
I_S	Supply Current	Off State; $V_{CC}=13V$; $V_{IN}=V_{OUT}=0V$		10	25	μA
		Off State; $V_{CC}=13V$; $V_{IN}=V_{OUT}=0V$; $T_j=25^{\circ}C$		10	20	μA
		On State; $V_{CC}=13V$; $V_{IN}=5V$; $I_{OUT}=0A$; $R_{SENSE}=3.9K\Omega$			5	mA
$I_{L(off1)}$	Off State Output Current	$V_{IN}=V_{OUT}=0V$	0		50	μA
$I_{L(off2)}$	Off State Output Current	$V_{IN}=0V$; $V_{OUT}=3.5V$	-75		0	μA
$I_{L(off3)}$	Off State Output Current	$V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=125^{\circ}C$			5	μA
$I_{L(off4)}$	Off State Output Current	$V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=25^{\circ}C$			3	μA

Note: 1. V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

Table 6. Switching ($V_{CC} = 13V$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$R_L=1.3\Omega$ (see figure 6)		50		μs
$t_{d(off)}$	Turn-off Delay Time	$R_L=1.3\Omega$ (see figure 6)		50		μs
$dV_{OUT}/dt_{(on)}$	Turn-on Voltage Slope	$R_L=1.3\Omega$ (see figure 6)		See relative diagram		$V/\mu s$
$dV_{OUT}/dt_{(off)}$	Turn-off Voltage Slope	$R_L=1.3\Omega$ (see figure 6)		See relative diagram		$V/\mu s$

Table 7. Logic Input

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level				1.25	V
I_{IL}	Low Level Input Current	$V_{IN}=1.25V$	1			μA
V_{IH}	Input High Level		3.25			V
I_{IH}	High Level Input Current	$V_{IN}=3.25V$			10	μA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
V_{ICL}	Input Clamp Voltage	$I_{IN}=1mA$	6	6.8	8	V
		$I_{IN}=-1mA$		-0.7		V

ELECTRICAL CHARACTERISTICS (continued)**Table 8. V_{CC} - Output Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _F	Forward on Voltage	-I _{OUT} =2A; T _J =150°C			0.6	V

Table 9. Protections (see note 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T _{TSD}	Shut-down Temperature		150	175	200	°C
T _R	Reset Temperature		135			°C
T _{hyst}	Thermal Hysteresis		7	15		°C
I _{lim}	DC Short Circuit Current	V _{CC} =13V 5V<V _{CC} <36V	30	45	75 75	A A
V _{demag}	Turn-off Output Clamp Voltage	I _{OUT} =2A; V _{IN} =0V; L=6mH	V _{CC} -41	V _{CC} -48	V _{CC} -55	V
V _{ON}	Output Voltage Drop Limitation	I _{OUT} =1A; T _J =-40°C....+150°C		50		mV

Note: 1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current Sense (9V≤V_{CC}≤16V) (See Fig. 5)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} =1A; V _{SENSE} =0.5V; T _J = -40°C...150°C	3300	4400	6000	
dK ₁ /K ₁	Current Sense Ratio Drift	I _{OUT} =1A; V _{SENSE} =0.5V; T _J = -40°C...+150°C	-10		+10	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} =10A; V _{SENSE} =4V; T _J =-40°C T _J =25°C...150°C	4200 4400	4900 4900	6000 5750	
dK ₂ /K ₂	Current Sense Ratio Drift	I _{OUT} =10A; V _{SENSE} =4V; T _J =-40°C...+150°C	-8		+8	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} =30A; V _{SENSE} =4V; T _J =-40°C T _J =25°C...150°C	4200 4400	4900 4900	5500 5250	
dK ₃ /K ₃	Current Sense Ratio Drift	I _{OUT} =30A; V _{SENSE} =4V; T _J =-40°C...+150°C	-6		+6	%
I _{SENSE0}	Analog Sense Leakage Current	V _{CC} =6...16V; I _{OUT} =0A; V _{SENSE} =0V; T _J =-40°C...+150°C	0		10	μA
V _{SENSE}	Max Analog Sense Output Voltage	V _{CC} =5.5V; I _{OUT} =5A; R _{SENSE} =10KΩ V _{CC} >8V; I _{OUT} =10A; R _{SENSE} =10KΩ	2 4			V V
V _{SENSEH}	Sense Voltage in Overtemperature conditions	V _{CC} =13V; R _{SENSE} =3.9KΩ		5.5		V
R _{VSENSEH}	Analog Sense Output Impedance in Overtemperature Condition	V _{CC} =13V; T _J >T _{TSD} ; Output Open		400		Ω
t _{DSENSE}	Current sense delay response	to 90% I _{SENSE} (see note 2)			500	μs

Note: 2. current sense signal delay after positive input slope.

Figure 5. I_{OUT}/I_{SENSE} versus I_{OUT}

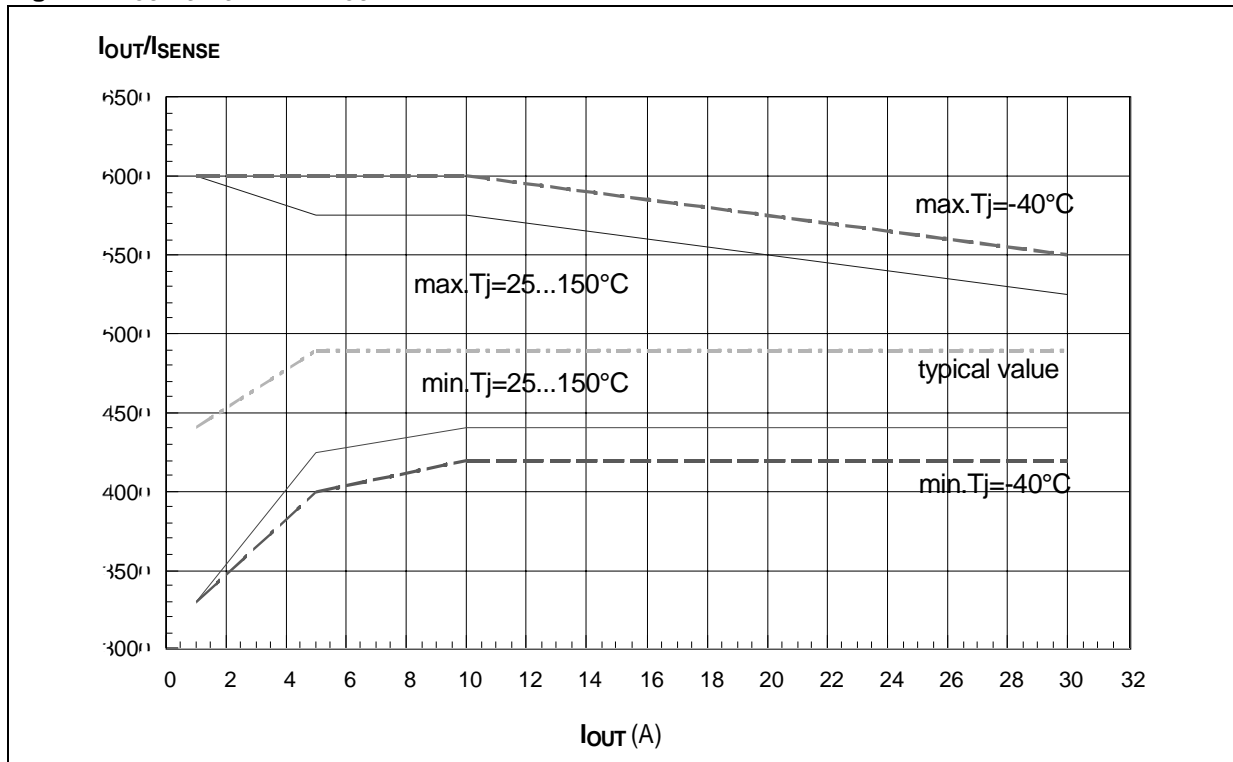


Figure 6. Switching Characteristics (Resistive load $R_L = 1.3\Omega$)

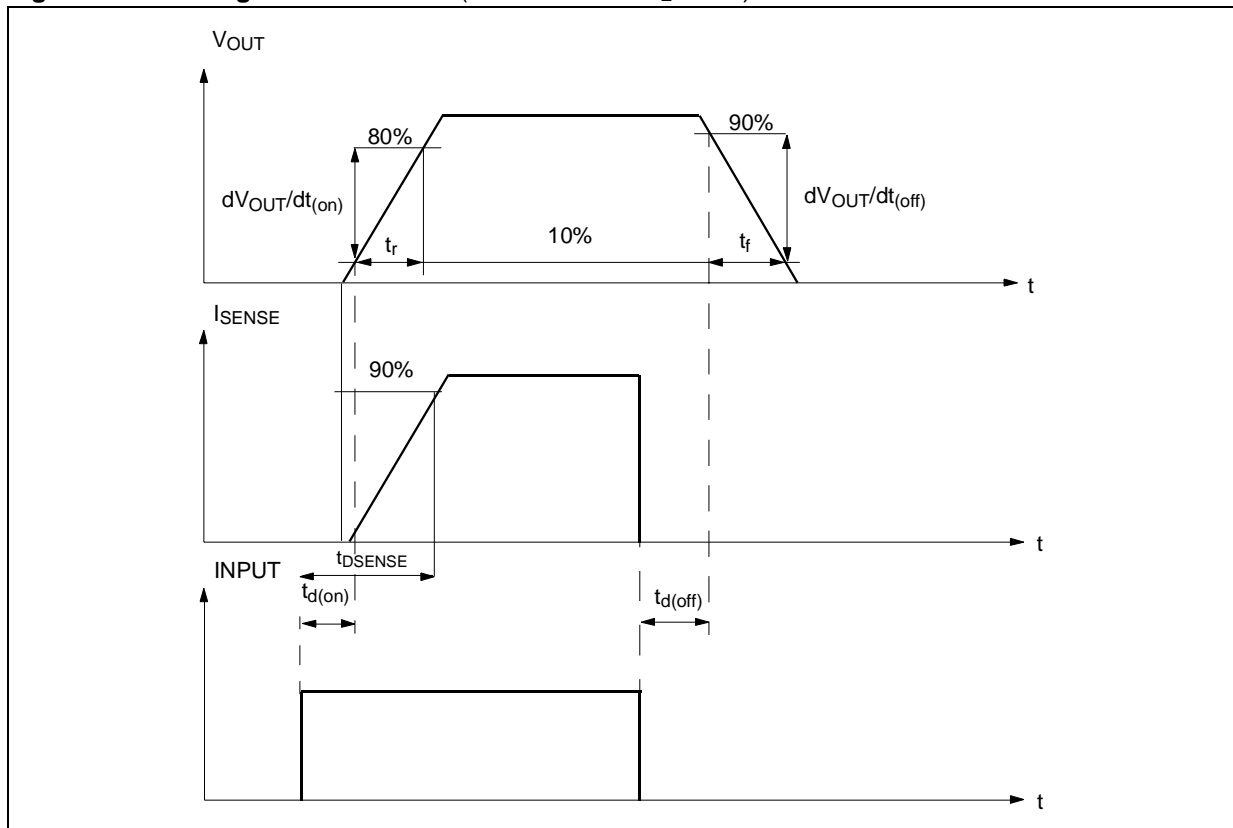


Table 11. Truth Table

CONDITIONS	INPUT	OUTPUT	SENSE
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Overvoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	$(T_j < T_{TSD}) 0$
	H	L	$(T_j > T_{TSD}) V_{SENSEH}$
Short circuit to V_{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

Table 12. Electrical Transient Requirements On V_{CC} Pin

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μ s 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μ s 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Waveforms

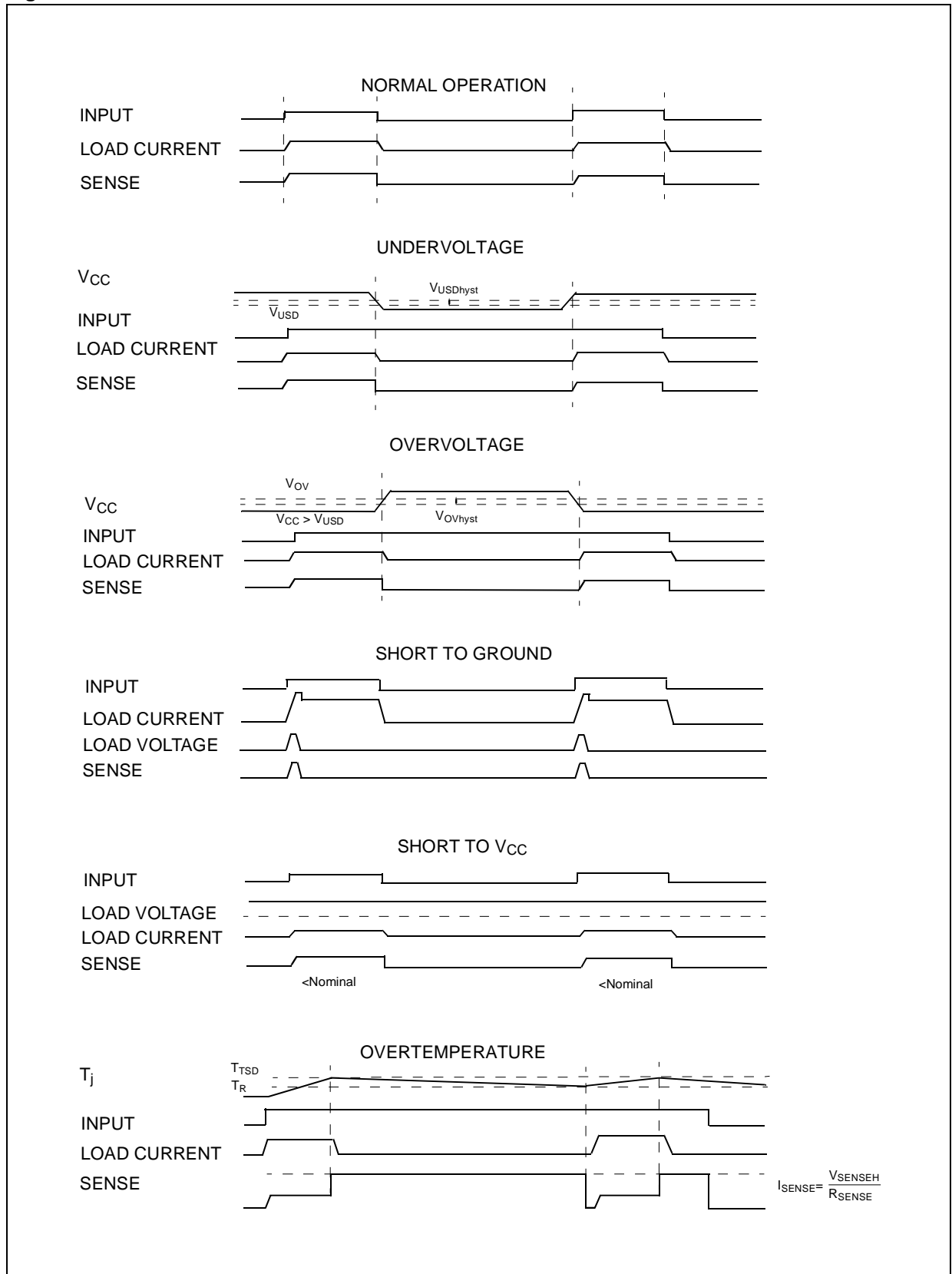
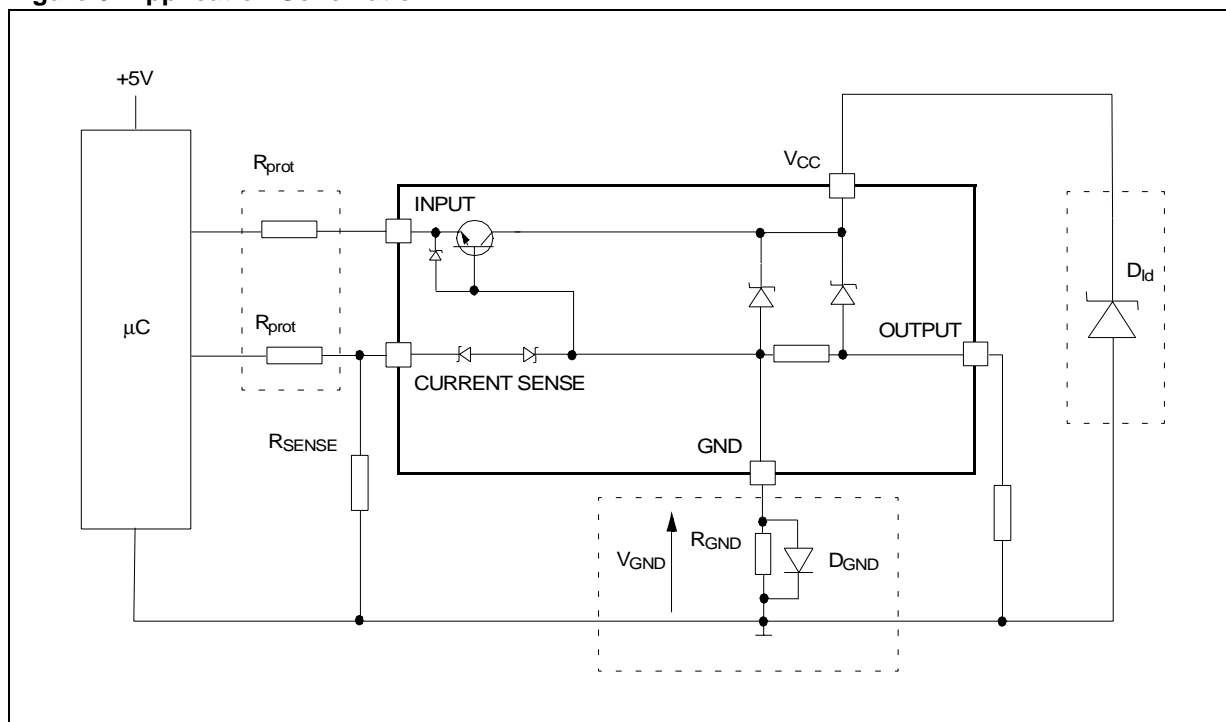


Figure 8. Application Schematic



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (RGND only). This can be used with any type of load.

The following is an indication on how to dimension the RGND resistor.

- 1) $R_{GND} \leq 600mV / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where -IGND is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device’s datasheet.

Power Dissipation in RGND (when VCC<0: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where IS(on)max becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the RGND will produce a shift (IS(on)max * RGND) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same RGND.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (DGND) in the ground line.

A resistor (RGND=1kΩ) should be inserted in parallel to DGND if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT line is also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT pin is to leave it unconnected, while unused SENSE pin has to be connected to Ground pin.

LOAD DUMP PROTECTION

DId is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds VCC max DC rating. The same applies if the device will be subject to transients on the VCC line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the VCC line, the control pins will be pulled negative. ST suggests to insert a resistor (Rprot) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OHµC} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For VCCpeak= - 100V and I_{latchup} ≥ 20mA; VOHµC ≥ 4.5V
 $5k\Omega \leq R_{prot} \leq 65k\Omega$.

Recommended R_{prot} value is 10kΩ.

Figure 9. Off State Output Current

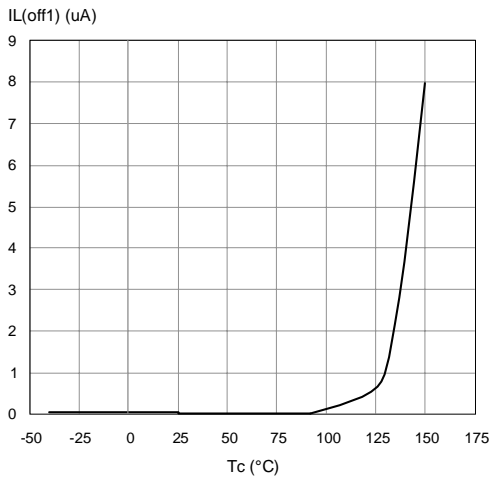


Figure 10. High Level Input Current

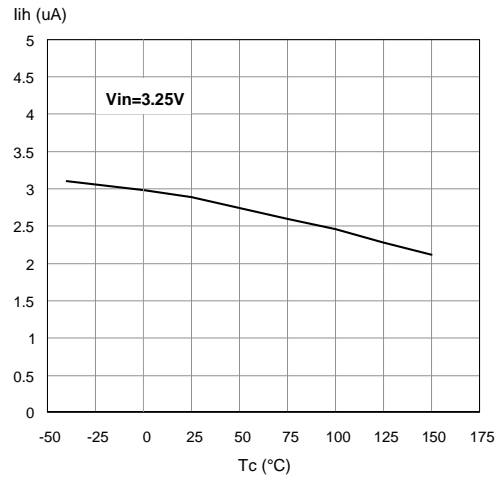


Figure 11. Input Clamp Voltage

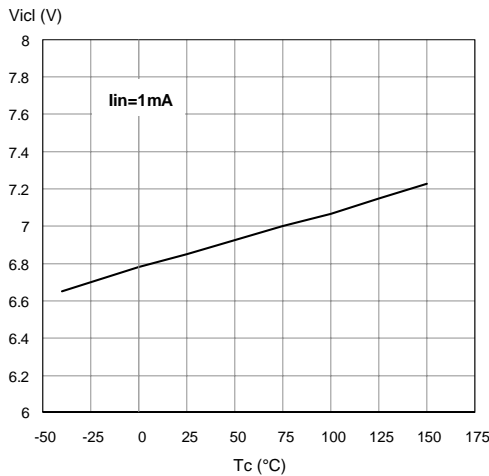


Figure 13. On State Resistance Vs VCC

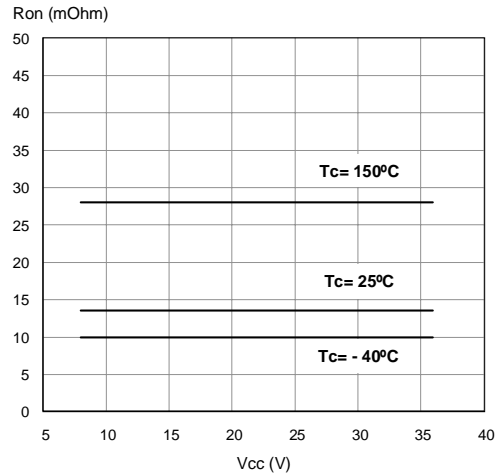


Figure 12. On State Resistance Vs Tcase

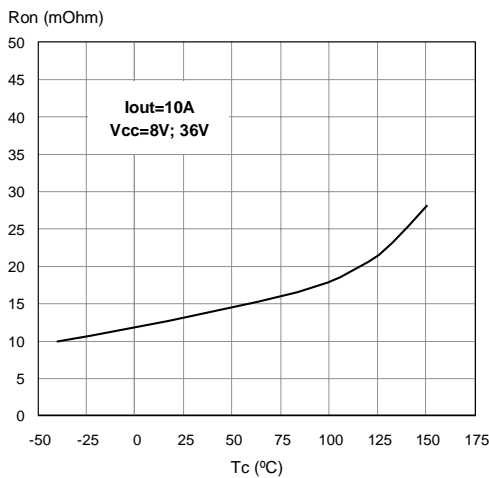


Figure 14. Input High Level

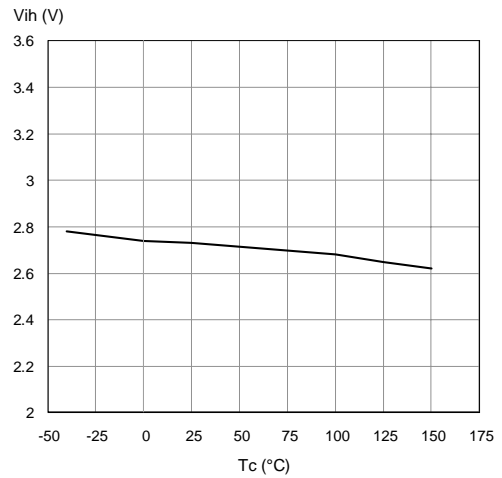


Figure 15. Input Low Level

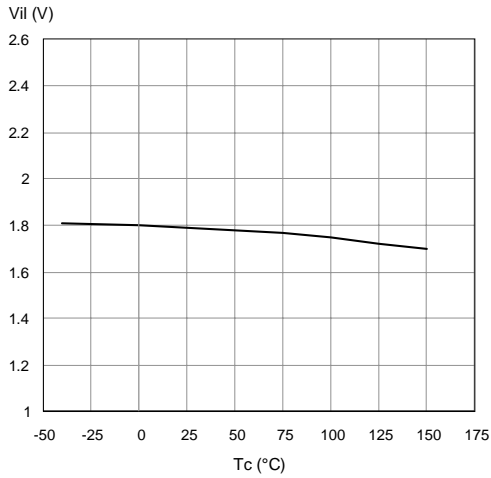


Figure 18. Input Hysteresis Voltage

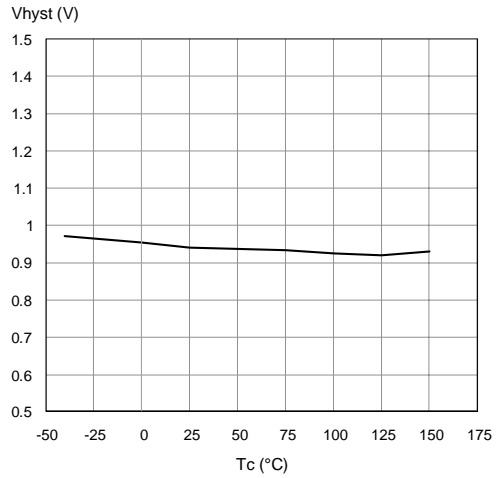


Figure 16. Turn-on Voltage Slope

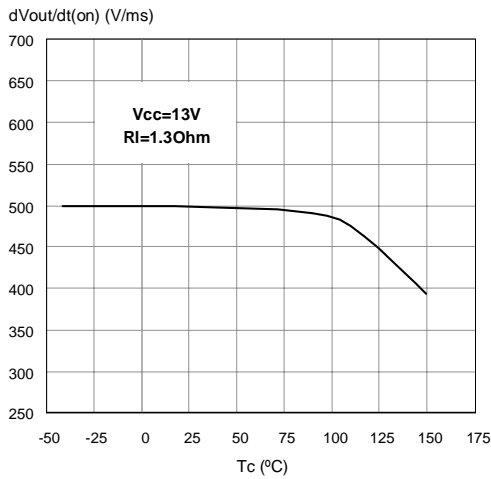


Figure 19. Turn-off Voltage Slope

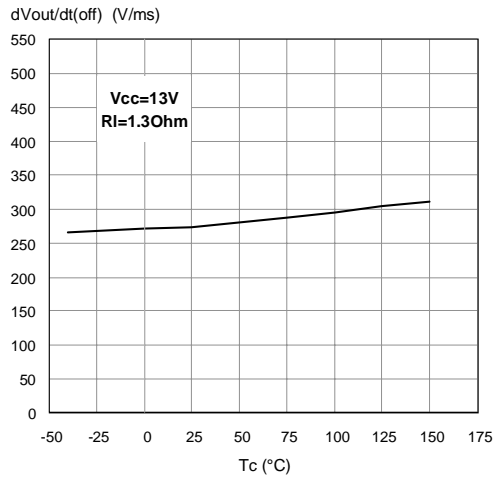


Figure 17. Overvoltage Shutdown

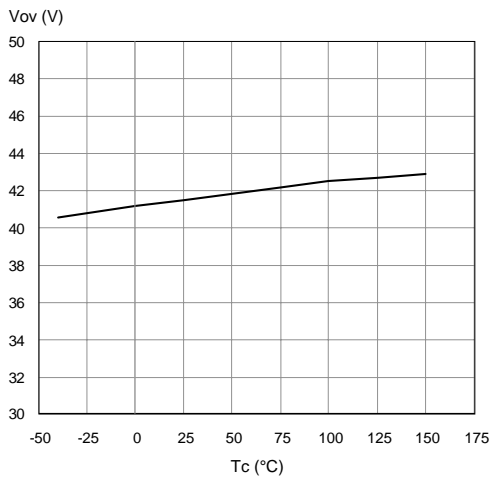


Figure 20. I_{LIM} Vs T_{case}

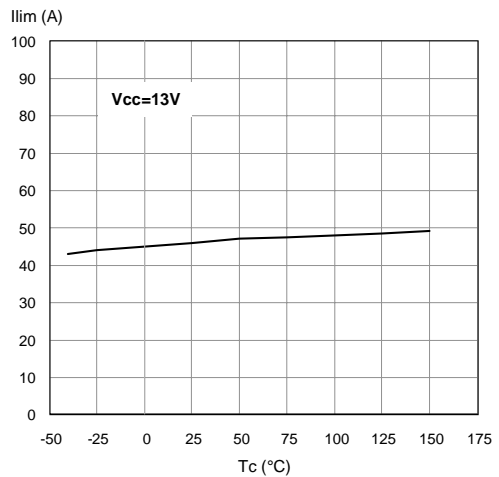
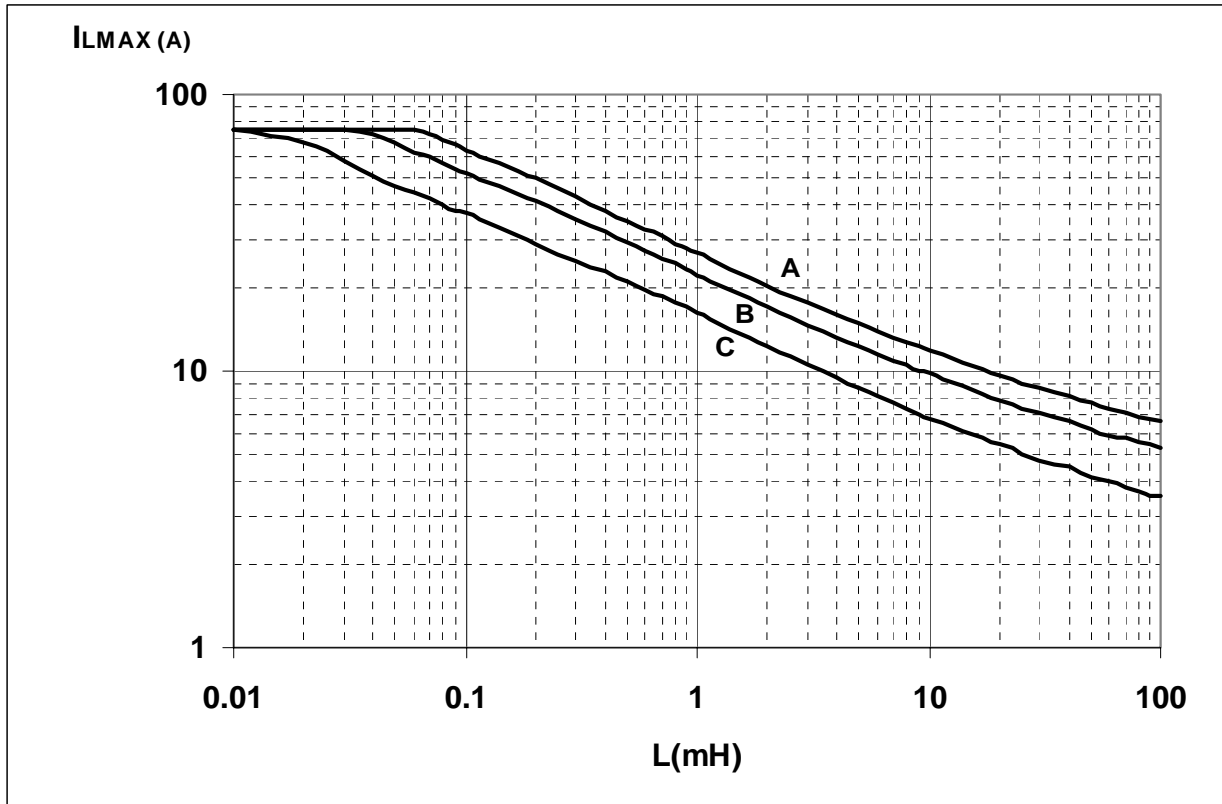


Figure 21. P²PAK Maximum turn off current versus load inductance



- A = Single Pulse at $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at $T_{Jstart}=100^{\circ}C$
- C= Repetitive Pulse at $T_{Jstart}=125^{\circ}C$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Conditions:

$V_{CC}=13.5V$

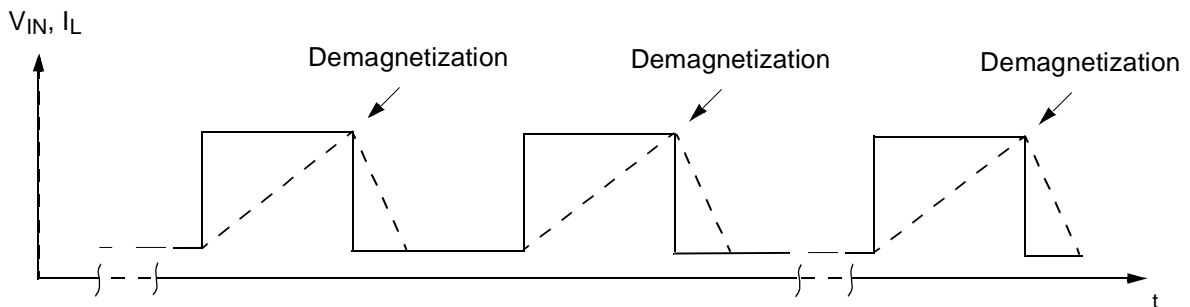
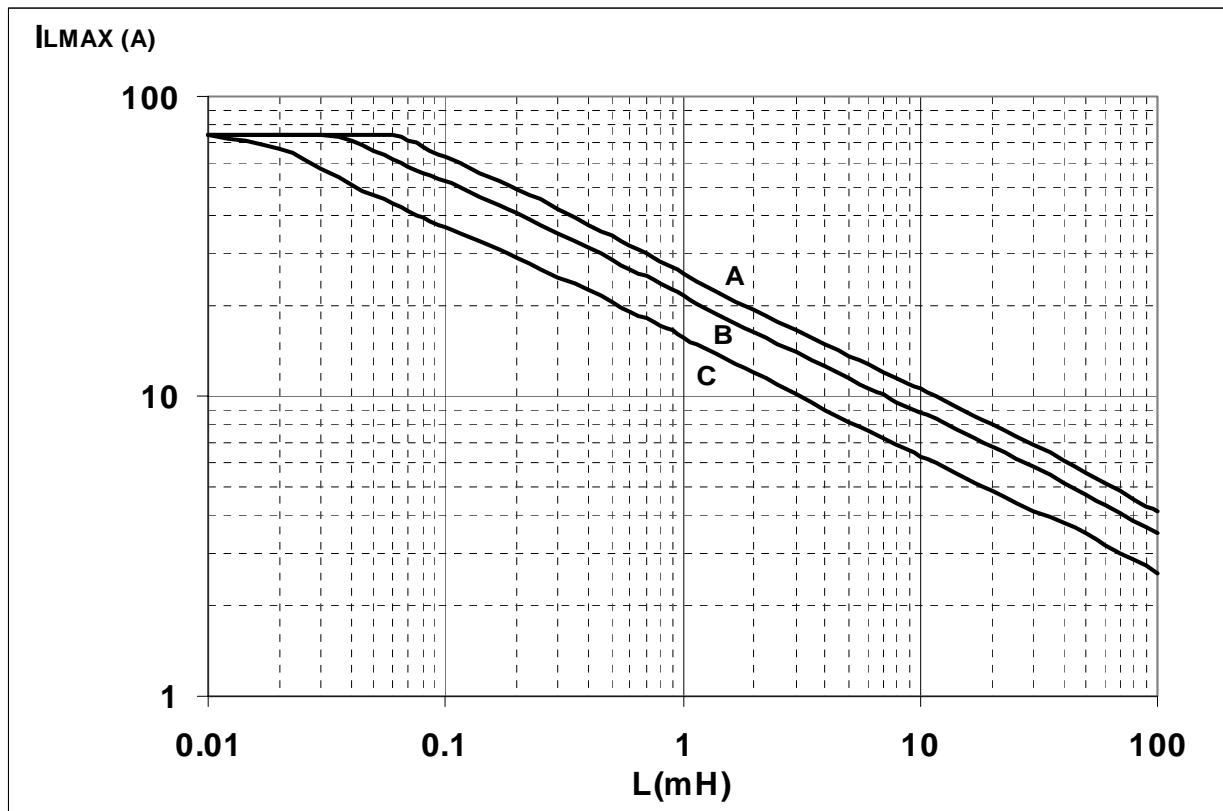


Figure 22. SO-16L Maximum turn off current versus load inductance



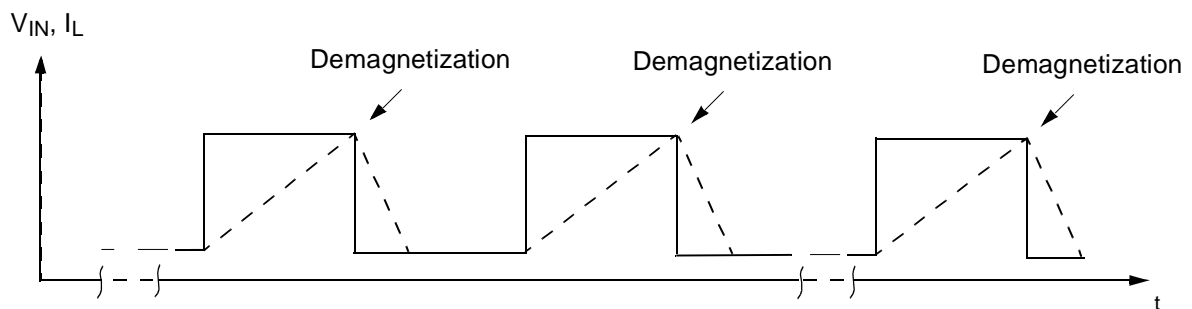
- A = Single Pulse at $T_{Jstart}=150^{\circ}C$
- B = Repetitive pulse at $T_{Jstart}=100^{\circ}C$
- C = Repetitive Pulse at $T_{Jstart}=125^{\circ}C$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Conditions:

$V_{CC}=13.5V$



SO-16L Thermal Data

Figure 23. SO-16L PC Board

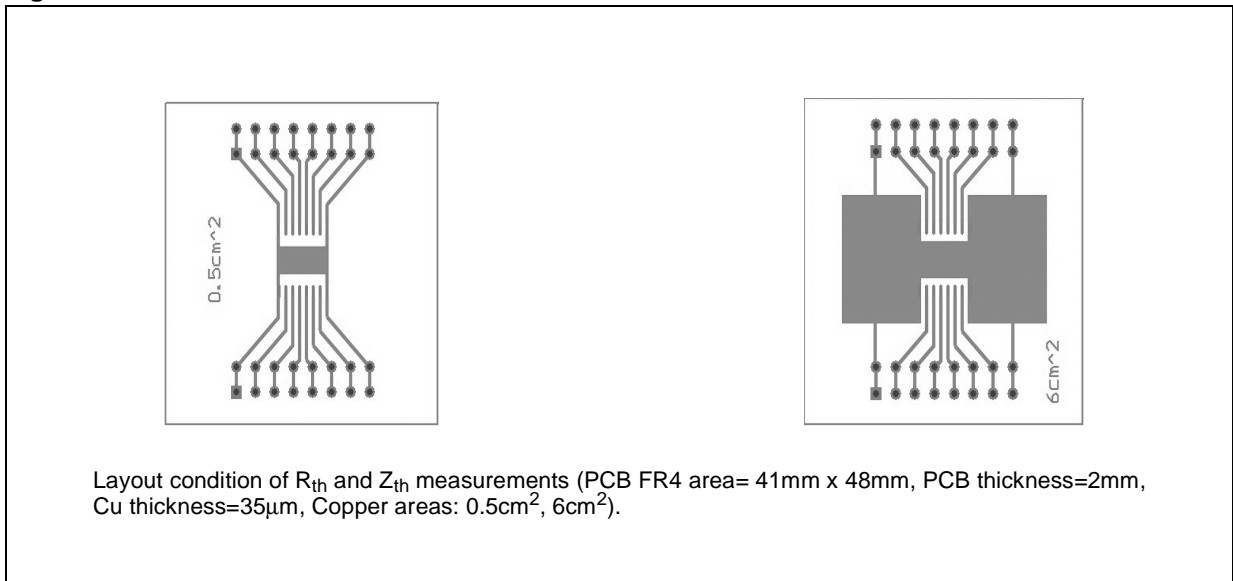
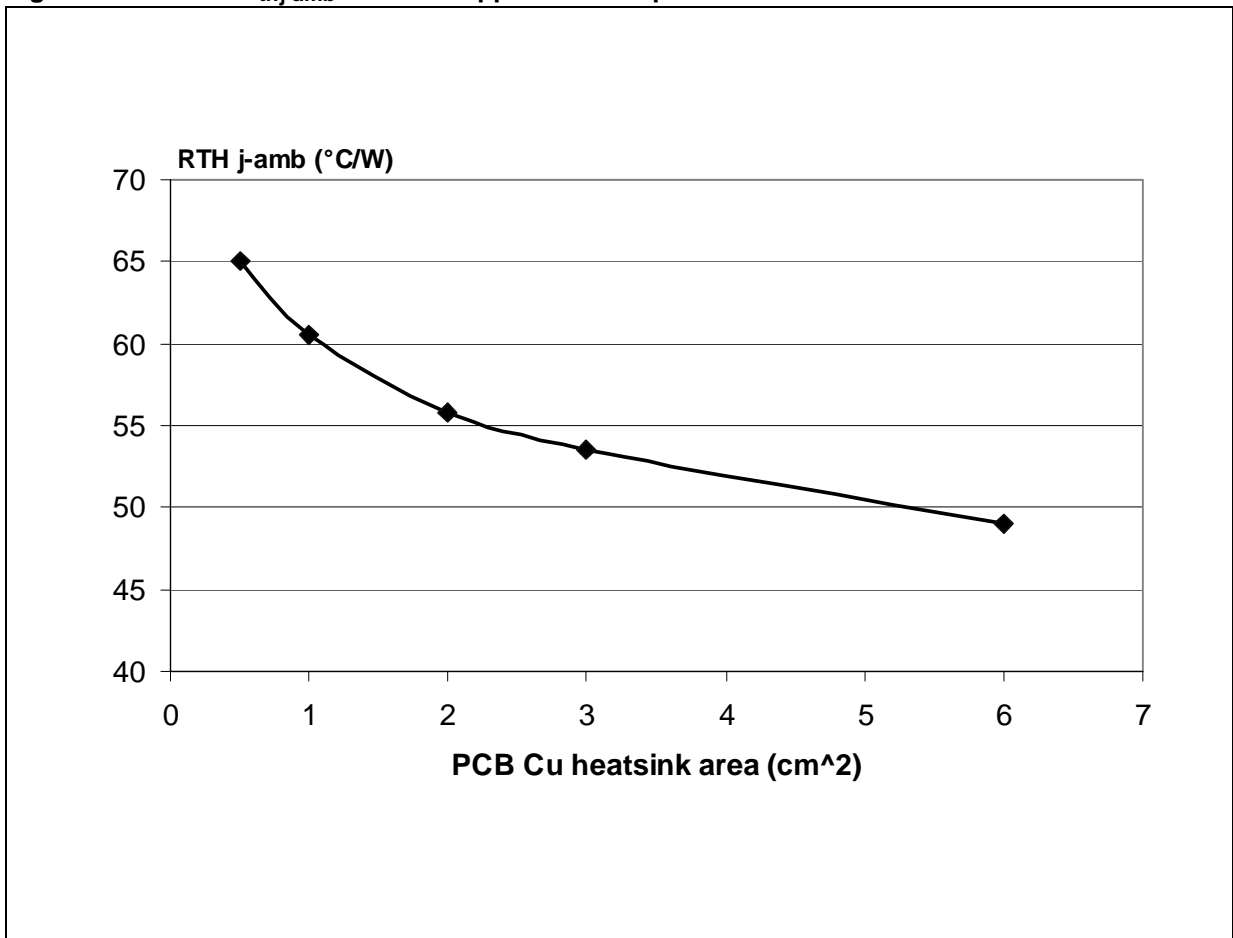


Figure 24. SO-16L $R_{thj-amb}$ Vs PCB copper area in open box free air condition



P²PAK Thermal Data

Figure 25. P²PAK PC Board

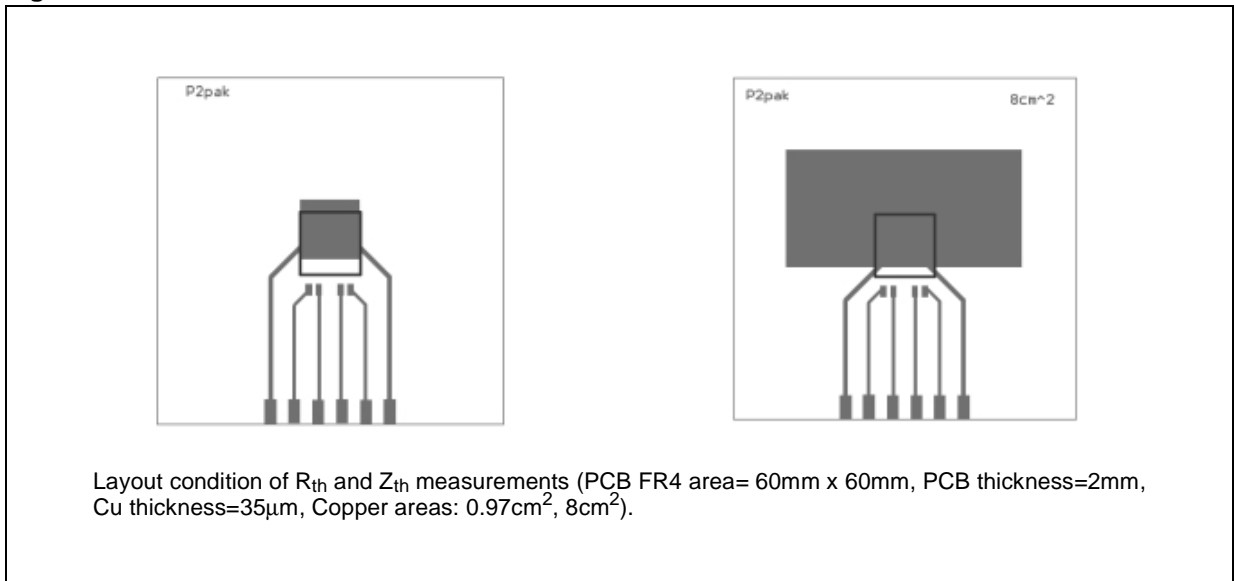


Figure 26. P²PAK $R_{thj-amb}$ Vs PCB copper area in open box free air condition

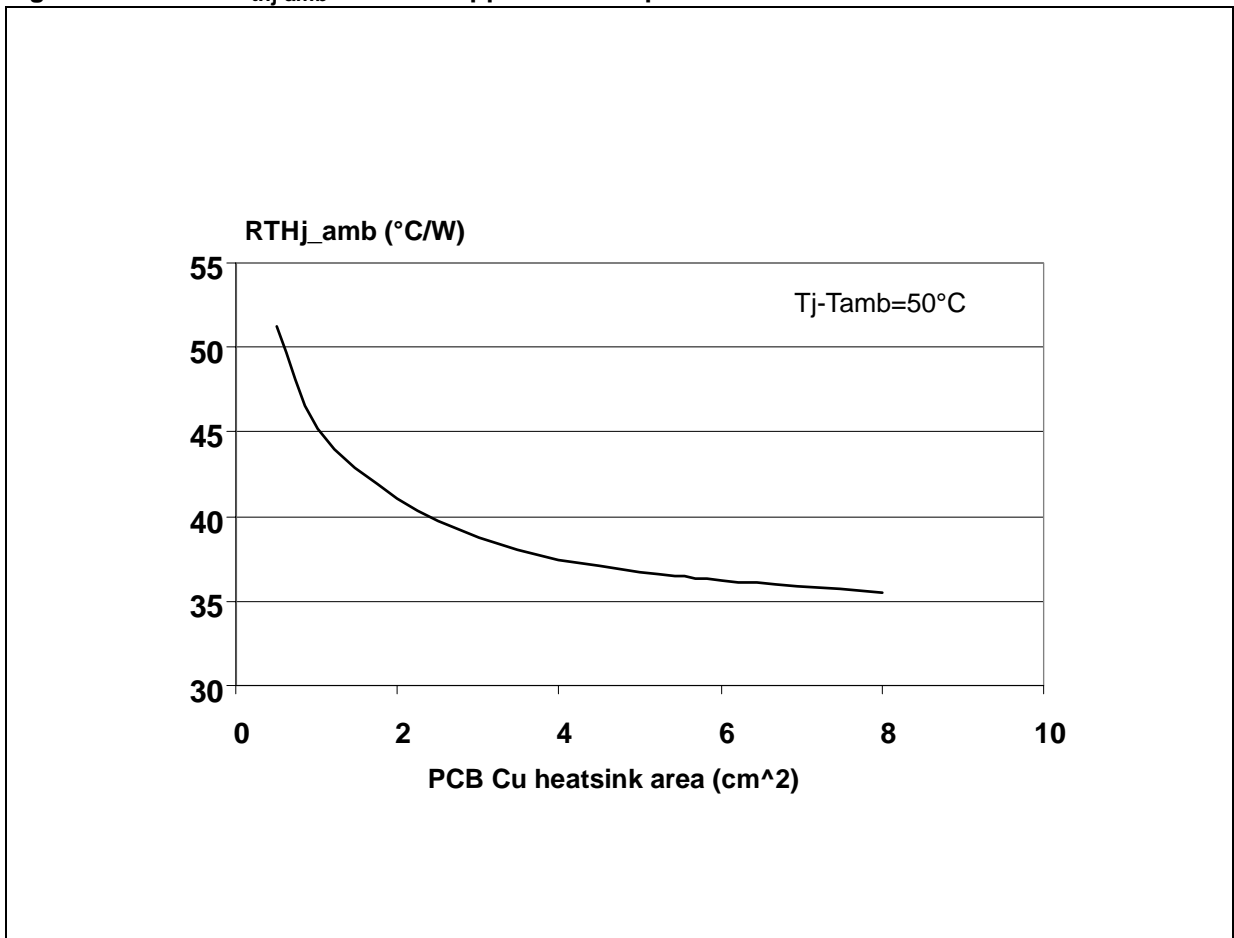


Figure 27. P²PAK Thermal Impedance Junction Ambient Single Pulse

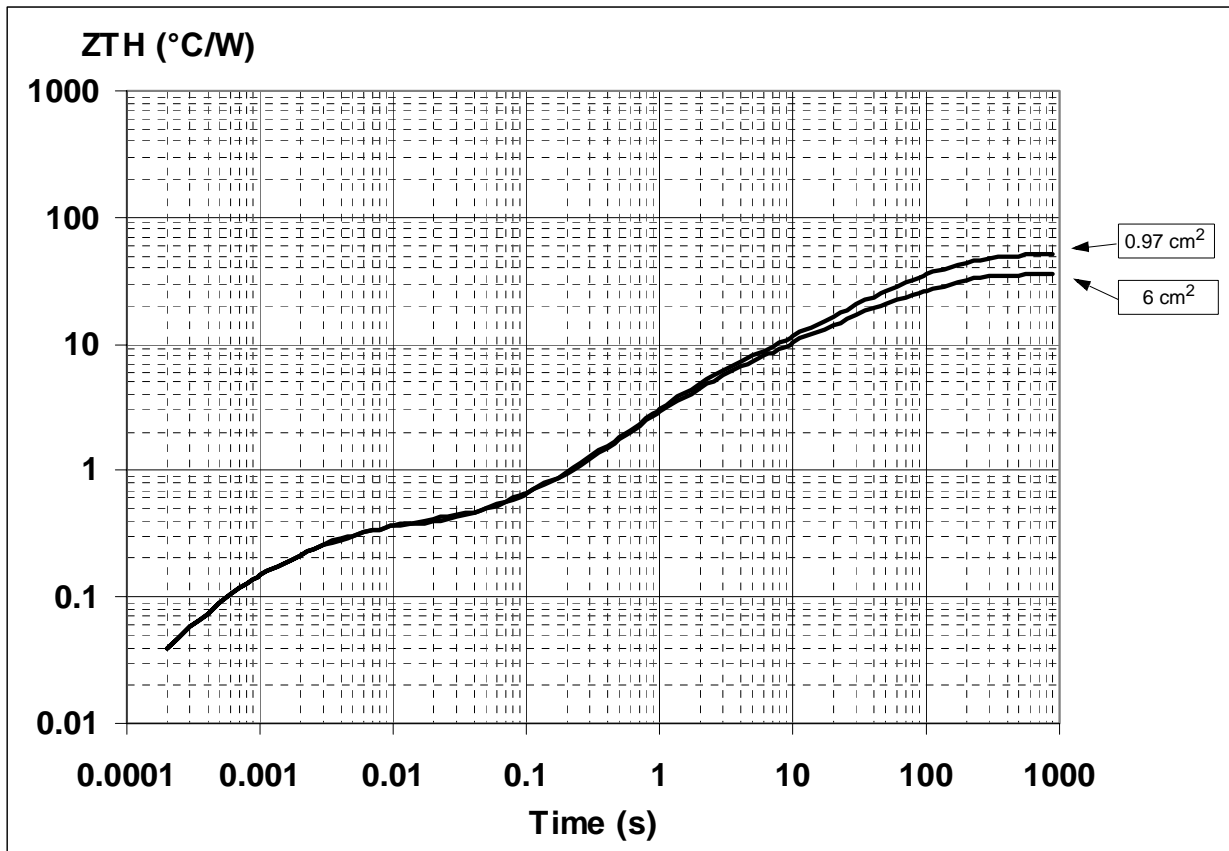
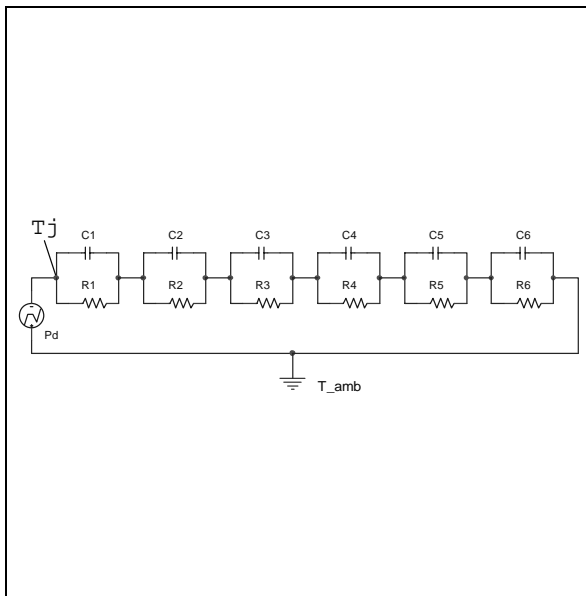


Figure 28. Thermal fitting model of a single channel HSD in P²PAK



Pulse calculation formula

$$T_{H\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 13. Thermal Parameter

Area/island (cm ²)	0.97	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	0.22	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0015	
C2 (W.s/°C)	0.007	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.4	
C5 (W.s/°C)	2	
C6 (W.s/°C)	3	5

Figure 29. SO-16L Thermal Impedance Junction Ambient Single Pulse

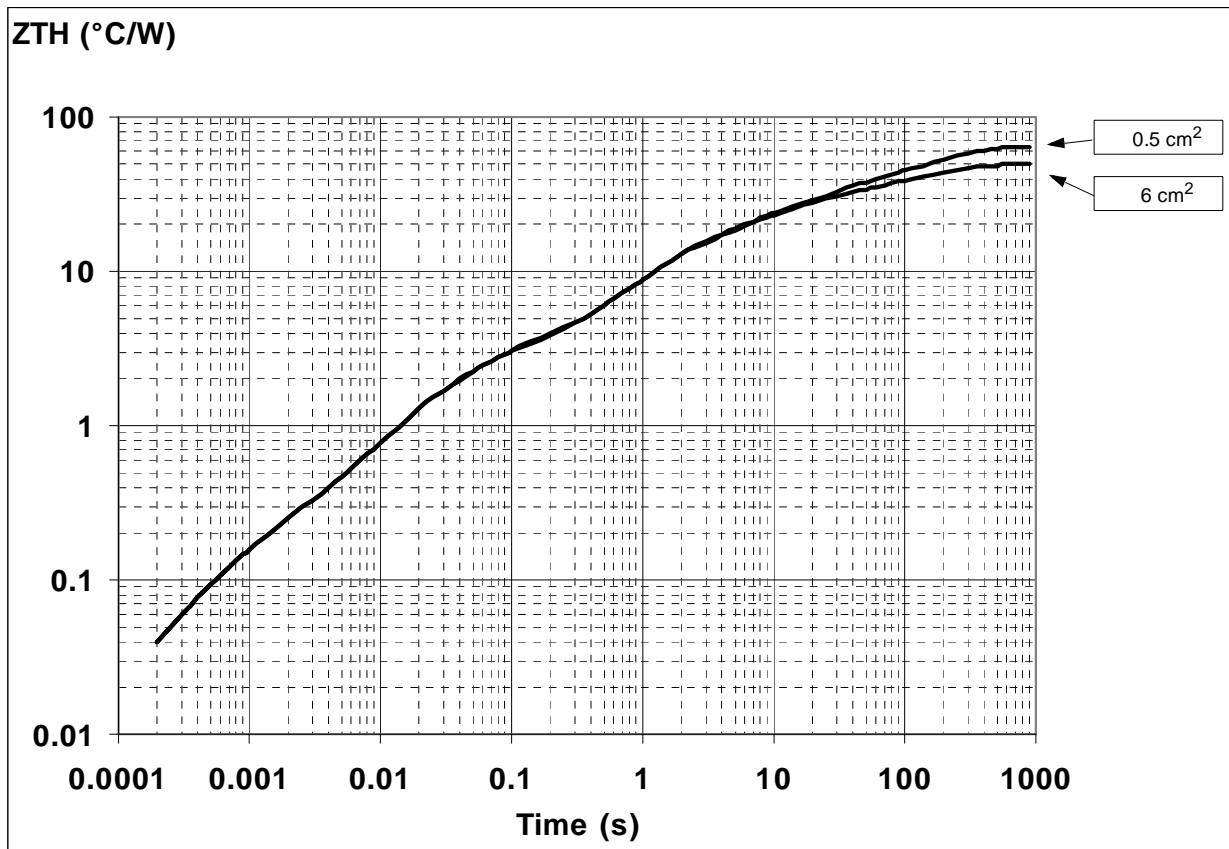
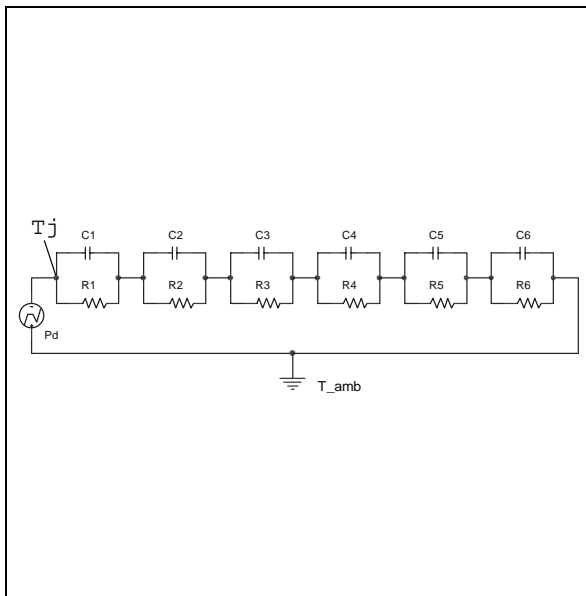


Figure 30. Thermal fitting model of a single channel HSD in SO-16L



Pulse calculation formula

$$T_{H\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 14. Thermal Parameter

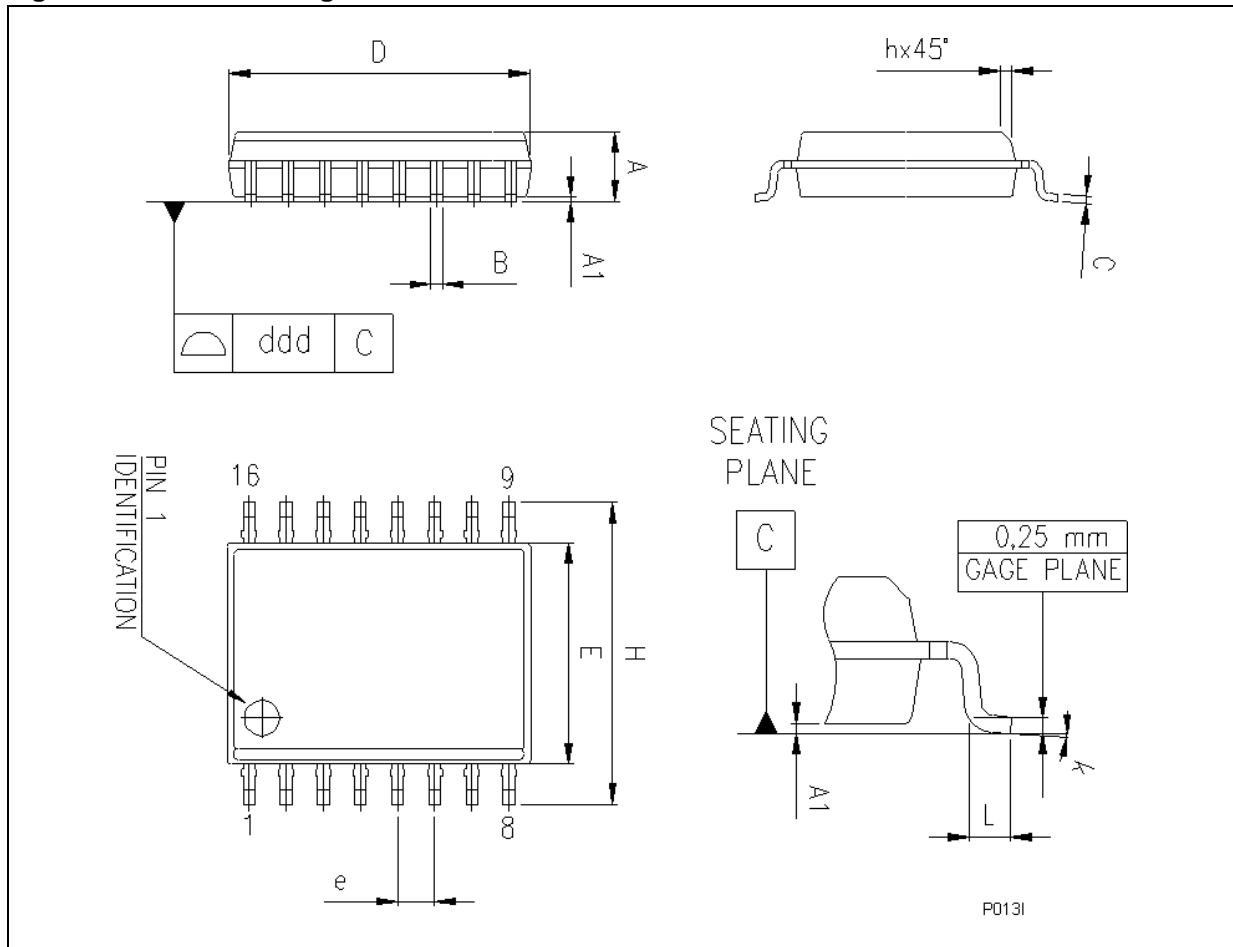
Area/island (cm ²)	0.5	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	2.2	
R4 (°C/W)	12	
R5 (°C/W)	15	
R6 (°C/W)	35	20
C1 (W.s/°C)	0.0015	
C2 (W.s/°C)	7.00E-03	
C3 (W.s/°C)	1.50E-02	
C4 (W.s/°C)	0.14	
C5 (W.s/°C)	1	
C6 (W.s/°C)	5	8

PACKAGE MECHANICAL

Table 15. SO-16L Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	10.10		10.50
E	7.40		7.60
e		1.27	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10
Package Weight	0.4Gr. (Typ.)		

Figure 31. SO-16L Package Dimensions

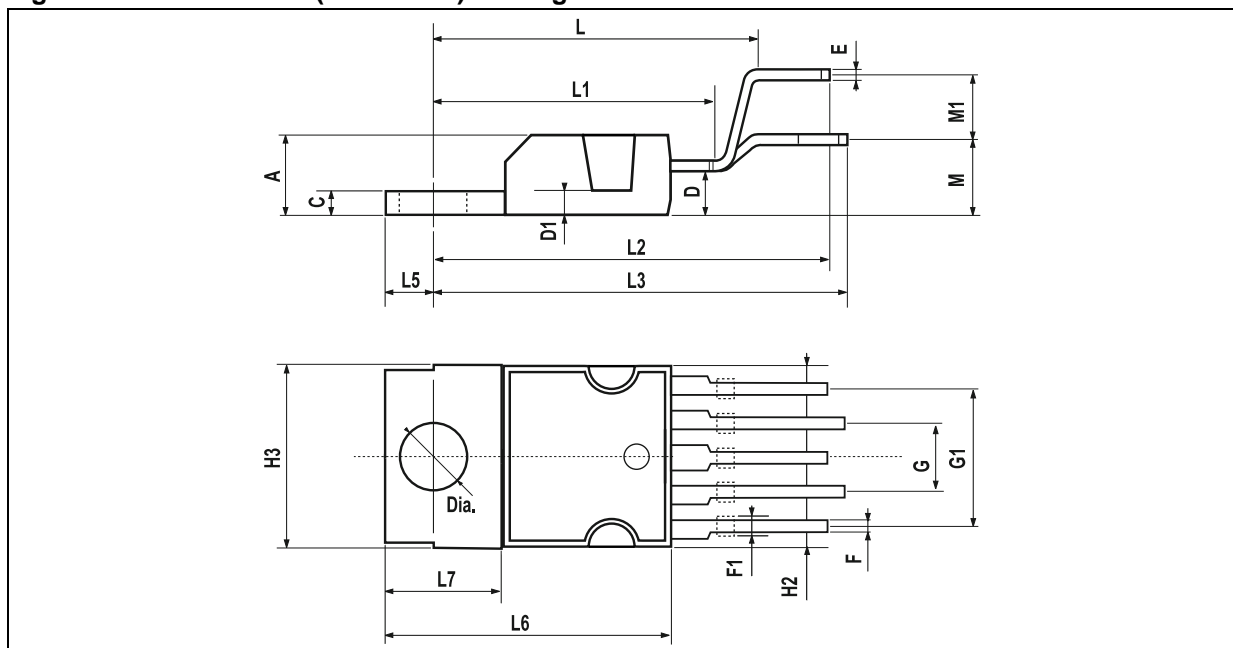


PACKAGE MECHANICAL

Table 16. PENTAWATT (VERTICAL) Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A			4.8
C			1.37
D	2.4		2.8
D1	1.2		1.35
E	0.35		0.55
F	0.8		1.05
F1	1		1.4
G	3.2	3.4	3.6
G1	6.6	6.8	7
H2			10.4
H3	10.05		10.4
L		17.85	
L1		15.75	
L2		21.4	
L3		22.5	
L5	2.6		3
L6	15.1		15.8
L7	6		6.6
M		4.5	
M1		4	
Diam.	3.65		3.85

Figure 32. PENTAWATT (VERTICAL) Package Dimensions



PACKAGE MECHANICAL

Table 17. P²PAK Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	4.30		4.80
A1	2.40		2.80
A2	0.03		0.23
b	0.80		1.05
c	0.45		0.60
c2	1.17		1.37
D	8.95		9.35
D2		8.00	
E	10.00		10.40
E1		8.50	
e	3.20		3.60
e1	6.60		7.00
L	13.70		14.50
L2	1.25		1.40
L3	0.90		1.70
L5	1.55		2.40
R		0.40	
V2	0°		8°
Package Weight	1.40 Gr (typ)		

Figure 33. P²PAK Package Dimensions

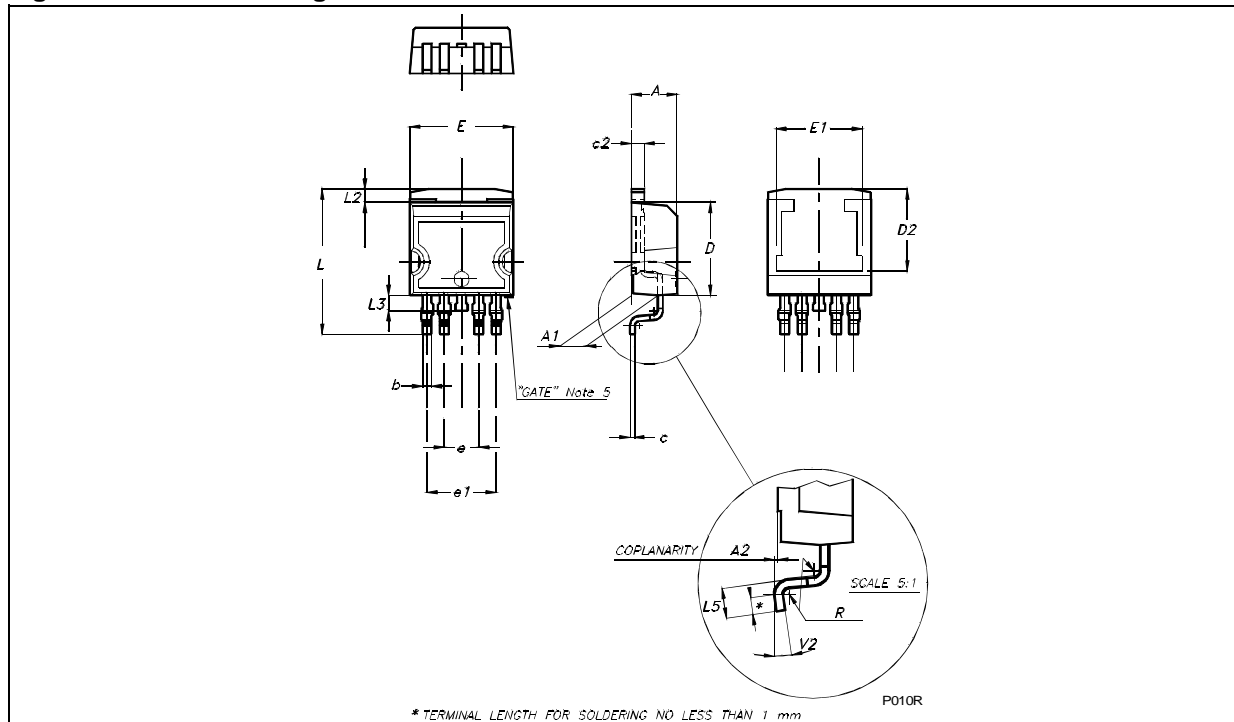


Figure 34. SO-16L TUBE SHIPMENT (no suffix)

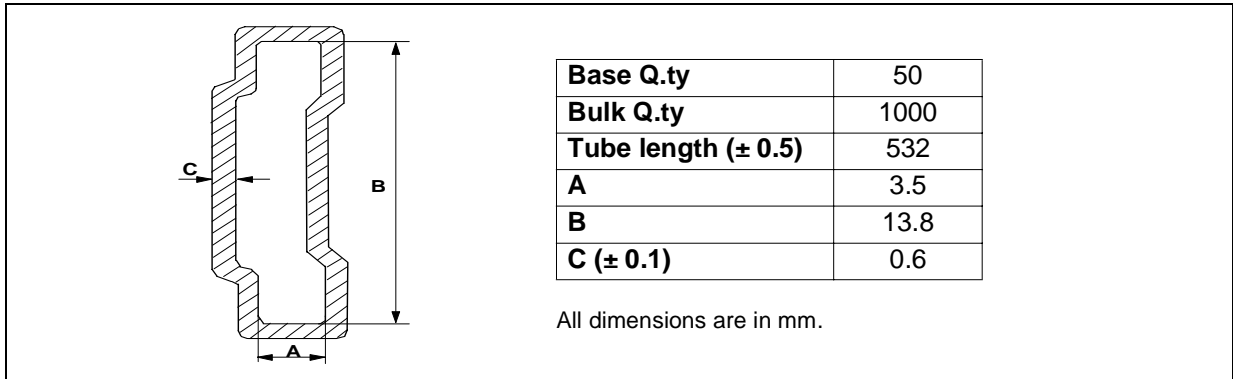


Figure 35. SO-16L TAPE AND REEL SHIPMENT (suffix "TR")

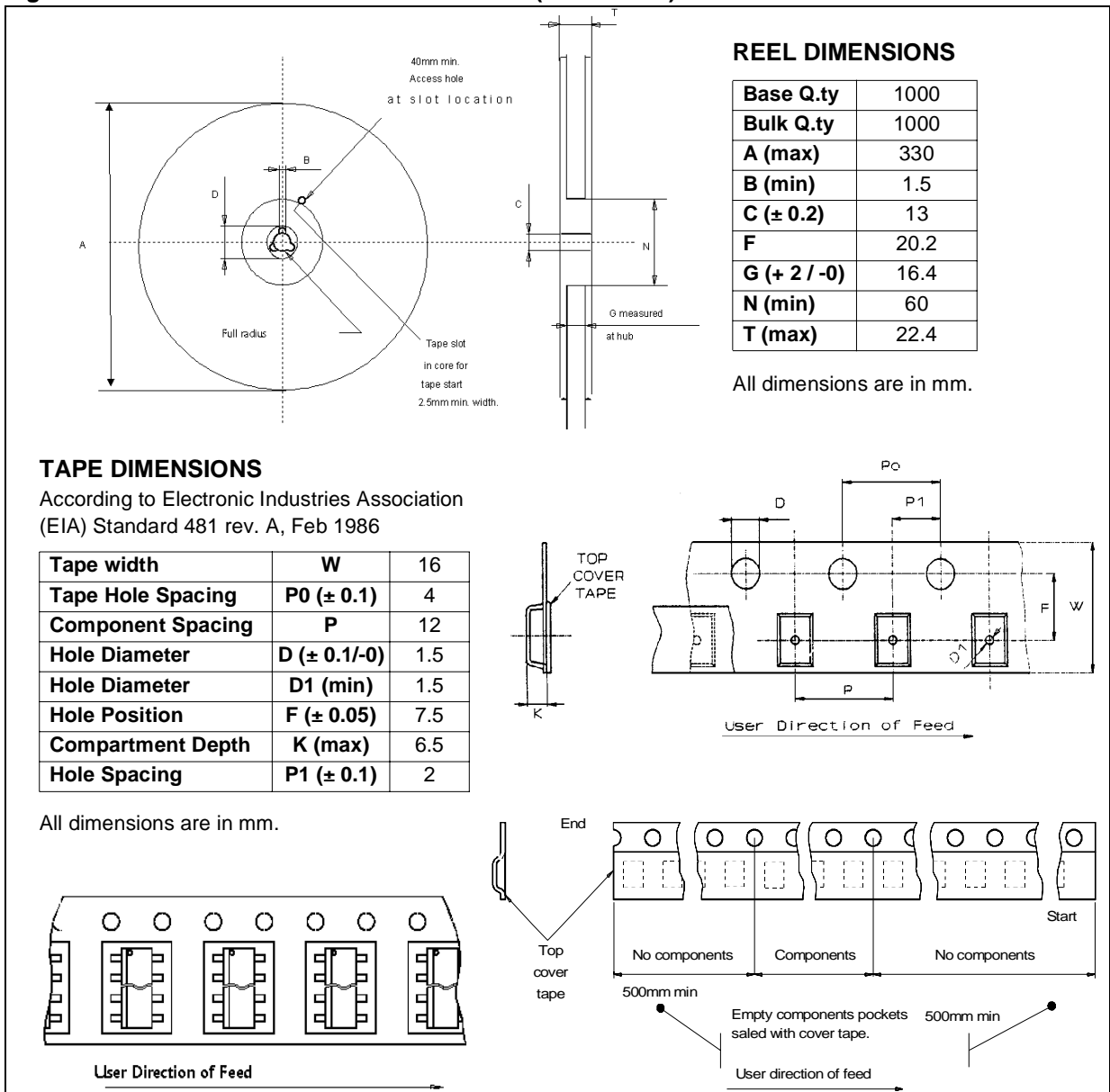


Figure 36. P²PAK TUBE SHIPMENT (no suffix)

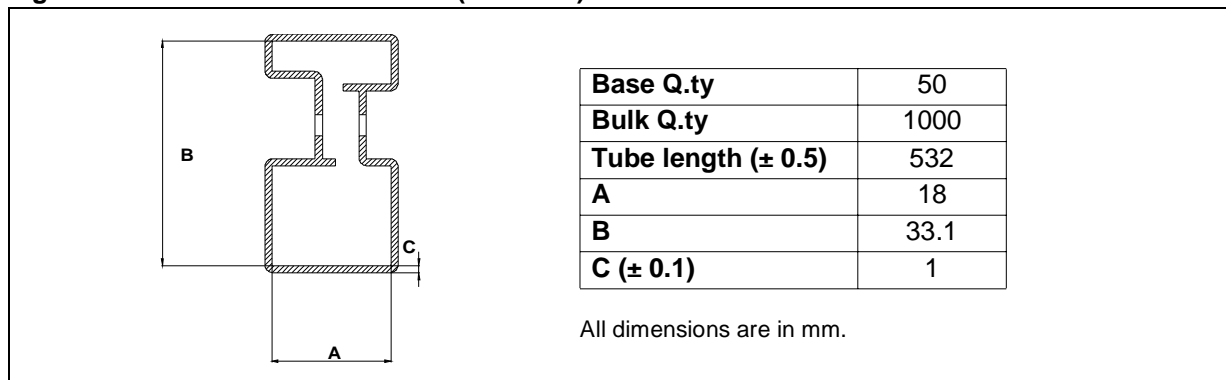
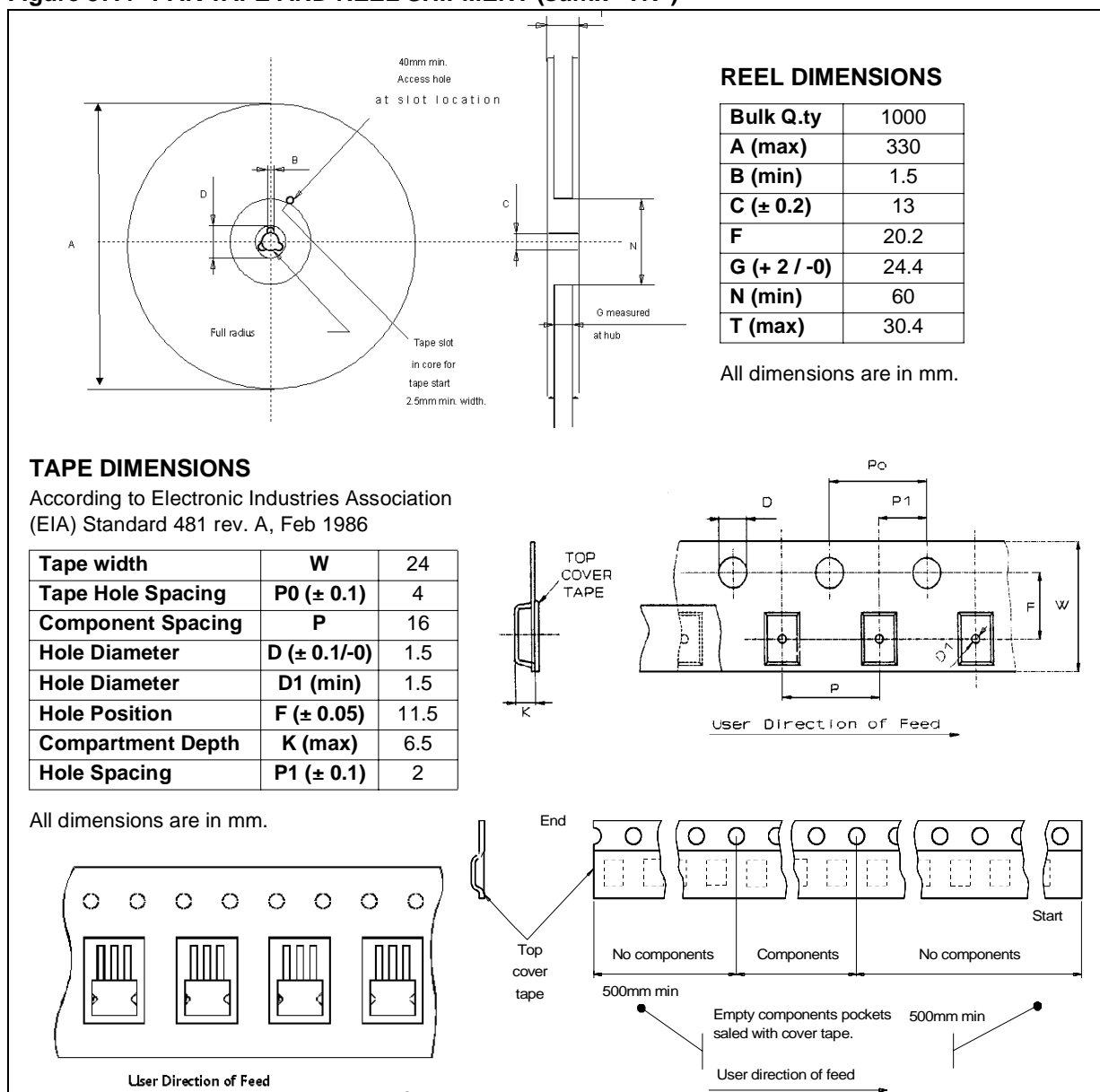


Figure 37. P²PAK TAPE AND REEL SHIPMENT (suffix “TR”)



REVISION HISTORY

Table 18. Revision History

Date	Revision	Description of Changes
Oct. 2004	1	- First Issue.

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