REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16																		

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
92-08-18

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, REAL TIME CLOCK, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-91641
A	67268	

SHEET 1 OF 16

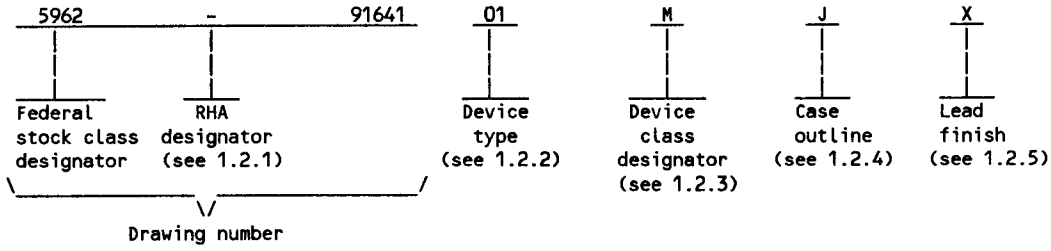
DESC FORM 193
JUL 91

5962-E471

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8572	Real time clock

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +7.0 V
DC input voltage range (V_{IN})	-0.5 V to V_{CC} + 0.5 V
DC output voltage range (V_{OUT})	-0.5 V to V_{CC} + 0.5 V
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Junction temperature (T_J)	+150°C
Power dissipation (P_D)	500 mW
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (Θ_{JA})	46°C/W board mount
	52°C/W socket mount

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) 2/	4.5 V dc to 5.5 V dc
Supply voltage (V_{BB}) (Battery-backed mode) 2/	2.2 V to V_{CC} - 0.4 V
DC input or output voltage (V_{IN}, V_{OUT})	0.0 V to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Address hold after read (t_{RAH})	3 ns (minimum)
Address hold after write strobe (t_{WAH})	3 ns (minimum)
Data hold after write strobe (t_{WDH})	3 ns (minimum)

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 3/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For F_{OSC} = 4.194304 or 4.9152 MHz, V_{BB} minimum = 2.8 V. In battery backed mode, $V_{BB} \leq V_{CC}$ - 0.4 V. Single supply mode: data retention voltage is 2.2 V minimum. In single supply mode (power connected to V_{CC} pin) 4.5 V $\leq V_{CC} \leq$ 5.5 V.

3/ Values will be added when they become available.

HANDBOOK

MILITARY
MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5 \text{ V} \le V_{CC} \le 5.5 \text{ V}$ Vpfail > V_{IH} V_{BB} = 3 V C_L = 100 pF unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}	All inputs except OSC IN	1,2,3	All	2		V
		OSC IN with external clock	1,2,3	All	V_{BB}-.1		V
Input low voltage	V_{IL}	All inputs except OSC IN	1,2,3	All		0.8	V
		OSC IN with external clock	1,2,3	All		0.1	V
Output high voltage (excluding OSC OUT)	V_{OH}	I_{OH} = -20 µA, V_{CC} = 4.5 V	1,2,3	All	V_{CC}-.1		V
		I_{OH} = -4 mA, V_{CC} = 4.5 V	1,2,3	All	3.5		V
Output low voltage (excluding OSC OUT)	V_{OL}	I_{OL} = 20 µA, V_{CC} = 4.5 V	1,2,3	All		0.1	V
		I_{OL} = 4 mA, V_{CC} = 4.5 V	1,2,3	All		0.25	V
Input leakage current (except OSC IN)	I_I	V_{IN} = V_{CC}, V_{CC} = 5.5 V	1,2,3	All		1	µA
		V_{IN} = 0 V, V_{CC} = 5.5 V	1,2,3	All		-1	µA
3-state leakage current	I_{OZ}	V_O = V_{CC}, V_{CC} = 5.5 V	1,2,3	All		5	µA
		V_O = 0 V, V_{CC} = 5.5 V	1,2,3	All		-5	µA
Output high leakage current INTR pin	I_{LKG}	V_O = V_{CC}, V_{CC} = 5.5 V, output open drain	1,2,3	All		15	µA
		V_O = 0 V, V_{CC} = 5.5 V, output open drain	1,2,3	All		-15	µA
Quiescent current	I_{CC}	FOSC = 32.768 KHz, V_{CC} = 5.5 V, V_{IN} = V_{CC} or GND, 2/,3/	1,2,3	All		275	µA
		FOSC = 32.768 KHz, V_{CC} = 5.5 V, V_{IN} = V_{CC} or GND, 2/,4/	1,2,3	All		1	mA
		FOSC = 32.768 KHz, V_{CC} = 5.5 V, V_{IN} = V_{IH} or V_{IL}, 2/,4/	1,2,3	All		12	mA
		FOSC = 4.9152 MHz or 4.194304 MHz, V_{CC} = 5.5 V, V_{IN} = V_{CC} or GND, 2/,4/	1,2,3	All		8	mA
		FOSC = 4.9125 MHz or 4.194304 MHz, V_{CC} = 5.5 V, V_{IN} = V_{IH} or V_{IL}, 2/,4/	1,2,3	All		20	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ $\overline{Vpfail} > V_{IH}$ $V_{BB} = 3\ V$ $C_L = 100\ pF$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Quiescent supply current (single supply mode)	I_{CC}	$V_{CC} = 5.5\ V$, $V_{BB} = GND$, $V_{IN} = V_{CC}$ or GND, FOSC = 32.768 KHz, 2/	1,2,3	All		40	µA
		$V_{CC} = 5.5\ V$, $V_{BB} = GND$, $V_{IN} = V_{CC}$ or GND, FOSC = 4.9152 MHz or 4.194304 MHz 2/	1,2,3	All		7.5	mA
Standby mode battery supply current 2/	I_{BB}	$V_{CC} = 0\ V$, FOSC = 32.768 KHz	1,2,3	All		10	µA
		$V_{CC} = 0\ V$, FOSC = 4.9152 MHz	1,2,3	All		400	µA
Battery supply leakage current	I_{BLK}	$V_{CC} = 5.5\ V$, $2.2\ V < V_{BB} < 4.0\ V$	1	All	-5	1.5	µA
			2,3	All	-5	3.5	µA
Input capacitance	C_{IN}	F = 1 MHz; See 4.4.1c	4	All		5	pF
Output capacitance	C_{OUT}		4	All		7	pF
Functional testing		$V_{CC} = 4.5\ V$, 5.5 V See 4.4.1b	7,8	All			
Address valid prior to read strobe	t_{AR}	$\overline{Vpfail} = 3\ V$; See figure 3	9,10,11	All	20		ns
Read strobe width	t_{RW}	$\overline{Vpfail} = 3\ V$; See figure 3 5/	9,10,11	All	80		ns
Chip select to data valid time	t_{CD}	$\overline{Vpfail} = 3\ V$; See figure 3	9,10,11	All		80	ns
Read strobe to data valid time	t_{RD}		9,10,11	All		70	ns
Read or chip select to tri-state	t_{DZ}		9,10,11	All		60	ns
Chip select hold after read strobe	t_{RCH}		9,10,11	All	0		ns
Minimum inactive time between read or write accesses	t_{DS}		9,10,11	All	50		ns
Address valid before write strobe	t_{AW}		9,10,11	All	20		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5 \text{ V} \le V_{CC} \le 5.5 \text{ V}$ $\overline{\text{Vpfail}} > V_{IH}$ $V_{BB} = 3 \text{ V}$ $C_L = 100 \text{ pF}$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip select to end of write strobe	t_{CW}	$\overline{\text{Vpfail}}$ = 3 V	9,10,11	All	90		ns
Write strobe width	t_{WW}	$\overline{\text{Vpfail}}$ = 3 V 6/	9,10,11	All	80		ns
Data valid to end of write strobe	t_{DW}	$\overline{\text{Vpfail}}$ = 3 V	9,10,11	All	50		ns
Chip select hold after write strobe	t_{WCH}		9,10,11	All	0		ns

1/ Unless otherwise specified, all testing shall be conducted under worst-case conditions.

2/ OSC IN driven by a signal generator. Contents of test register = 00H and MFO pin not configured as buffered oscillator output.

3/ I_{CC} tested with all power fail circuitry disabled, by setting D7 of interrupt control register 1 to 0.

4/ I_{CC} tested with all power fail circuitry enabled, by setting D7 of interrupt control register 1 to 1.

5/ Read Strobe width as used in the read timing table is defined as the period when both chip select and read inputs are low. Hence read commences when both signals are low and terminates when either signal returns high.

6/ Write Strobe width as used in the write timing table is defined as the period when both chip select and write inputs are low. Hence write commences when both signals are low and terminates when either signal returns high.

Device Type	All		
Case Outline	J		
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	$\overline{CS}$	13	MFO
2	$\overline{RD}$	14	INTR
3	$\overline{WR}$	15	D0
4	A0	16	D1
5	A1	17	D2
6	A2	18	D3
7	A3	19	D4
8	A4	20	D5
9	V_{BB}	21	D6
10	OSC IN	22	D7
11	OSC OUT	23	$\overline{PFAIL}$
12	GND	24	V_{CC}

FIGURE 1. Terminal connections.

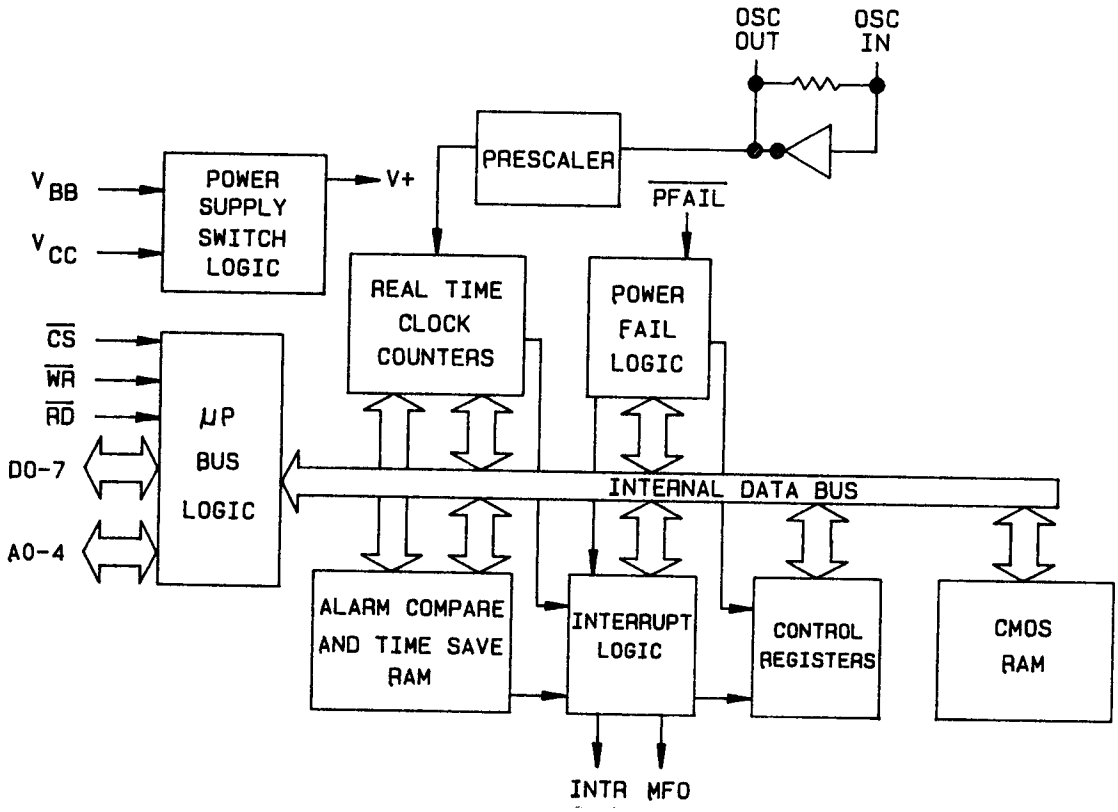


FIGURE 2. Block diagram.

Read timing diagram

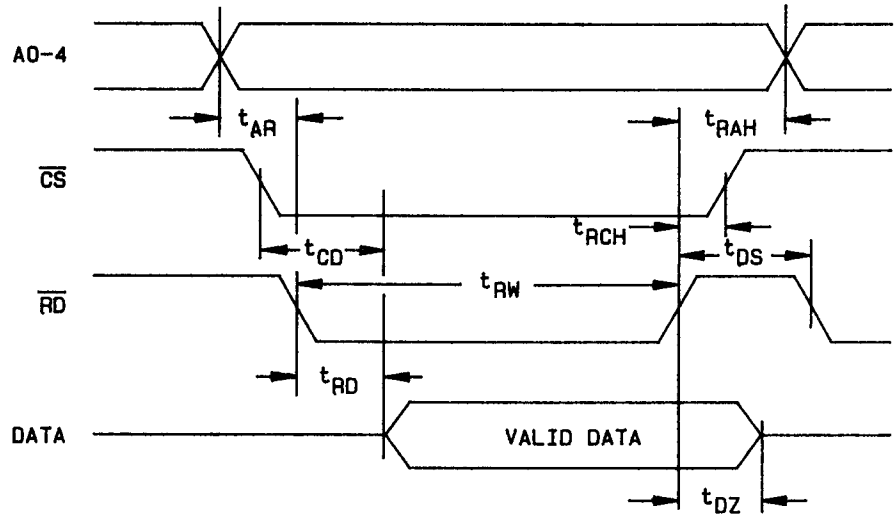
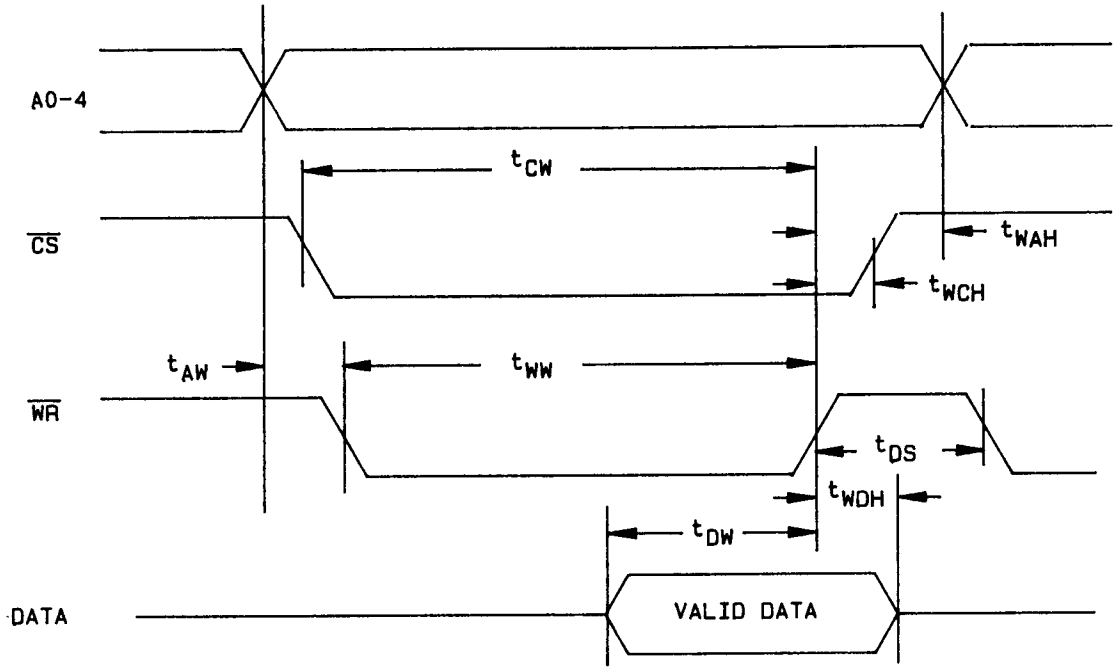
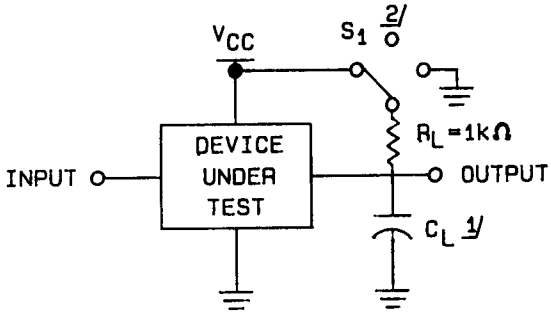


FIGURE 3. Switching waveforms and test circuit.

Write timing diagram





AC Test conditions	
Input pulse levels	GND to 3.0 V dc
Input rise and fall times	6 ns (10% to 90%)
Input and output Reference levels	1.3 V dc
Tri-state reference levels (see note 2)	active high +0.5 V
	active low -0.5 V

NOTES:
1. C_L = 100 pF, includes jig and scope capacitance
2. S1 = V_{CC} for active low to high impedance measurements
   S1 = GND for active high to high impedance measurements
   S1 = open for all other timing measurements

FIGURE 3. Switching waveforms and test circuit - Continued.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 ($C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1,7,9	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1/ 1,2,3 7,8,9, 10,11	1/ 1,2,3 7,8,9, 10,11	2/ 1,2,3 7,8,9, 10,11	1/ 1,2,3 7,8,9, 10,11	2/ 1,2,3 7,8,9, 10,11
Group A test requirements (see 4.4)	1,2,3,4, 7,8,9 10,11	1,2,3,4, 7,8,9, 10,11	1,2,3,4, 7,8,9, 10,11	1,2,3,4, 7,8,9, 10,11	1,2,3,4, 7,8,9, 10,11
Group B end-point electrical parameters (see 4.4)			1,7,9		
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3		1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.
f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.5 Symbols, definitions, and functional descriptions. See Table III.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

TABLE III. Pin descriptions.

Symbol	Name and function
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$ (inputs)	These pins interface to microprocessor control lines. The $\overline{CS}$ pin is an active low enable for the read and write operations. Read and write pins are also active low and enable reading or writing to the device. All three pins are disabled when power failure is detected. However, if a read or write is in progress at this time, it will be allowed to complete its cycle.
A0-A4 (inputs)	These five pins are for register selection. They individually control which location is to be accessed. These inputs are disabled when power failure is detected.
OSC IN (input) OSC OUT (output)	These two pins are used to connect the crystal to the internal parallel resonant oscillator. The oscillator is always running when power is applied to V_{BB} and V_{CC}, and the correct crystal select bits in the Real Time Mode Register have been set.
MFO (output)	The multi-function output can be used as a second interrupt output for interrupting the microprocessor. This pin can also provide an output for the oscillator. The MFO is configured as push-pull, active high for normal or single power supply operation and as an open drain during standby mode. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.
INTR (output)	The interrupt output is used to interrupt the processor when a timing event or power fail has occurred and the respective interrupt has been enabled. The INTR output is permanently configured active low, open drain. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

TABLE III. Pin descriptions - Continued.

Symbol	Name and function
D0-D7 (input/output)	These eight bidirectional pins connect to the host microprocessor's data bus and are used to read from and write to the device. When the $\overline{\text{PFAIL}}$ pin goes low and a write is not in progress, these pins are at tri-state.
$\overline{\text{PFAIL}}$	In battery backed mode, this pin can have a digital signal applied to it via some external power detection logic. When $\overline{\text{PFAIL}}$ = logic 0 the device goes into a lockout mode, in a minimum of 30 microseconds or a maximum of 63 microseconds unless lockout delay is programmed. In the single power supply mode, this pin is not usable as an input and should be tied to V_{CC}.
V_{BB} (battery power pin)	This pin is connected to a backup power supply. The power supply is switched to the internal circuitry when V_{CC} becomes lower than V_{BB}. Utilizing this pin eliminates the need for external logic to switch in and out the back-up power supply. If this feature is not to be used then this pin must be tied to ground, the device programmed for single power supply only, and power applied to the V_{CC} pin.
V_{CC}, GND	V_{CC} is the main system power pin. GND is the common ground pin for V_{BB} and V_{CC}.