

2-channel Read/Write Amplifier for GMR-Ind Head Hard Disk Drive

Description

The CXA3541N is a read/write amplifier for GMR-Ind (Giant Magneto Resistive-Inductive) heads used in hard disk drives, and is capable of supporting up to two channels.

Features

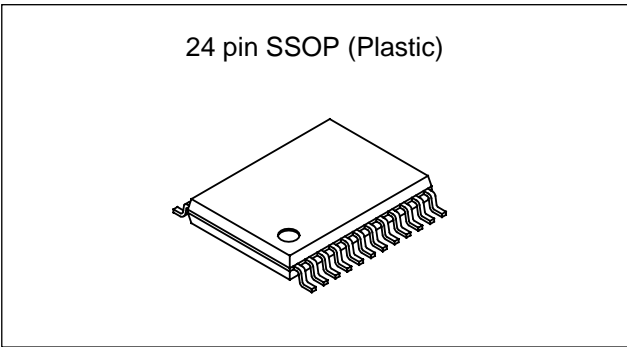
- +5V and -3V power supply
- Current bias voltage sense type
- Low power 180mW at read
- Differential read amplifier gain; $\times 100/135$ ($R_{MR} = 50\Omega$)
- Input noise of $0.77nV/\sqrt{Hz}$ (typ.), $R_{MR} = 50\Omega$, $I_B = 5.9mA$
- Recovery time write to read; 300ns (typ.)
- Write data is triggered by differential P-ECL signal
- Servo bank write
- Write unsafe detection circuit
- Serial port
 - Head selection
 - MR bias
 - Write current

Applications

Hard disk drives with GMR-Ind heads

Structure

Bipolar silicon monolithic IC



Absolute Maximum Ratings ($T_a = 25^\circ C$)

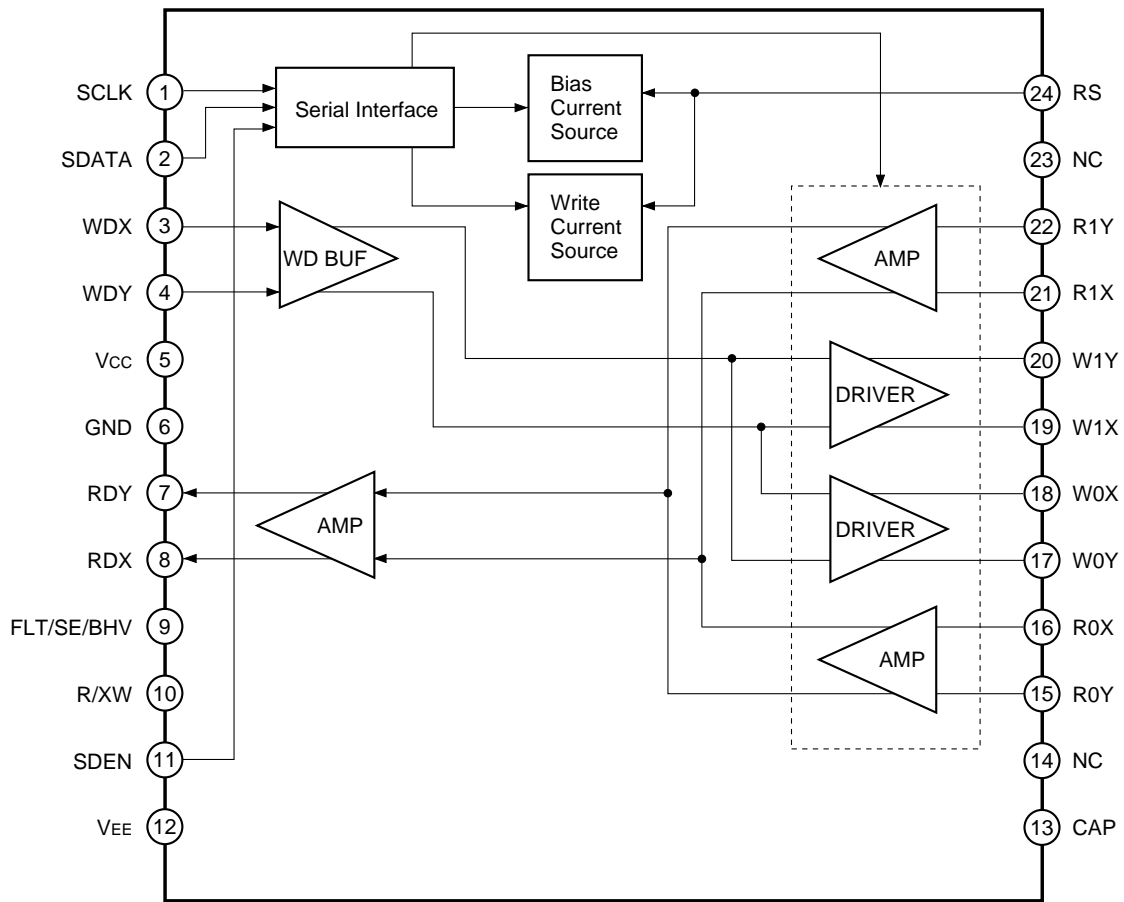
| | | | |
|-------------------------------|-----------|------------------------|------------------|
| • Supply voltage | V_{CC} | -0.3 to +5.8 | V |
| • Supply voltage | V_{EE} | -3.7 to +0.3 | V |
| • Digital input voltage | V_{di} | -0.3 to $V_{CC} + 0.3$ | V |
| • Operating temperature | T_{opr} | 0 to +70 | °C |
| • Storage temperature | T_{stg} | -55 to +150 | °C |
| • Allowable power dissipation | P_D | 800 | mW (on board) |

Operating Conditions

| | | | |
|-------------------|----------|--------------|----|
| • Supply voltage | V_{CC} | 4.4 to 5.5 | V |
| | V_{EE} | -3.5 to -2.6 | V |
| • MR bias voltage | V_{MR} | -300 to +300 | mV |
| • Bias current | I_B | 3 to 8 | mA |
| • Write current | I_W | 19.5 to 49.5 | mA |

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Block Diagram and Pin Configuration



Pin Description

| Pin No. | Symbol | Equivalent circuit | Description |
|--------------|-----------------------|--------------------|--|
| 1 2 11 | SCLK SDATA SDEN | | Serial control signal input. |
| 3 4 | WDX WDY | | Differential P-ECL write data input. |
| 5 | Vcc | | 5V power supply. |
| 6 | GND | | Ground. |
| 7 8 | RDY RDX | | Read amplifier output with coupling capacitors. High impedance in the write mode. |
| 9 | FLT/SE/BHV | | Head unsafe detection output. Servo bank write enable input. Buffered head voltage output. |

| Pin No. | Symbol | Equivalent circuit | Description |
|----------------------|--------------------------|--------------------|---|
| 10 | R/XW | | Read/write control signal input. Read when high, write when low. |
| 12 | VEE | | -3V power supply. |
| 13 | CAP | | Connect an external capacitor of read amplifier between this pin and VEE. |
| 14 23 | NC | | Non connection. |
| 16 15 21 22 | R0X R0Y R1X R1Y | | MR heads for read. Two channels are provided. |
| 18 17 19 20 | W0X W0Y W1X W1Y | | Inductive heads for write. Two channels are provided. |

| Pin No. | Symbol | Equivalent circuit | Description |
|---------|--------|--------------------|---|
| 24 | RS | | <p>Bias current setting register is connected between this pin and GND.</p> |

Electrical Characteristics

(Unless otherwise specified; $V_{CC} = 5V$, $V_{EE} = -3V$, $T_a = 25^\circ C$, $CAP = 0.1\mu F$, $R_S = 7.5k\Omega$)

| No. | Item | Symbol | Measurement conditions | Min. | Typ. | Max. | Unit |
|---|---|-------------------|--|-----------------------|------|-----------------------|------|
| Power Dissipation $I_W = 29.5mA$, $I_B = 5.9mA$ | | | | | | | |
| 1-1 | V _{CC} power supply current | ISP1 | Sleep mode | | 2.15 | 2.85 | mA |
| 1-2 | | IID1 | Idle mode | | 22 | 29 | mA |
| 1-3 | | IRE1 | Read mode | | 37 | 48 | mA |
| 1-4 | | IWR1 | Write mode | | 98 | 130 | mA |
| 1-5 | V _{EE} power supply current | IID2 | Idle mode | | 10 | 13 | mA |
| 1-7 | | IRE2 | Read mode | | 10 | 13 | mA |
| 1-8 | | IWR2 | Write mode | | 10 | 13 | mA |
| 1-9 | Bank write mode | ICCBW | $ICCBW = 17 + 17 \times N + I_W \times N$ $I_W = 29.5mA$ | — | 111 | — | mA |
| Digital Inputs | | | | | | | |
| 2-1 | TTL input low input voltage | V _{IL} | TTL input; R/XW Internal pull-up resistor | 0 | | 0.8 | V |
| 2-2 | TTL input high input voltage | V _{IH} | | 2.0 | | V _{CC} + 0.3 | V |
| 2-3 | TTL input input current | I _{TTL} | High voltage: 5V Low voltage: 0V | -200 | | 200 | μA |
| 2-4 | Serial interface input low input voltage | V _{SIL} | Serial input; SDATA, SCLK, SDEN | | | 0.8 | V |
| 2-5 | Serial interface input high input voltage | V _{SIH} | | 2.35 | | | V |
| 2-6 | Serial interface input input current | V _{ST} | High voltage: 3.3V Low voltage: 0V Pull-down resistor: 14kΩ | -500 | | 500 | μA |
| 3-1 | P-ECL common voltage | V _{PC} | $(V_H + V_L)/2$ | 1.55 | | V _{CC} | V |
| 3-2 | P-ECL differential voltage | V _{PD} | $(V_H - V_L)$ | 0.2 | | 1.5 | V |
| 3-3 | P-ECL high voltage | V _{PH} | | | | V _{CC} | V |
| 3-4 | P-ECL input current | I _{WD} | Input voltage: 4V | -20 | | 20 | μA |
| Power Dissipation $I_W = 29.5mA$, $I_B = 5.9mA$ | | | | | | | |
| 4-1 | Bank write enable voltage | V _{SEH} | | V _{CC} + 1.2 | | V _{CC} + 1.4 | V |
| 4-2 | Bank write enable current | I _{SEH} | | 6 | | 14 | mA |
| 5-1 | FLT output low voltage | V _{FLTL} | Open collector output External resistance = 2.4kΩ | | | 0.8 | V |
| 5-2 | FLT output high voltage | V _{FLTH} | Open collector output External resistance = 2.4kΩ | 4.5 | | | V |
| 6 | BHV gain accuracy | E _{BHV} | $V_{BHV} = V_{CC} - 4 \times I_B \times (R_{MR} + 5.5\Omega)$ $I_B = "111"$, $R_{MR} = 50\Omega$ | -8 | | 8 | % |

| No. | Item | Symbol | Measurement conditions | Min. | Typ. | Max. | Unit |
|---|---------------------------------------|------------|--|------|-------|------|------------------------|
| Read Characteristics $R_{MR} = 50\Omega$, $I_B = 5.9mA$ | | | | | | | |
| R1 | Low gain | A_{VL} | Gain = 0 $R_{MR} = 50\Omega$, $I_B = 5.9mA$ | 82 | 100 | 118 | V/V |
| R2 | High gain | A_{VH} | Gain = 1 $R_{MR} = 50\Omega$, $I_B = 5.9mA$ | 110 | 135 | 160 | V/V |
| R3 | Low frequency cut-off (-3dB) | F_{CL} | | | 350 | 550 | kHz |
| R4 | High frequency cut-off (-3dB) | F_{CH} | | 140 | 200 | | MHz |
| R5 | Input reflected noise | E_{Ni} | Exclusive of head noise $R_{MR} = 50\Omega$, $I_B = 5.9mA$ | | 0.77 | 0.95 | $\frac{nV}{\sqrt{Hz}}$ |
| R6 | MR bias current range 1 | I_{BR1} | | 3 | | 8 | mA |
| R7 | MR bias accuracy | E_{IB} | | -7 | | +7 | % |
| R8 | MR bias resolution | R_{IB} | 3-bit DAC | — | 0.714 | — | mA |
| R9-1 | V_{CC} power supply rejection ratio | $PSRR1$ | Ripple voltage: 100mVp-p 100kHz to 50MHz | 38 | | | dB |
| R9-2 | V_{EE} power supply rejection ratio | $PSRR2$ | Ripple voltage: 100mVp-p 100kHz to 10MHz | 45 | | | dB |
| R10-1 | Common mode rejection ratio 1 | $CMRR1$ | Ripple voltage: 100mVp-p 100kHz to 50MHz | 37 | | | dB |
| R10-2 | Common mode rejection ratio 2 | $CMRR2$ | Ripple voltage: 100mVp-p 51MHz to 80MHz | 27 | | | dB |
| R11 | Control line input noise rejection | $CLRR$ | Ripple voltage: 100mVp-p 4MHz to 80MHz | 40 | | | dB |
| R12 | RDX/RDY offset difference magnitude | V_{OFF1} | Write to read | | | 50 | mV |
| R13 | RDX/RDY output impedance | $RDro$ | Differential, read mode | 30 | | 100 | Ω |
| Read Safety Characteristics | | | | | | | |
| P1 | MR head open threshold | $MRop$ | Head X – Head Y | 600 | 750 | 900 | mV |
| P2 | MR head short threshold | $MRsh$ | Head X – Head Y $I_B = "000"$ to $"011"$ | 15 | 50 | 90 | mV |
| Write Characteristics | | | | | | | |
| W1 | Write current range | I_{WR} | DAC code = x "0000" to x "1111" | 19.5 | | 49.5 | mA |
| W2 | Write current accuracy | E_{IW} | $R_H = 0\Omega$ | -7 | | +7 | % |
| W3 | Write current resolution | R_{IW} | 4-bit DAC | — | 2 | — | mA |
| W4 | Leakage current | I_{LEAK} | Unselected head | | | 200 | μA |
| W6 | Damping resistor | R_D | | 800 | 1000 | 1200 | Ω |
| W7 | Write current propagation delay time | T_{pd} | $L_H = 0$, $R_H = 0$ Write data to 50% of write current | | | 10 | ns |
| W8 | Write current rise/fall time | T_R/T_F | $R_H = 15\Omega$, $L_H = 150nH$, $I_W = 25mA$ | — | 1.9 | — | ns |
| W9 | Erase current accuracy | E_{IE} | $V_{CC} = 3.5V$ DAC code = x "0101" | -18 | -9 | 0 | % |
| W10 | Bank write current accuracy | | Refer to Fig. | | | | |

| No. | Item | Symbol | Measurement conditions | Min. | Typ. | Max. | Unit |
|---|--|------------------------|--|------|------|----------|------|
| Write Safety Characteristics | | | | | | | |
| U1 | Write head open threshold | Rop | Detect open head | | 1.2 | 1.4 | V |
| U2 | Head voltage when short to GND | V _G | Detect short to GND | | | 0.1 | V |
| U3 | WD frequency too low | f _{WDL} | | 0.5 | | 1.8 | MHz |
| U4 | Write safety detect time | T _{WS} | T1: 2 transitions on WDX/WDY | | | 300 + T1 | ns |
| U5 | Low V _{CC} threshold | V _{WthL} | Fault detected | 3.7 | 3.9 | 4.1 | V |
| U6 | Low V _{CC} threshold | V _{WthH} | Fault removed | 3.9 | 4.1 | 4.3 | V |
| U7 | Low V _{CC} threshold hysteresis | V _{hys} | | — | 200 | — | mV |
| Switching Characteristics I _w = 29.5mA, I _B = 5.9mA | | | | | | | |
| S1 | Write to Read | T _{WR} | Signal on WDX/WDY 90% RD signal or 10% I _w | | 300 | 500 | ns |
| S2 | Read to Write | T _{RW} | 90% I _w | | 50 | 70 | ns |
| S3 | Idle to Read | T _{IR} | 90% RD signal | | | 1.0 | μs |
| S4 | Sleep to Read | T _{SR1} | 90% RD signal, 90% I _B *1 I _B = "011" | | 600 | 2000 | μs |
| Bank Write Characteristics I _w = 29.5mA, I _B = 5.9mA | | | | | | | |
| S5 | Read to Bank write | T _{RB} | 90% I _w | | | 100 | ns |
| S6 | Bank write to Read | T _{BR} | 10% I _w | | | 100 | ns |
| S7 | Idle to Bank write Idle to Write | T _{IW} | 90% I _w | | | 300 | μs |
| Serial Port Timing | | | | | | | |
| B1 | Setup time | T _{SU} (sden) | SDEN to first SCLK | 30 | | | ns |
| B2 | Hold time | T _H (sden) | Last SCLK to deassert SDEN | 15 | | | ns |
| B4 | SCLK frequency | f (sclk) | | | | 30 | MHz |
| B5 | SCLK pulse width | T _w (sclk) | | 10 | | | ns |
| B6 | SCLK – SDATA setup time | T _{SU} (d) | | 10 | | | ns |
| B7 | SCLK – SDATA hold time | T _H (d) | | 10 | | | ns |
| B8 | SDEN low time | T _{SL} | | 100 | | | ns |

*1 T_{SR} is proportional to I_B and external CAP value.

Serial Port Characteristics

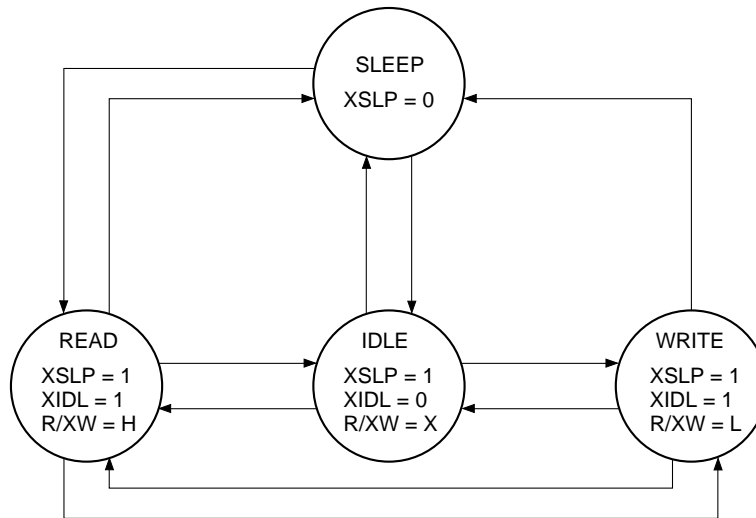
| ADR1 | ADR0 | DATA5 | DATA4 | DATA3 | DATA2 | DATA1 | DATA0 |
|------|------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | XSLP | XIDL | N/A | N/A | N/A | HS |
| 0 | 1 | GAIN | BHV | N/A | IB2 | IB1 | IB0 |
| 1 | 0 | MROPN | MRSHT | IW3 | IW2 | IW1 | IW0 |

* IB[2:0] bits are initialized by "0" at power on.

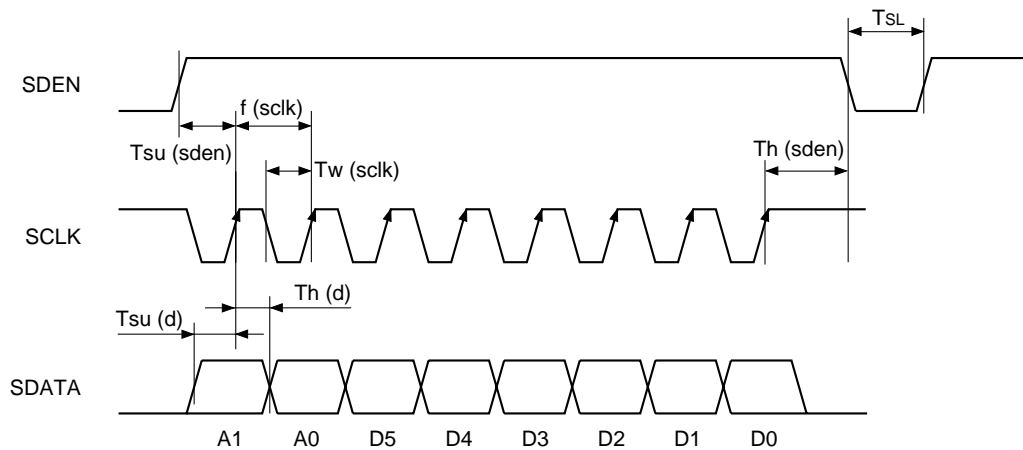
Code Description

| Bit | Function |
|---------|--|
| XSLP | 0 = Set the pre-amplifier into low power "sleep" mode. |
| XIDL | 0 = Set pre-amplifier to idle mode. |
| HS | Head select bit. |
| GAIN | Set the pre-amplifier to high or low gain mode. 1 = Set pre-amplifier to high gain mode. |
| BHV | Active the BHV test point pin. "1" active. |
| IB[2:0] | MR bias current set. |
| MROPN | 1 = Set MR head open detector active. |
| MRSHT | 1 = Set MR head short detector active. |
| IW[3:0] | Set write current. |

Mode Control



Serial Port Timing Detail



Serial Port Timing

After the SDEN goes high, the last eight bits are transferred into the register. The SCLK will shift the data presented at SDATA into an internal shift register on the rising edge of each clock. As SCLK initial condition, both of low and high signal is acceptable.

Unsafe Condition

1. Write fault condition
FLT is a high level in write fault condition.
 - Open write head leads. $f_{WD} < 15\text{MHz}$
 - Write head leads shorted to ground.
 - WD frequency is too low.
 - Power supply is out of tolerance.
2. Read fault condition
FLT is a low level in read fault condition.
 - Open short MR head. (This function is set by serial resistor.)

Bank Write Control (Refer to Bank "Write current vs. Current accuracy" characteristic curve)

1. Set the read mode.
2. Force a certain voltage (min. $V_{CC} + 1.2\text{V}$) to FLT/SE pin by using the pull-up register. ($R_{SE} = 820\Omega$)
#This operation disables all fault detection.
3. Set V_{CC} at 3.5V (in case of the erase mode only)
4. Start the write operation by setting R/XW = L.
5. Terminate the write operation by setting R/XW = H.
 - i) Allow 50% write duty or less.
 - ii) Low voltage detector is disabled in the bank write mode and erase mode.
 - iii) Don't change the serial register data bits in following conditions:
 - $V_{CC} = 3.5\text{V}$
 - On entering write data.

BHV (Buffered Head Voltage)

1. Applicable within $V_{CC} = 5\text{V} \pm 5\%$.
2. Turn BHV on, but turn off MROPN and MRSHT.
3. V_{BHV} is determined by basis of V_{CC} . $V_{BHV} = V_{CC} - (4 \times I_B \times (R_{MR} + 5.5\Omega))$

Head Condition

1. Short X-Y terminal on un-used write head.
2. Recommended X-Y terminal on un-used read head short.

Polarity

1. Read output signal on RDX is negative, when MRX is positive by increasing R_{MR} .
2. Write current flows into X side, when WDX is high and WDY is low.

Head Select Table**(2ch)**

| HS | Normal operation |
|----|------------------|
| 0 | 0 |
| 1 | 1 |

MR Bias

| IB2 | IB1 | IB0 | I _B [mA] |
|-----|-----|-----|---------------------|
| 0 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 3.714 |
| 0 | 1 | 0 | 4.429 |
| 0 | 1 | 1 | 5.143 |
| 1 | 0 | 0 | 5.857 |
| 1 | 0 | 1 | 6.571 |
| 1 | 1 | 0 | 7.286 |
| 1 | 1 | 1 | 8.0 |

Write Current

| IW3 | IW2 | IW1 | IW0 | Write current [mA _{0-P}] |
|-----|-----|-----|-----|------------------------------------|
| 0 | 0 | 0 | 0 | 19.5 |
| 0 | 0 | 0 | 1 | 21.5 |
| 0 | 0 | 1 | 0 | 23.5 |
| 0 | 0 | 1 | 1 | 25.5 |
| 0 | 1 | 0 | 0 | 27.5 |
| 0 | 1 | 0 | 1 | 29.5 |
| 0 | 1 | 1 | 0 | 31.5 |
| 0 | 1 | 1 | 1 | 33.5 |
| 1 | 0 | 0 | 0 | 35.5 |
| 1 | 0 | 0 | 1 | 37.5 |
| 1 | 0 | 1 | 0 | 39.5 |
| 1 | 0 | 1 | 1 | 41.5 |
| 1 | 1 | 0 | 0 | 43.5 |
| 1 | 1 | 0 | 1 | 45.5 |
| 1 | 1 | 1 | 0 | 47.5 |
| 1 | 1 | 1 | 1 | 49.5 |

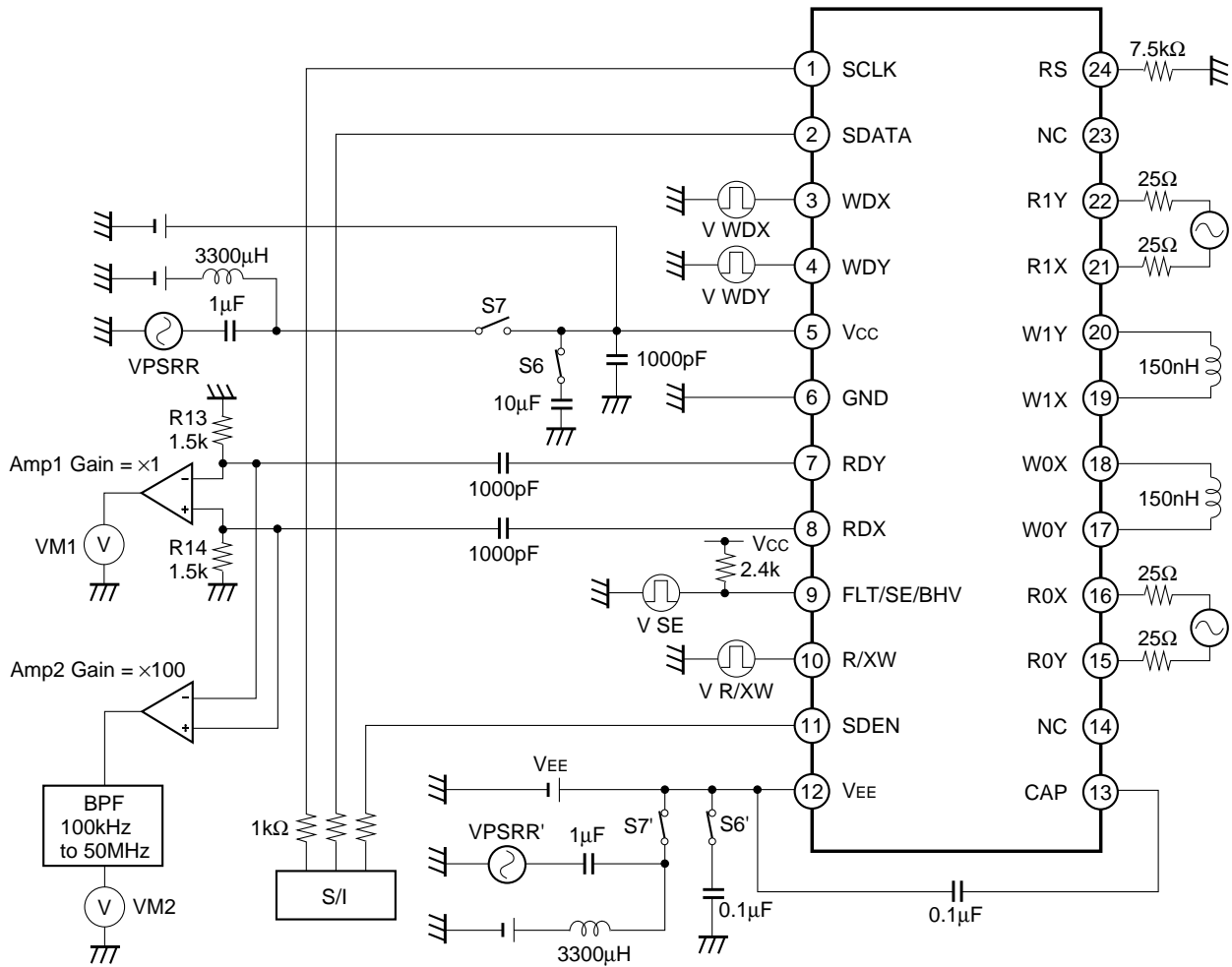
Actual head current is defined by the following equation:

$$I_{\text{HEAD}} = I_w / (1 + R_H/R_D)$$

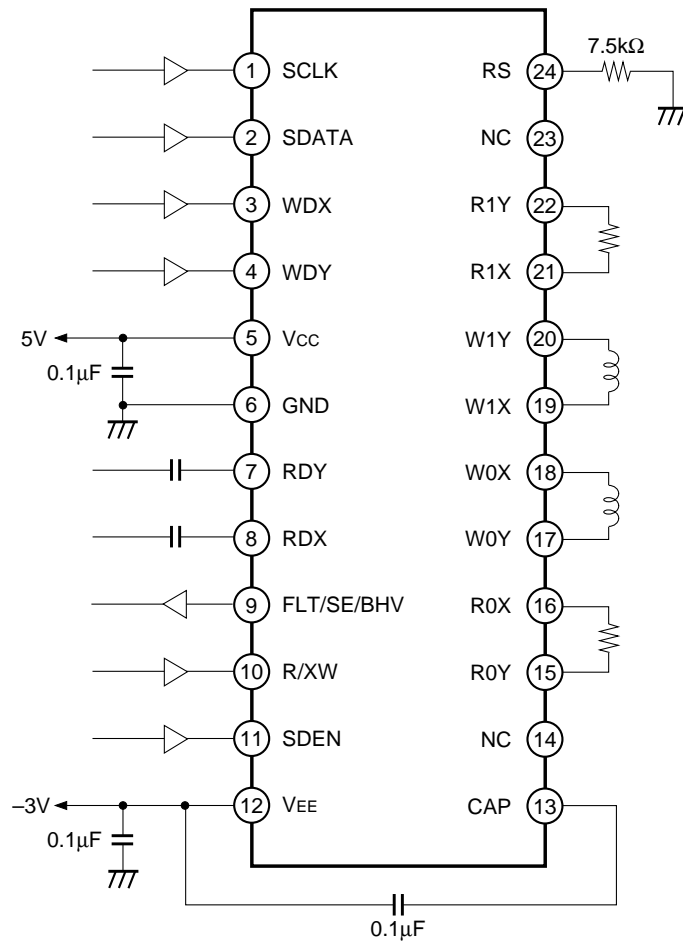
R_H: Head resistance

R_D: Damping resistance

Electrical Characteristics Measurement Circuit

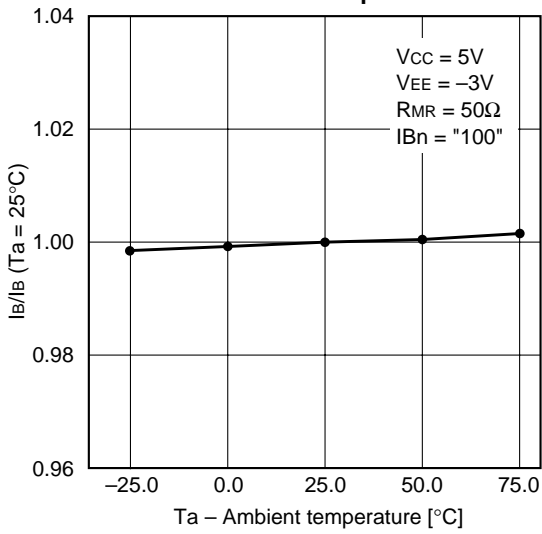


Application Circuit

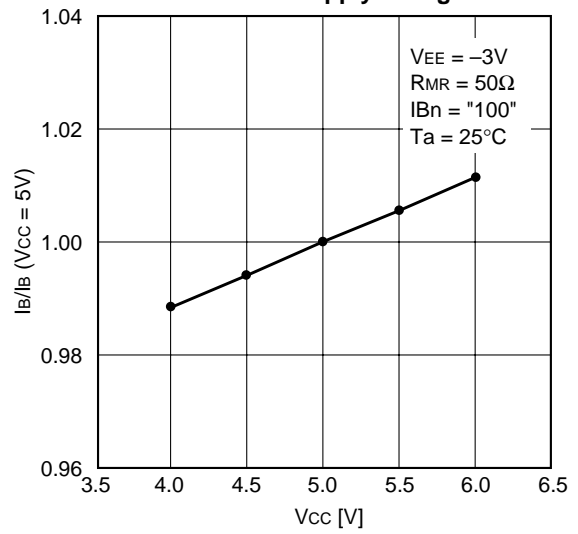


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

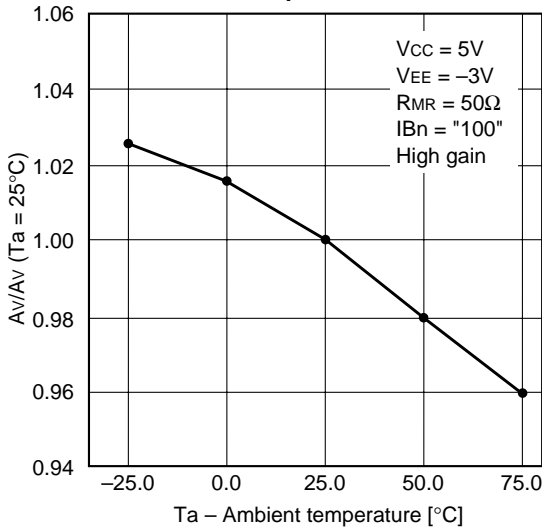
Normalized bias current vs. Ambient temperature



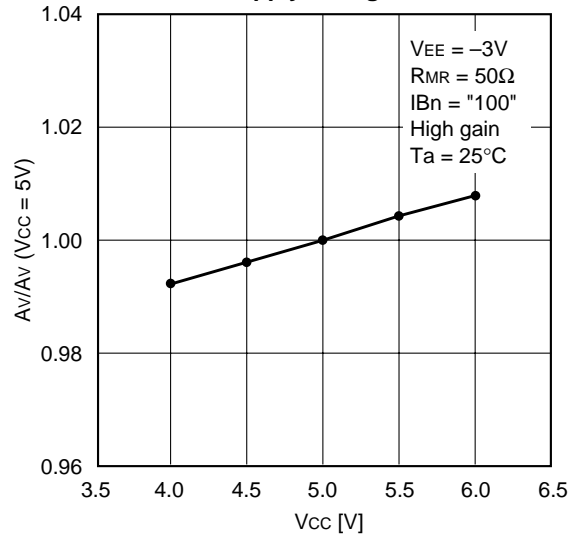
Normalized bias current vs. Power supply voltage



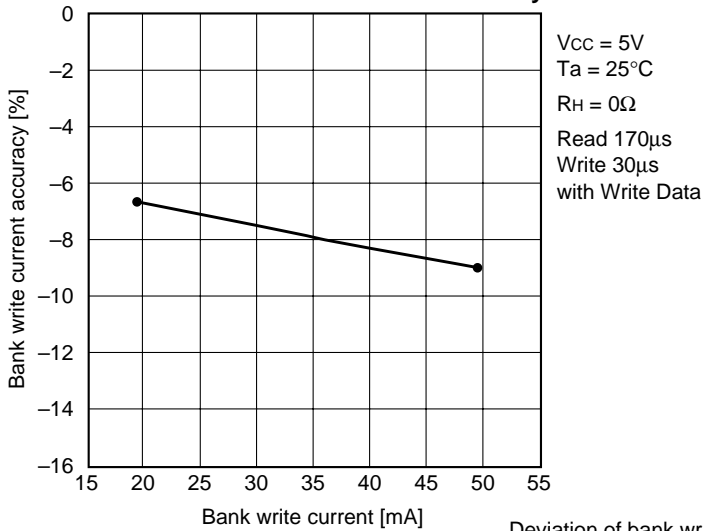
Normalized read amplifier voltage gain vs. Ambient temperature



Normalized read amplifier voltage gain vs. Power supply voltage

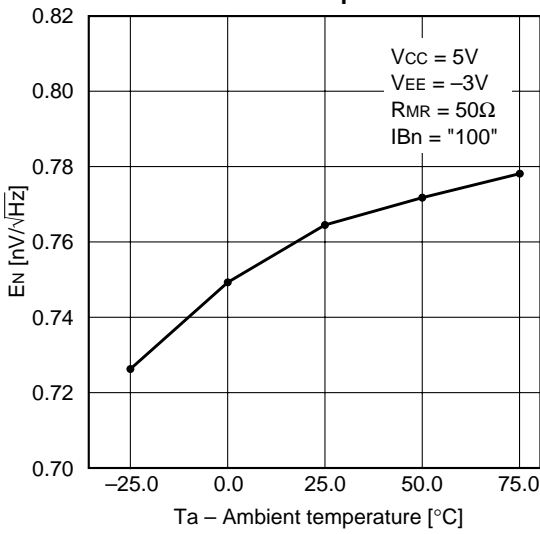


Bank write current vs. Current accuracy

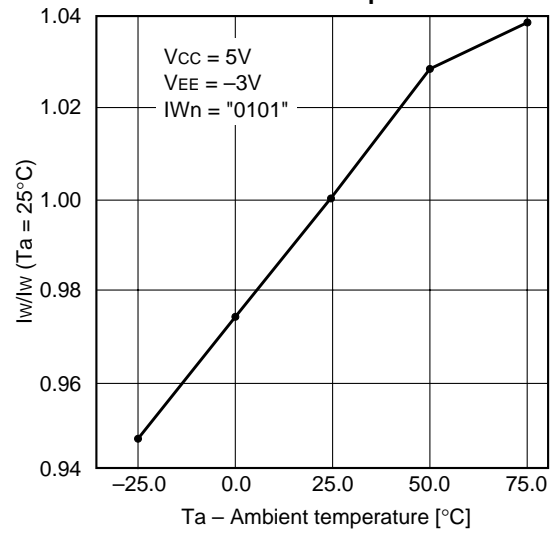


Deviation of bank write current is within ± 7% at basis of the chart.

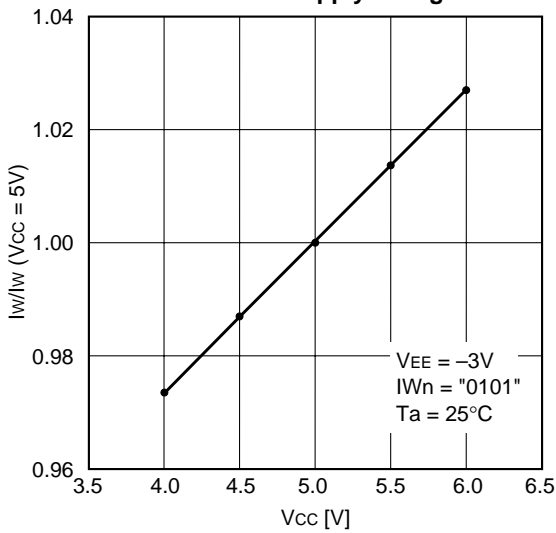
Input referred noise voltage vs. Ambient temperature



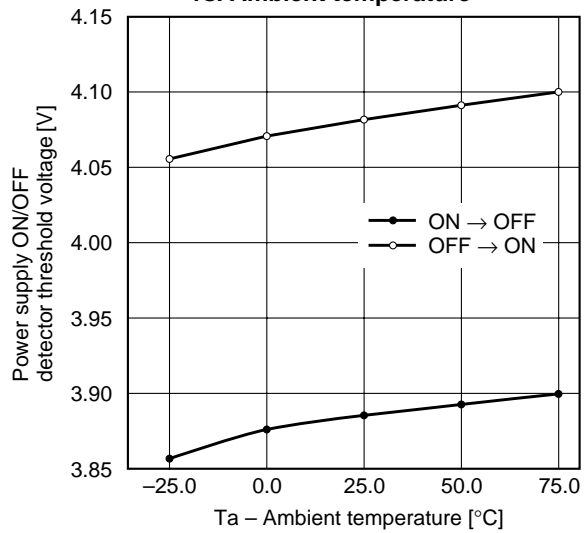
Normalized write current vs. Ambient temperature



Normalized write current vs. Power supply voltage



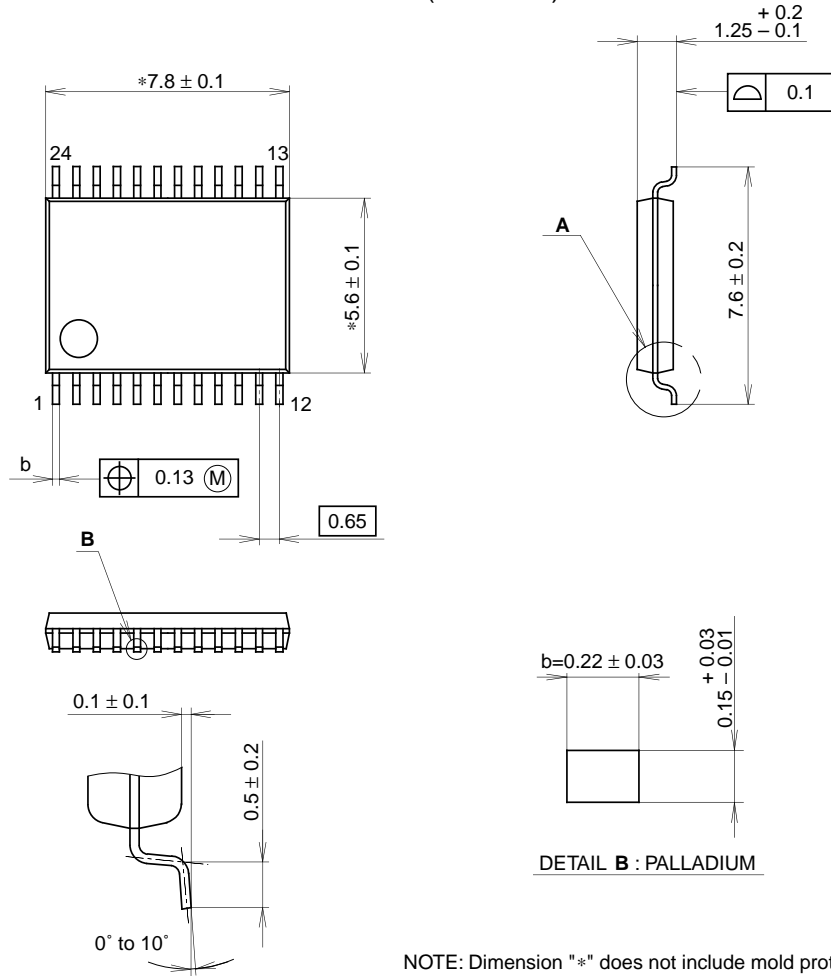
Power supply ON/OFF detector threshold voltage vs. Ambient temperature



Package Outline

Unit: mm

24PIN SSOP (PLASTIC)



DETAIL A

DETAIL B : PALLADIUM

NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

| | |
|------------|-----------------------|
| SONY CODE | SSOP-24P-L01 |
| EIAJ CODE | P-SSOP24-7.8x5.6-0.65 |
| JEDEC CODE | _____ |

| | |
|------------------|-------------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | PALLADIUM PLATING |
| LEAD MATERIAL | COPPER ALLOY |
| PACKAGE MASS | 0.1g |