MICRO NETWORKS

ADS574

25μsec, 12-Bit
SAMPLING A/D CONVERTER

FEATURES

- **Low Cost**
- **Pin-Compatible with MN574/674/774**
- **Eliminates External S/H in Most Applications**
- **Complete, 25μsec, 12-Bit A/D Converter with Internal**
  - **Clock**
  - **Reference**
  - **Control Logic**
- **Full 8- or 16-Bit μP Interface:**
  - **3-State Output Buffer**
  - **Chip Select, Address Decode**
  - **Read/Write Control**
- **No-Missing-Codes Guaranteed Over Temperature**
- **Single +5V Supply Operation**
- **Low Power: 120mW Max**
- **Package Options**
  - **0.3" Plastic DIP**
  - **0.3" Hermetic DIP**
  - **0.6" Plastic DIP**
  - **0.6" Hermetic DIP**
  - **SOIC**

DESCRIPTION

The ADS574 is a complete, low-cost, 12-bit successive-approximation A/D converter with an internal sample/hold function. In most existing applications, it is drop-in compatible with non-sampling 574 types, and eliminates the need for an external S/H amplifier. The ADS574 uses an innovative, capacitor-array internal D/A converter, based on CMOS technology. The use of a CMOS architecture results in much lower power consumption and the ability to operate from a single +5V supply (the formerly required −12V or −15V supply is optional, depending on the application).

The ADS574 is complete with internal clock, reference, control logic, and 3-state output buffer. The interface logic provides for easy handshaking with most popular 8- and 16-bit microprocessors. The ADS574's 3-state output buffer connects directly to the μP's data bus, and is readable as either one 12-bit word or two 8-bit bytes. Chip select, chip enable, address decode (for short cycling), and read/write (read/convert) control inputs enable the ADS574 to connect directly to a system address bus and control lines, and to operate totally under processor control.

Internal scaling resistors allow a pin-selectable choice of four input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. The maximum throughput time (including both acquisition and conversion) for 12-bit conversions is 25μsec over the full operating-temperature range. The ADS574 is available for operation over the commercial (0°C to +70°C) and military (-55°C to +125°C) temperature ranges. Package options include 28-pin single (0.300) or double (0.600) plastic or hermetic ceramic DIPs, and 28-pin plastic SOIC. For availability of devices screened to MIL-STD-883, consult factory.

Model Number	Package	Temperature Range	Linearity Error Max (T_{min} to T_{max})
ADS574JE	0.3" Plastic DIP	0°C to +70°C	±1LSB
ADS574KE	0.3" Plastic DIP	0°C to +70°C	±½LSB
ADS574JP	0.6" Plastic DIP	0°C to +70°C	±1LSB
ADS574KP	0.6" Plastic DIP	0°C to +70°C	±½LSB
ADS574JU	SOIC	0°C to +70°C	±1LSB
ADS574KU	SOIC	0°C to +70°C	±½LSB
ADS574JH	0.6" Ceramic DIP	0°C to +70°C	±1LSB
ADS574KH	0.6" Ceramic DIP	0°C to +70°C	±½LSB
ADS574SF	0.3" Ceramic DIP	−55°C to +125°C	±1LSB
ADS574TF	0.3" Ceramic DIP	−55°C to +125°C	±¾LSB
ADS574SH	0.6" Ceramic DIP	−55°C to +125°C	±1LSB
ADS574TH	0.6" Ceramic DIP	−55°C to +125°C	±¾LSB

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

ADS574 12-Bit SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	
J, K Grades	−40°C to +85°C
S, T Grades	−55°C to +125°C
Specified Temperature Range:	
J, K Grades	0°C to +70°C
S, T Grades	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} to Digital Ground	0 to −16.5V
V_{DD} to Digital Ground	0 to +7V
Analog Ground to Digital Ground	±1V
Control Inputs (CE, CS, A_0, 12/8, R/C) to Digital Ground	−0.5V to V_{DD} to +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$) to Analog Ground	±16.5V
$20V_{IN}$ to Analog Ground	±24V
Ref Out	Indefinite Short to Ground, Momentary
	Short to V_{DD}
Junction Temperature	+165°C
Lead Temperture (Soldering, 10 sec)	+300°C
Thermal Resistance Θ_{JA}: Ceramic	50°C/W
Plastic	100°C/W

ORDERING INFORMATION

PART NUMBER — ADS574 T H

Select suffix J, K, S or T for desired performance and specific temperature range.

Select suffix E, F, H, P or U for desired package option.

DESIGN SPECIFICATIONS ALL UNITS ($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = −15V to +5V, f_S = 40kHz, f_{IN} = 10kHz) (unless otherwise indicated)

	MIN.	TYP.	MAX.	UNITS
ANALOG INPUTS				
Input Voltage Range: Unipolar		0 to +10, 0 to +20		Volts
Bipolar		±5, ±10		Volts
Input Impedance: 0 to +10V, ±5V	15	21		kΩ
0 to +20V, ±10V	60	84		kΩ
DIGITAL INPUTS CE, CS, R/C, A_0, 12/8				
Logic Levels: Logic "1"	+2.0		+5.5	Volts
Logic "0"	−0.5		+0.8	Volts
Loading: Logic Current	−5		+5	μA
Input Capacitance		0.1		pF
		5		
DIGITAL OUTPUTS DB0 to DB11, Status				
Output Coding: Unipolar Ranges		Straight Binary		
(Note 1) Bipolar Ranges		Offset Binary		
Logic Levels: Logic "1" (I_{SOURCE} = 500μA)	+2.4			Volts
Logic "0" (I_{SINK} = 1.6mA)			+0.4	Volts
Leakage (DB0 to DB11) in High-Z State	−5	0.1	+5	μA
Output Capacitance		5		pF
INTERNAL REFERENCE				
Reference Output Voltage (Pin 8)	+2.4	+2.5	+2.6	Volts
Available Output Source Current	0.5			mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: V_{EE} Supply (Note 2)	−16.5		V_{DD}	Volts
Power Supply Range: V_{DD} Supply	+4.5		+5.5	Volts
Current Drains: I_{EE} (V_{EE} = −15V)		−1		mA
I_{DD}		+13	+20	mA
Power Dissipation				
V_{EE} = 0V to +5V		65	100	mW
DYNAMIC CHARACTERISTICS				
Sampling Rate (Max)	40			kHz
Aperture Delay t_{AP}				
With V_{EE} = +5V		20		nsec
With V_{EE} = 0V to −15V		4.0		μsec
Aperture Uncertainty (Jitter)				
With V_{EE} = +5V		300		psec rms
With V_{EE} = 0V to −15V		30		nsec rms
CONVERSION TIME (Including Acquisition Time)				
t_{AQ} + t_C at 25°C:				
8-Bit Cycle		16	18	μsec
12-Bit Cycle		22	25	μsec
12-Bit Cycle, T_{MIN} to T_{MAX}		22	25	μsec

PERFORMANCE SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = −15V to +5V, f_S = 40kHz, f_{IN} = 10kHz unless otherwise indicated)

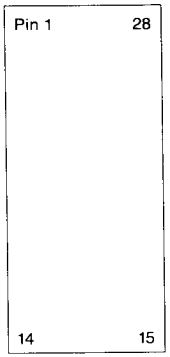
GRADE	ADS574J, S			ADS574K, T			
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
RESOLUTION			12			12	Bits
TRANSFER CHARACTERISTICS							
DC ACCURACY							
At 25°C:							
Linearity Error			±1			±½	LSB
Unipolar Offset Error (Notes 3, 4)			±2			±2	LSB
Bipolar Offset Error (Notes 3, 5)			±10			±4	LSB
Full-Scale Calibration Error (Notes 3, 6, 7)			±0.25			±0.25	%FSR
Inherent Quantization Uncertainty		±½			±½		LSB
T_{MIN} to T_{MAX}:							
Linearity Error: J, K, Grades			±1			±½	LSB
S, T Grades			±1			±¾	LSB
Full-Scale Calibration Error:							
Untrimmed: J, K Grades			±0.47			±0.37	%FSR
S, T Grades			±0.75			±0.5	%FSR
Trimmed to Zero at 25°C: J, K Grades			±0.22			±0.12	%FSR
S, T Grades			±0.5			±0.25	%FSR
Resolution for No Missing Codes	12			12			Bits
TEMPERATURE COEFFICIENTS (Note 8)							
Unipolar Offset			±5			±2.5	ppm/°C
Max. Change Over Temperature:			±2			±1	LSB
Bipolar Offset			±10			±5	ppm/°C
Max. Change Over Temperature: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration			±45			±25	ppm/°C
Max Change Over Temperature: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
AC ACCURACY (Note 9)							
Spurious-Free Dynamic Range	73	78		76	78		dB
Total Harmonic Distortion		−77	−72		−77	−75	dB
Signal-to-Noise Ratio	69	72		71	72		dB
Signal-to-(Noise+Distortion) Ratio (SINAD)	68	71		70	71		dB
Intermodulation Distortion		−75			−75		dB
(f_{IN1} = 10kHz; f_{IN2} = 11.5kHz)							
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration (Note 10)							
+4.75V < V_{DD} < +5.25V			±½			±½	LSB

SPECIFICATION NOTES:

1. See table of transition voltages in section labeled Digital Output Coding.
2. The use of V_{EE} is optional. This input sets the mode for the internal sample/hold circuit. When V_{EE} = −15V, I_{EE} = −1mA typ; when V_{EE} = 0V, I_{EE} = ±5μA typ; when V_{EE} = +5V, I_{EE} = +167μA typ.
3. Adjustable to zero with external potentiometer.
4. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when the ADS574 is operating with a unipolar range. The ideal value for this transition is +½LSB. See section labeled Digital Output Coding.
5. Bipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000 when the ADS574 is operating with a bipolar range. The ideal value for this transition is −½LSB. See section labeled Digital Output Coding.
6. Listed specs assume a fixed 50Ω resistor between Ref Out (Pin 8) and Ref In (Pin 10) and a fixed 50Ω resistor between Ref Out (Pin 8) and Bipolar Offset (Pin 12) in bipolar configurations; or Bipolar Offset grounded in unipolar configurations. Full-scale calibration error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111. The ideal value for this transition is 1½LSBs below the nominal full-scale voltage. See section labeled Digital Output Coding.
7. FSR is a full-scale range. For the ±10V input range, FSR is 20V. For the 0 to +10V input range, FSR is 10V.
8. Temperature coefficient specifications assume the use of the internal reference.
9. Specifications assume V_{EE} = +5V, which starts a conversion immediately upon a Convert command. If V_{EE} = 0V to −15V, the ADS574 emulates standard ADC574 operation. In this mode, the internal sample/hold circuit acquires the input signal after receiving the Convert command, and does not assume that the input level had been stable before the arrival of the Convert command.
10. Worst-case change in accuracy, compared with accuracy with a +5V supply.

Specifications are subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

PIN DESIGNATIONS



1	+5V Supply ($+V_{DD}$)	28	Status Output
2	Data Mode Select 12/$\overline{8}$	27	DB11 (MSB)
3	Chip Select $\overline{CS}$	26	DB10 (Bit 2)
4	Byte Address A_0	25	DB9 (Bit 3)
4	Read/Convert R/$\overline{C}$	24	DB8 (Bit 4)
6	Chip Enable CE	23	DB7 (Bit 5)
7	No Connect*	22	DB6 (Bit 6)
8	+2.5V Ref Out	21	DB5 (Bit 7)
9	Analog Ground	20	DB4 (Bit 8)
10	+2.5V Ref In	19	DB3 (Bit 9)
11	Mode Control V_{EE}	18	DB2 (Bit 10)
12	Bipolar Offset	17	DB1 (Bit 11)
13	10V Input	16	DB0 (LSB)
14	20V Input	15	Digital Ground

*No Internal Connection

DESCRIPTION OF OPERATION

The ADS574 is a complete 12-bit A/D converter. It uses the successive-approximation conversion technique and incorporates all required function blocks — capacitor-array D/A converter, comparator, clock, reference, and control logic. The CMOS-based capacitor-array architecture provides an inherent sample/hold function; the ADS574 is thus a sampling equivalent of the industry-standard 574 A/D converter. The device mates directly to most popular 8-, 16-, and 32-bit microprocessors and contains all the necessary address-decoding logic, control logic, and 3-state output buffering to operate completely under processor control. In most cases, the ADS574 will require only a power supply, a bypass capacitor, and two resistors to provide the complete A/D conversion function. The completeness of the device makes it most convenient to think of the ADS574 as a function block with specific input/output transfer characteristics; it is thus quite unnecessary to be concerned with its inner workings.

Operating the ADS574 under microprocessor control (note that it also functions as a stand-alone A/D) entails, in most applications, a series of read and write instructions. Initiating a conversion requires sending a command from the processor to the A/D, and also involves a write operation. Once the proper signals have been received and a conversion has begun, the ADS574 cannot be stopped or restarted, and digital output data is not available until the conversion has been completed. Immediately following the initiation of a conversion cycle, the ADS574's Status Output (also called Busy Line or End-of-Conversion (EOC) Line) rises to logic "1", indicating that a conversion is in progress. At the end of a conversion, the internal control logic will cause the Status Output to drop to 0, and will enable internal circuitry to allow reading output data by external command. By monitoring the state of the Status Output or by waiting an appropriate period of time, the microprocessor will know when the conversion is complete and that output data is valid and ready to be read.

If the ADS574 interfaces with 12-bit or wider microprocessors, it is possible to 3-state-enable all 12 output bits simultaneously, allowing data collection with a single read operation. If the ADS574 operates with an 8-bit processor, output data can be formatted to read in two 8-bit bytes. The first byte will contain the 8 most-significant bits (MSBs). The second byte will contain the remaining 4 least-significant bits (LSBs), in a left-justified format, with 4 trailing zeroes.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS AND GROUNDING — Proper attention to layout and decoupling is necessary to obtain specified performance from the ADS574. It is very important that the ADS574's power supply be filtered, well-regulated, and free from high-frequency noise. The use of a noisy supply may cause the generation of unstable output codes. It is advisable to bypass the +5V supply with a 10μF tantalum capacitor, located as close as possible to the converter. It is recommended to pay special attention to the avoidance of noise and spikes if a switching power supply is employed.

To avoid noise pickup, it is important to minimize coupling between analog inputs and digital signals. Pins 10 (Reference In), 12 (Bipolar Offset), and 13 and 14 (Analog Inputs) are particularly susceptible to noise. The circuit layout should be configured to locate the ADS574 and associated analog-input circuitry as far as possible from high-speed digital circuitry. The use of wire-wrap circuit construction is not recommended; careful printed-circuit construction is preferable. If external offset and gain-adjust potentiometers are used, the trimmers should be located as close to the ADS574 as possible. If no trims are required and fixed resistors are used, they should be situated as close to the converter as possible.

Analog (Pin 9) and Digital (Pin 15) Ground pins are not internally connected. It is advisable to tie them together as close to the converter as possible, preferably via a large analog ground plane beneath the package. If it is necessary to run these commons separately, it is recommended to connect a 10nF ceramic bypass capacitor between Pins 9 and 15, as close to the converter as possible. Pin 9 (Analog Ground) is the common reference point for the ADS574's internal reference. It should be connected as close as possible to the analog-input signal reference point.

CONTROL FUNCTIONS — Operating the ADS574 under microprocessor control is most easily understood by examining the various control-line functions in a truth table. Table 1 is a summary of the ADS574's control-line functions. Table 2 is the truth table that applies to these functions.

Unless Chip Enable (CE, Pin 6, logic "1" = active) and Chip Select ($\overline{CS}$, Pin 3, logic "0" = active) are both asserted, various combinations of logic signals applied to other control lines (R/$\overline{C}$, 12/$\overline{8}$, and A_0) will have no effect on the ADS574's operation. When CE and $\overline{CS}$ are both asserted, the signal applied to R/$\overline{C}$ (Read/Convert, Pin 5) determines whether a data Read (R/$\overline{C}$ = "1") or a Convert operation (R/$\overline{C}$ = "0") is initiated.

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" =read) ("0"=convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode. A_0 selects 8-bit (A_0="1") or 12-bit (A_0="0") conversion mode. When reading output data in 2 8-bit bytes. A_0="0" accesses 8 MSBs (high byte) and A_0="1" accesses 4 LSBs and trailing "0's" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1"=12 bits) ("0"=8 bits)	When reading output data, 12/$\overline{8}$="1" enables all 12 output bits simultaneously. 12/$\overline{8}$="0" will enable the MSbs or LSBs as determined by the A_0 line.

Table 1. ADS574 Control Line Functions

CONTROL INPUTS					ADS574 OPERATION
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	
O	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	1→0	X	0	Initiates 12-Bit Conversion
1	0	1→0	X	1	Initiates 8-Bit Conversion
0→1	0	0	X	0	Initiates 12-Bit Conversion
0→1	0	0	X	1	Initiates 8-Bit Conversion
1	1→0	0	X	0	Initiates 12-Bit Conversion
1	1→0	0	X	1	Initiates 8-Bit conversion
1	0	1	1	X	Enables 12-Bit Parallel Output
1	0	1	0	0	Enables 8 MSBs
1	0	1	0	1	Enables 4 LSBs and 4 Trailing Zeros

Table 2. Control Line Truth Table

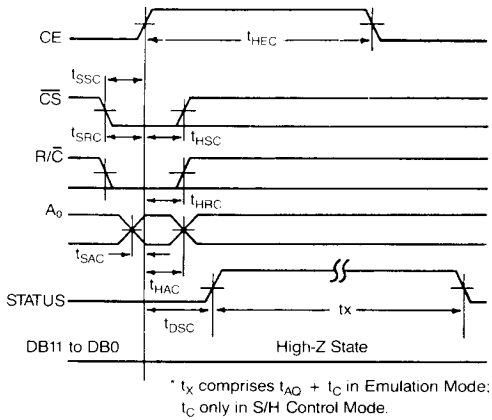
In the initiation of a conversion, the signal applied to A_0 (Byte Address/Short Cycle, Pin 4) determines whether a 12-bit conversion (A_0 = "0") or an 8-bit conversion (A_0 = "1") is initiated. It is the combination of CE = "1", $\overline{CS}$ = "0", R/$\overline{C}$ = "0", and A_0 = "1" or "0" that initiates a convert operation. The actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$, or the falling edge of R/$\overline{C}$, as shown in Table 2 and the section entitled "TIMING — INITIATING CONVERSIONS". In the initiation of a conversion, the 12/$\overline{8}$ line has "don't care" status.

When reading digital output data from the ADS574, it is necessary to assert CE and $\overline{CS}$. The signals applied to 12/$\overline{8}$ and A_0 will determine the format of the output data. Logic "1" applied to the R/$\overline{C}$ line will initiate actual output data access. If the 12/$\overline{8}$ line is at logic "1", all 12 output data bits will be accessed simultaneously when the R/$\overline{C}$ line's state changes from "0" to "1".

If the 12/$\overline{8}$ line is at logic "0", output data will be accessible as two 8-bit bytes as detailed in the section entitled "TIMING — READING OUTPUT DATA". In this situation, A_0 = "0" will result in accessing the 8 MSBs. In this mode, only the 8 upper bits or the 4 lower bits can be accessed at one time, as addressed by A_0. In these applications, the 4 LSBs (Pins 16 to 19) should be hard- wired to the 4 MSBs (Pins 24 to 27). Thus, during a read operation, when A_0 is low, the upper 8 bits are enabled and they present data on Pins 20 through 27. See the section entitled "HARD-WIRING TO 8-BIT DATA BUSES".

TIMING — INITIATING CONVERSIONS — It is the combination of CE = "1", $\overline{CS}$ = "0", R/$\overline{C}$ = "0", A_0 = "1" (initiate 8-bit conversion) or A_0 = "0" (initiate 12-bit conversion) that initiates a convert operation. As stated earlier, the actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$, or the falling edge of R/$\overline{C}$. Whichever occurs last will control the conversion; however, all three may occur simultaneously. The nominal delay time from either input transition to the beginning of the conversion (rising edge of Status) is the same for all three inputs (60 nsec typ). If it is desirable that a particular one of these three inputs be responsible for initiating the conversion, the other two should be unchanging for a minimum of 50 nsec prior to the transition of the chosen input.

Because the ADS574's control logic latches the A_0 signal upon the initiation of a conversion, the A_0 line should be stable immediately prior to whichever of the cited transitions is used to initiate the conversion. The R/$\overline{C}$ transition is normally used to initiate conversions in stand-alone operation; however, it is not recommended to use this line to initiate conversions in μP applications. If R/$\overline{C}$ is high just prior to a conversion, there will be a momentary enabling of output data as if a Read operation were occurring, and the result could be system bus contention. In most applications, A_0 should be stable and R/$\overline{C}$ low before either CE or $\overline{CS}$ is used to initiate a conversion.



* t_X comprises t_{AO} + t_C in Emulation Mode; t_C only in S/H Control Mode.

Figure 1. Convert Timing

Figure 1 shows timing for a typical application. In this application, $\overline{CS}$ is brought low, R/$\overline{C}$ is brought low, and A_0 is set to its chosen value prior to CE's 0-to-1 transition. The sequence can be accomplished in a number of ways, including connecting $\overline{CS}$ and A_0 to address bus lines, connecting R/$\overline{C}$ to a read/write line (or its equivalent), and generating 0-to-1 transition on CE using the system clock. In this example, $\overline{CS}$ should be at logic "0" 50 nsec prior to the CE transition (t_{SSC} = 50 nsec min), R/$\overline{C}$ should be at logic "0" 50 nsec prior to the CE transition (t_{SRC} = 50 nsec min), and A_0 should be stable 0 nsec prior to the CE transition (t_{SAC} = 0 nsec min). The minimum pulse width for CE ="1"is 50 nsec (t_{HEC} = 50 nsec min) and both $\overline{CS}$ and R/$\overline{C}$ must be valid for at least 50 nsec while CE ="1"(t_{HSC} and t_{HRC} = 50 nsec min) while CE is high to

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
t_{DSC}	STS Delay from CE		60	200	nsec
t_{HEC}	CE Pulse Width	50	30		nsec
t_{SSS}	$\overline{CS}$ to CE Setup	50	20		nsec
t_{HSC}	$\overline{CS}$ Low During CE High	50	20		nsec
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		nsec
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20		nsec
t_{SAC}	A_0 to CE Setup	0			nsec
t_{HAC}	A_0 Valid During CE High	50	20		nsec

Table 3. Convert Timing Parameters

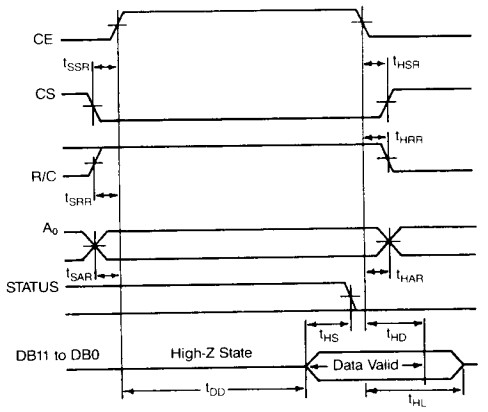


Figure 2. Read Timing

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
t_{DD}	Access Time from CE		75	150	nsec
t_{HD}	Data Valid after CE Low	25	35		nsec
t_{HL}	Output Float Delay		100	150	nsec
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		nsec
t_{SRR}	R/$\overline{C}$ to CE Setup	0			nsec
t_{SAR}	A_0 to CE Setup	50	25		nsec
t_{HSR}	$\overline{CS}$ Valid after CE Low	0			nsec
t_{HRR}	R/$\overline{C}$ High after CE Low	0			nsec
t_{HAR}	A_0 Valid after CE Low	50			nsec
t_{HS}	STS Delay after Delay Valid	300	400	1000	nsec

Table 4. Read Timing Parameters

effectively initiate the conversion. Similarly, A_0 must be valid for at least 50 nsec (t_{HAC} = 50 nsec min) while CE is high to effectively initiate the conversion. The Status line rises to a logic"1"no later than 200 nsec after the rising edge of CE (t_{DSC} = 200 nsec max). Once Status is at logic "1", additional convert commands will be ignored until the ongoing conversion is complete. Table 3 gives the limits for the convert timing parameters.

TIMING — RETRIEVING DATA — When a conversion is in progress (Status output = "1"), the ADS574's 3-state output buffer is in its high-impedance state. After the falling edge of Status indicates the conversion is complete, the combination of CE = "1", $\overline{CS}$ = "0", and R/$\overline{C}$ = "1" is used to activate the buffer and read the digital output data.

If the cited combination of control signals is satisfied and the 12/$\overline{8}$ line has logic "1" imposed, all 12 output bits will become valid simultaneously. If the 12/$\overline{8}$ line has logic "0" imposed, output data will be formatted for an 8-bit data bus.

Figure 2 shows timing for a typical application. In this application, $\overline{CS}$ is brought low, A_0 is set to its final state, and R/$\overline{C}$ is brought high, all before the rising edge of CE. $\overline{CS}$ and A_0 should be valid 50 nsec prior to CE (t_{SSR} and t_{SAR} = 50 nsec min). R/$\overline{C}$ can become valid at the same time as CE (t_{SRR} = 0 nsec min).

A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which ensures that the outputs strapped together in 8-bit bus applications will never be enabled at the same time.

Access time is measured from the point at which CE and R/$\overline{C}$ are both high (assuming $\overline{CS}$ is already low). Data actually becomes valid typically 400 nsec before the falling edge of Status, as indicated by t_{HS}. In most applications, the 12/$\overline{8}$ input will be hard-wired high or low; although it is fully TTL/CMOS compatible and may be actively driven. Table 4 gives the limits for the read timing parameters.

S/H CONTROL MODE AND NON-SAMPLING 574 EMULATION MODE — Figure 3 and Table 5 show the basic differences between the two operating modes. In both modes, the acquisition time is 4μsec typ. In the Control mode, during the 4μsec acquisition time, the input signal may not slew faster than the inherent slew rate of the ADS574. After the Convert command arrives, any changes in the input signal level have no effect on the conversion, as the input signal is already sampled and the conversion process begins immediately.

In the Control mode, a Convert command can provide some useful peripheral functions — for example, control an input MUX or a programmable-gain amplifier. In these applications, the input signal has time to settle before the subsequent acquisition occurs after the conversion. The internal sample/hold function keeps aperture jitter to a minimum; therefore, it is possible to digitize high input frequencies without the need for an external sample/hold amplifier.

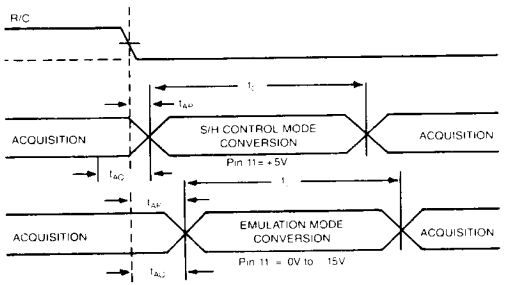


Figure 3. Signal Acquisition and Conversion Timing

SYMBOL	PARAMETER	S/H CONTROL TYP.	S/H CONTROL MAX.	EMULATION TYP.	EMULATION MAX.	UNITS
$t_{AQ}+t_C$	Throughput Times:					
	12-Bit Conversion	22	25	22	25	μsec
	8-Bit Conversion	16	18	16	18	μsec
t_C	Conversion Time:					
	12-Bit Conversion	18		18		μsec
	8-Bit Conversion	12		12		μsec
t_{AQ}	Acquisition Time	4		4		μsec
t_A	Aperture Delay	20		4000		nsec
t_J	Aperture Jitter	0.3		30		nsec

Table 5. Conversion Timing Over T_{MIN} to T_{MAX}

In the Emulation mode, the ADS574 introduces a delay time between the Convert command and the start of conversion, in order to allow the converter enough time to acquire the signal before the conversion. The delay causes an effective increase in aperture time from 0.02 μsec to 4 μsec, and allows the ADS574 to replace industry-standard, non-sampling 574 types in existing sockets. Slewing of the analog input prior to the Convert command has no effect on the accuracy of the ADS574. In both the Control and Emulation modes, the internal sample/hold circuit begins slewing to track the input signal immediately after the conversion is complete.

In the Emulation mode, the ADS574 can replace existing, non-sampling 574 types in almost all applications, without any changes in system hardware or software. It is not necessary that the input signal be stable before a Convert command arrives, but it must remain stable during the acquisition period after the Convert command is received (as it must with other 574 types) for accurate performance. Unlike other, non-sampling 574 types, the ADS574 allows the input to begin slewing before the end of conversion (after the 4μsec acquisition period), so it is possible to increase system throughput in many cases.

HARD-WIRING TO 8-BIT DATA BUSES — For applications with 8-bit data buses, output lines DB4 to DB11 (Pins 20 to 27) should connect directly to lines D_0 to D_7 in the system data bus. In addition, output lines DB0 to DB3 (Pins 16 to 19) should connect to lines D_4 to D_7 on the system data bus, and to ADS574 output lines DB8 to DB11 (Pins 24 to 27). Figure 4 shows the proper connections. Thus connected, if A_0 is low during a read operation, the upper 8 bits are enabled and become valid on output pins 20 to 27. When A_0 is high during an operation, the 4 LSBs are enabled on output pins 16 to 19 and the 4 middle bits (Pins 20 to 23) are overridden with zeros.

	D7	D6	D5	D4	D3	D2	D1	D0
High Byte (A_0 = 0)	MSB	DB10	DB9	DB8	DB7	DB6	DB5	DB4
Low Byte (A_0 = 1)	DB3	DB2	DB1	DB0	0	0	0	0

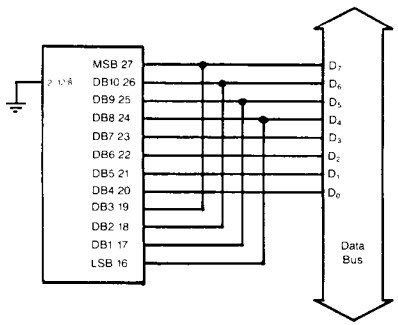


Figure 4. Connection to 8-Bit Bus

STAND-ALONE OPERATION — The ADS574 can be used in a stand-alone mode in systems having dedicated input ports and not requiring full bus-interface capability. In this mode, $\overline{CE}$ and 12/$\overline{8}$ are tied to logic "1" (they may be hard-wired to +5V), $\overline{CS}$ and A_0 are tied to logic "0" (they may be grounded), and the conversion is controlled by R/$\overline{C}$. A conversion is initiated whenever R/$\overline{C}$ is brought low (assuming a conversion is not already in progress), and all 12 bits of the 3-state output buffers are enabled whenever R/$\overline{C}$ is brought high (assuming Status has already gone low, indicating completion of conversion).

This configuration gives rise to two possible modes of operation. Conversions can be initiated with either positive or negative R/$\overline{C}$ pulses. Figure 5 details operation with a negative start pulse. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$, and they return to valid logic levels after the conversion cycle is completed. The Status output goes high 200 nsec after R/$\overline{C}$ goes low (t_{DS}) and returns low no longer than 1000 nsec after data is valid (t_{HS}). In this mode, output data is available most of the time, and becomes invalid only during a conversion.

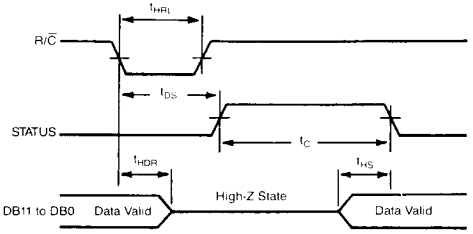


Figure 5. Stand Alone Mode With Negative Start Pulse.

Figure 6 details operation with a positive start pulse. Output data lines are enabled during the time R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion, and the data lines return to the high-impedance state and remain in that state until the next rising edge of R/$\overline{C}$. In this mode, output data is inaccessible most of the time, and becomes valid only when R/$\overline{C}$ goes high. Table 6 gives the timing parameters for the two modes.

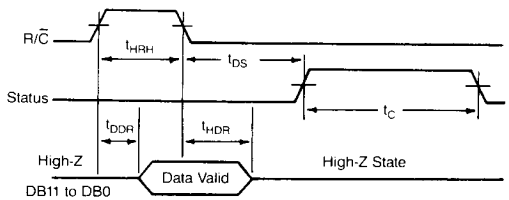


Figure 6. Stand-Alone Mode with Positive Start Pulse.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	25			nsec
t_{DS}	STS Delay after R/$\overline{C}$			200	nsec
t_{HDR}	Data Valid after R/$\overline{C}$ Low	25			nsec
t_{HRH}	High R/$\overline{C}$ Pulse Width	100			nsec
t_{DDR}	Data Access Time			150	nsec

Table 6. Stand-Alone Mode Timing over T_{MIN} to T_{MAX}

UNIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the unipolar operating mode are shown in Figure 7. If the 0 to +10V input range is to be used, apply the analog input to Pin 13. If the 0 to +20V input range is to be used, apply the analog input to Pin 14. If the gain adjustment is not needed, replace trim potentiometer R_2 with a fixed, 50Ω ±1% metal-film resistor to meet all published specifications. If the offset adjustment is not needed, connect Pin 12 (Bipolar Offset) directly to Pin 9 (Analog Ground).

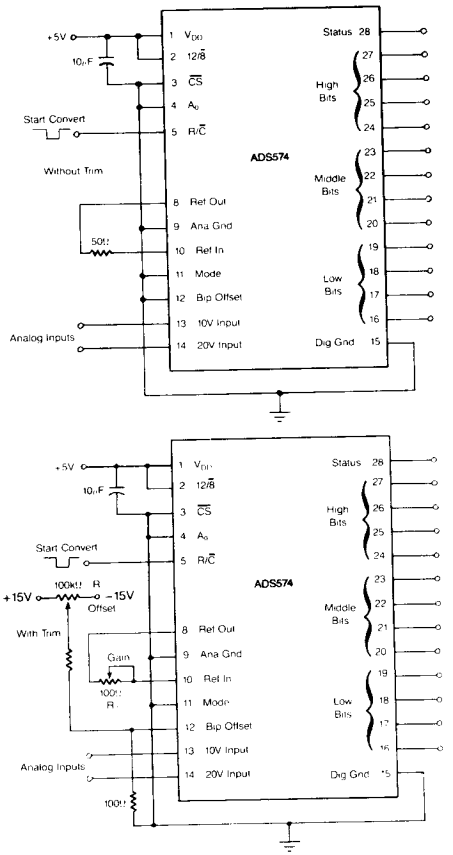


Figure 7. Unipolar Connections

Unipolar offset error refers to the accuracy of the 0000 0000 0000 to 0000 0000 0001 digital output transition (see section entitled "DIGITAL OUTPUT CODING"). If the offset adjustment is not used, the actual transition will occur within specified limits of its ideal value (+½LSB). For the 10V range, 1 LSB = 2.44mV. For the 20V range, 1 LSB = 4.88mV. To adjust the offset, apply an analog input equal to +½LSB and, with the ADS574 continuously converting, adjust the offset potentiometer "down" until the digital output is all ones, and then adjust "up" until the LSB "flickers" between "0" and "1".

Unipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after the unipolar offset adjustment has been effected. Ideally, this transition should occur 1½LSBs below the nominal full-scale voltage for the selected input range. This corresponds to +9.9963V and +19.9927V, respectively, for the 10V and 20V unipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain potentiometer "up" until the digital outputs are all ones, and then adjusting "down" until the LSB "flickers" between "0" and "1".

In some applications, it is desirable to have the LSB equal exactly 2.5mV (10.24V input range) or 5mV (20.48V input range). To implement these ranges, replace the 100 gain trimpot by a 50Ω fixed resistor. Then insert a 2.7kΩ trimpot in series with Pin 13 for a 10.24V range; Pin 14 for a 20.48V range. Offset trimming then proceeds as described earlier, and the gain trim is effected with the new trimpot.

BIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the bipolar operating mode are shown in Figure 8. If the ±5V input range is to be used, apply the analog input to Pin 13. If the ±10V range is to be used, apply the analog input to Pin 14. If either bipolar offset or bipolar gain adjustments are not to be used, the trimpots should be replaced by fixed, 50Ω ±1% metal-film resistors to meet all published specifications.

Bipolar offset error refers to the accuracy of the 0111 1111 1111 to 1000 0000 0000 digital output transition (see section entitled "DIGITAL OUTPUT CODING"). Ideally, this transition should occur ½LSB below 0V, and if the bipolar offset adjustment is not used, the transition will occur within the specified limit of its ideal value. Offset adjustment in the bipolar configuration is performed not at the zero-crossing point but at the minus full-scale point. The procedure is to apply an analog input equal to −FS + ½LSB (−4.9988V for the ±5V range; −9.9976V for the ±0V range), and adjust the bipolar offset trimpot "down" until the digital output is all zeros. Then adjust "up" until the LSB "flickers" between "0" and "1".

Bipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after the bipolar offset adjustment has been effected. Ideally, this transition should occur 1½LSBs below the nominal positive full-scale value of the selected input range. This corresponds to +4.9963V and +9.9927V for the ±5V and ±10V ranges, respectively. Gain trimming is accomplished by applying either of these voltages and adjusting the gain trimpot "up" until the digital outputs are all ones, then adjusting "down" until the LSB "flickers" between "1" and "0".

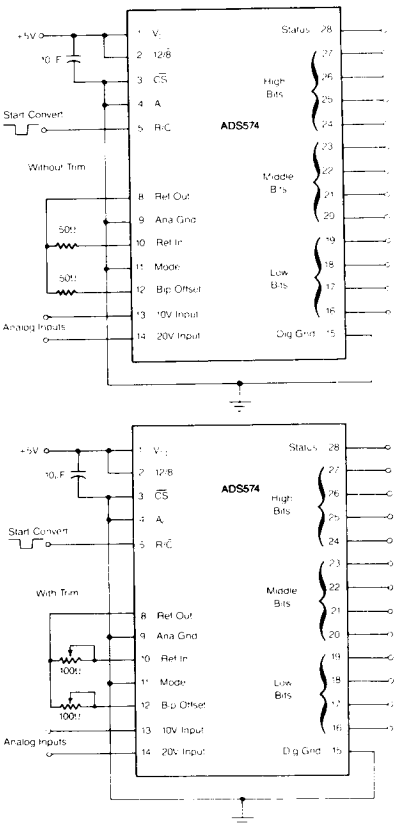


Figure 8. Bipolar Connections

DIGITAL OUTPUT CODING

ANALOG INPUT VOLTAGE (Volts)				DIGITAL OUTPUT
0 to +10V	0 to +20V	±5V	±10V	MSB LSB
+10.0000	+20.0000	+5.0000	+10.0000	1111 1111 1111
+9.9963	+19.9927	+4.9963	+9.9927	1111 1111 111Ø *
+5.0012	+10.0024	+0.0012	+0.0024	1000 0000 000Ø *
+4.9988	+9.9976	−0.0012	−0.0024	0000 0000 0000 *
+4.9963	+9.9927	−0.0037	−0.0073	0111 1111 111Ø *
+0.0012	+0.0024	−4.9988	−9.9976	0000 0000 000Ø *
0.0000	0.0000	−5.0000	−10.0000	0000 0000 0000

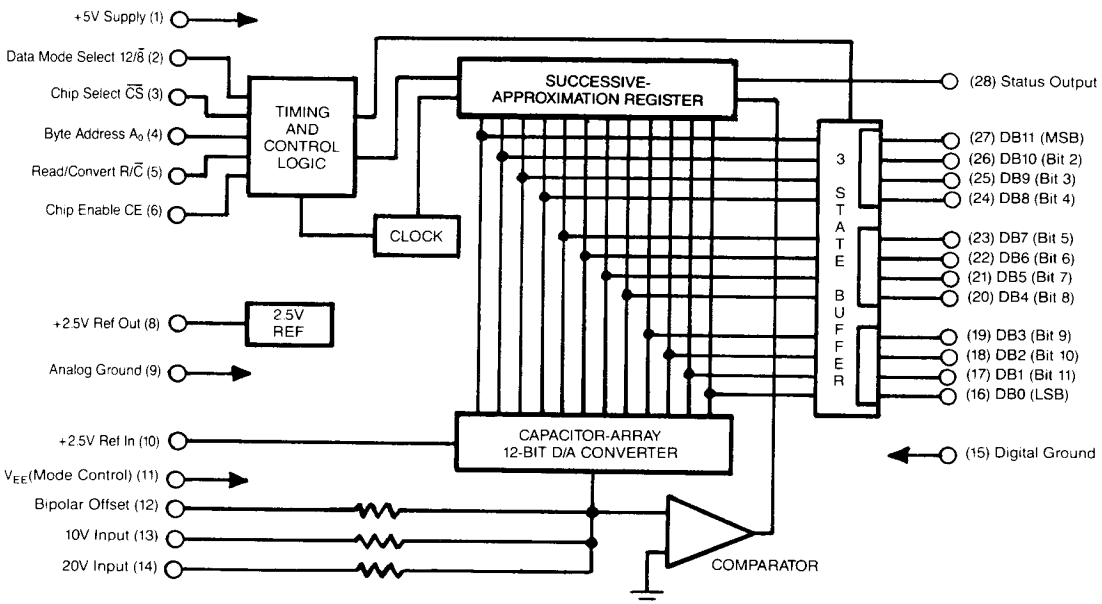
DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to +10V or ±5V input ranges, 1LSB for 12 bits =2.44mV. 1LSB for 11 bits =4.88mV.
4. For 0 to +20V or ±10V input ranges, 1LSB for 12 bits =4.88mV. 1LSB for 11 bits =9.77mV.

*Voltages given are the theoretical values for the transition indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

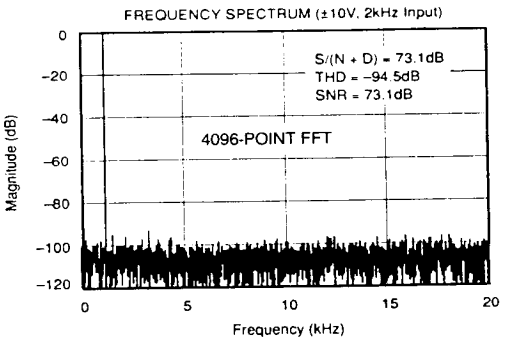
EXAMPLE: For an ADS574 operating on its ±10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of −9.9976 volts. Subsequently, any input voltage more negative than −9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of −0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at +9.9927 volts. An input more positive than +9.9927 volts will give all "1's".

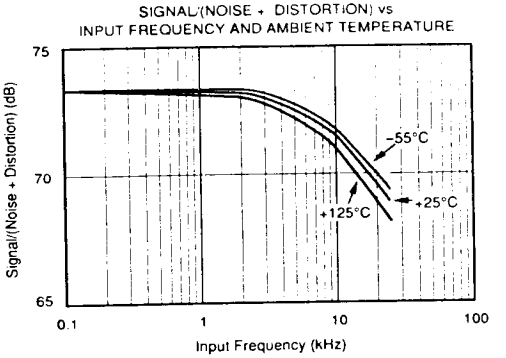
ADS574 BLOCK DIAGRAM

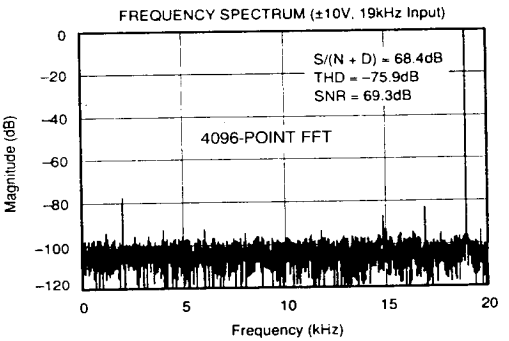


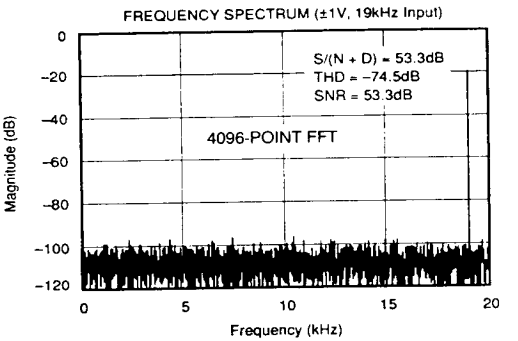
TYPICAL PERFORMANCE

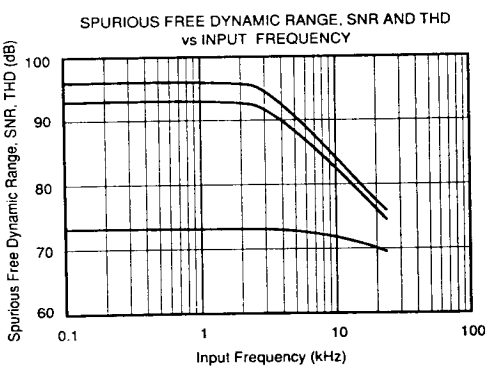
(T_A =25°C, Supplies = +5V, ±10V Bipolar Input, f_{IN} =40kHz, unless otherwise indicated)

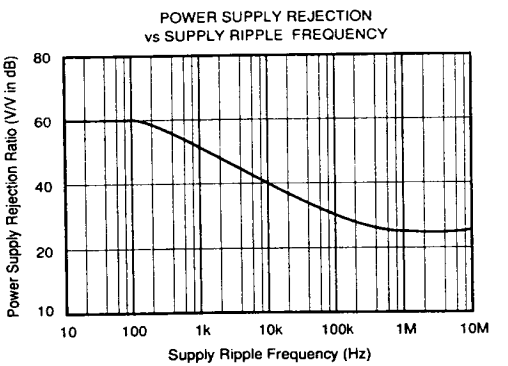




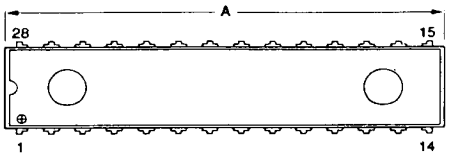






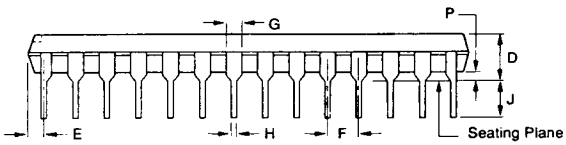


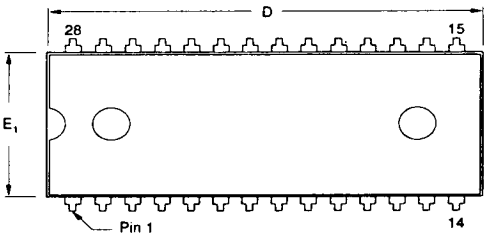
PACKAGE OUTLINES



PACKAGE E. PLASTIC SINGLE DIP

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.255	1.355	31.88	34.42
B	.270	.290	6.86	7.37
D	.150	.170	3.81	4.32
E	.010	.080	0.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.045	.055	1.14	1.40
H	.016	.020	0.41	0.51
J	.125	N/A	3.18	N/A
K	.300 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.020	.040	0.51	1.02

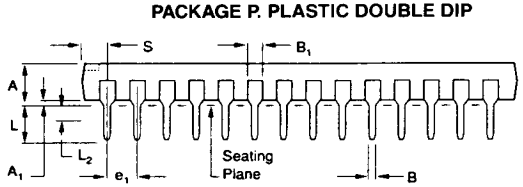


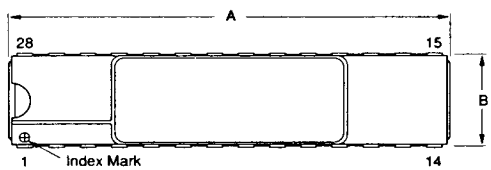


PACKAGE P. PLASTIC DOUBLE DIP

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A[1]	.169	.200	4.29	5.08
A_1[1]	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B_1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D[1]	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E_1[1]	.485	.550	12.32	13.97
e_1	.100 BASIC		2.54 BASIC	
e_A	.600 BASIC		15.24 BASIC	

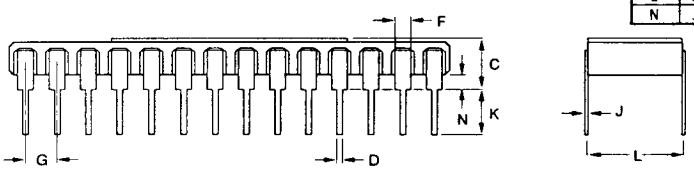
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
L	.100	.200	2.54	5.08
L_2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
S[1]	.040	.080	1.02	2.03



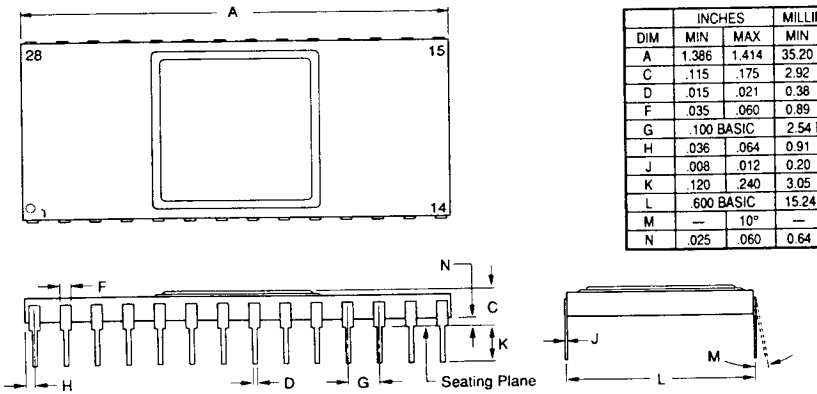


PACKAGE F. CERAMIC HERMETIC SINGLE DIP

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.388	1.412	35.26	35.86
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 BASIC		1.27 BASIC	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52

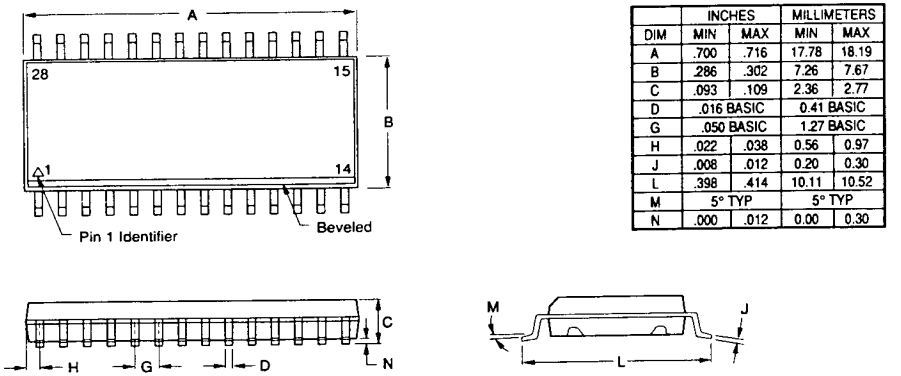


PACKAGE H. CERAMIC HERMETIC DOUBLE DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.386	1.414	35.20	35.92
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

PACKAGE U. PLASTIC SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.700	.716	17.78	18.19
B	.286	.302	7.26	7.67
C	.093	.109	2.36	2.77
D	.016 BASIC		0.41 BASIC	
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.398	.414	10.11	10.52
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30