REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
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SHEET	15	16	17	18															

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE
AMSC N/A

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DRAWING APPROVAL DATE
93-10-18

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, COORDINATE TRANSFORMER, 16X16 BIT, MONOLITHIC SILICON

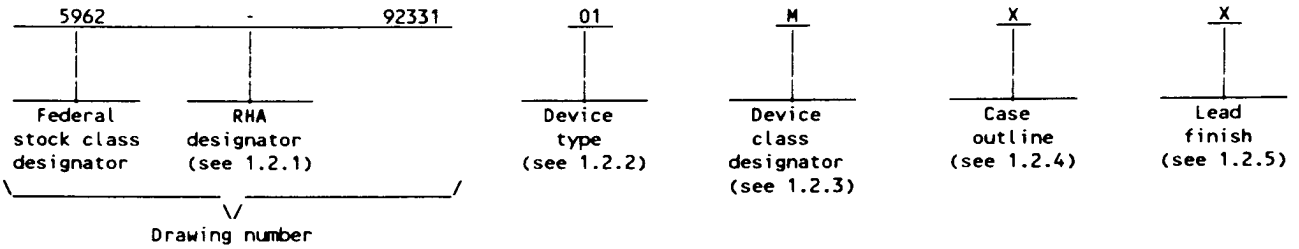
SIZE	CAGE CODE	
A	67268	5962-92331

SHEET 1 OF 18

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TMC2330V	CMOS Coordinate Transformer, 16 x 16 Bit, 55 ns
02	TMC2330V1	CMOS Coordinate Transformer, 16 x 16 Bit, 45 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA5-P120	120	Pin grid array
Y	CQCC1-G132	132	Gullwing leaded chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply Voltage range	-0.5V dc TO 7.0V dc
Input Voltage range	-0.5V dc to V_{DD} +0.5 V dc
Applied output voltage range 2/	-0.5V dc to V_{DD} +0.5V dc
Forced output current 3/	-6.0 mA to 12.0 mA
Output short circuit duration 4/	1 second
Power dissipation, unloaded (P_D)	975 mW
Junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	4.5V dc to 5.5V dc
Input LOW voltage (V_{IL})	.8V dc maximum
Input HIGH voltage (V_{IH})	2.0V dc minimum
Input LOW current (I_{OL})	8 mA maximum
Input HIGH current (I_{OH})	-4 mA minimum
Cycle time (T_{CY})	
Device type 01	55 ns minimum
Device type 02	45 ns minimum
Clock pulse width, LOW (T_{PWL})	
Device type 01	11 ns minimum
Device type 02	8 ns minimum
Clock pulse width, HIGH (T_{PWH})	
Device type 01	8 ns minimum
Device type 02	6 ns minimum
Data Input setup time (t_S)	
Device type 01	13 ns minimum
Device type 02	11 ns minimum
Data Input hold time (t_H)	2 ns minimum
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 5/

1/ Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT applied.

2/ Applied voltage must be current limited to specified range, and measured with respect to GND.

3/ Forcing voltage must be limited to specified range.

4/ Single output in HIGH state to GND.

5/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Quiescent supply current	I_{DDQ}	V_{DD} = 5.5 V, V_{in} = 0V	1,2,3	ALL		10	mA
Dynamic supply current, unloaded	I_{DDU}	V_{DD} = 5.5 V, f = 20 MHZ $\overline{OERX}$, $\overline{OEPY}$ = V_{DD}	1,2,3	ALL		175	mA
Input LOW current	I_{IL}	V_{DD} = 5.5 V, V_{in} = 0V	1,2,3	ALL	-10	10	µA
Input HIGH current	I_{IH}	V_{DD} = 5.5 V, V_{in} = V_{DD}	1,2,3	ALL	-10	10	µA
Output LOW voltage	V_{OL}	V_{DD} = 4.5 V, IOL = 8 mA	1,2,3	ALL		0.4	V
Output HIGH voltage	V_{OH}	V_{DD} = 4.5 V, IOH = -4 mA	1,2,3	ALL	2.4		V
Output leakage current, output LOW	I_{OZL}	V_{DD} = 5.5 V, V_{in} = 0V	1,2,3	ALL	-40	40	µA
Output leakage current, output HIGH	I_{OZH}	V_{DD} = 5.5 V, V_{in} = V_{DD}	1,2,3	ALL	-40	40	µA
Short circuit 2/ output current	I_{OS}	V_{DD} = 5.5 V, output HIGH one pin to GND, one second duration max	1,2,3	ALL	-20	100	mA
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz see 4.4.1c	4	ALL		15	pF
Output capacitance	C_{OUT}	T_A = 25°C, f = 1 MHz see 4.4.1c	4	ALL		15	pF

See footnotes at the end of the table.

TABLE I. Electrical performance characteristics. (continued)

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional testing 3/		V_{DD} = 5 V, see 4.4.1b	7,8A,8B	ALL			
Digital output delay 3/ 4/	t_D	V_{DD} = 4.5 V	9,10,11	01		25	ns
		see Figure 4	10	02		23	ns
Digital output hold time 3/	t_{HO}	V_{DD} = 5.5 V see Figure 4	9,10,11	ALL		4	ns
Output enable delay 4/	t_{ENA}	V_{DD} = 4.5 V	9,10,11	01		17	ns
		see Figure 4	10	02		16	ns
Output disable delay 4/	t_{DIS}	V_{DD} = 4.5 V	9,10,11	01		17	ns
		see Figure 4	10	02		16	ns

1/ All testing to be performed using worst-case test conditions unless otherwise specified.

2/ Not more than one output should be shorted.

3/ All transitions are measured at 1.5 V level.

4/ Device 02 is differentiated from device 01 at +125°C only, (following 25°C and -55°C testing).

DEVICE TYPES 01 AND 02

CASE OUTLINE X

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	PYOUT_{5}	B3	PYOUT_{6}	C5	GND	E1	RTP	G11	GND	K1	YPIN_{2}	L10	YPIN_{31}	M12	XRIN_{1}
A2	PYOUT_{7}	B4	PYPUT_{9}	C6	V_{DD}	E2	GND	G12	XRIN_{12}	K2	YPIN_{4}	L11	VDD	M13	XRIN_{2}
A3	PYOUT_{8}	B5	PYOUT_{11}	C7	GND	E3	VDD	G13	XRIN_{13}	K3	GND	L12	XRIN_{3}	N1	YPIN_{8}
A4	PYOUT_{10}	B6	PYOUT_{13}	C8	V_{DD}	E11	VDD	H1	ACC_{0}	K11	GND	L13	XRIN_{4}	N2	YPIN_{10}
A5	PYOUT_{12}	B7	OVF	C9	GND	E12	GND	H2	ACC_{1}	K12	XRIN_{5}	M1	YPIN_{6}	N3	YPIN_{12}
A6	PYOUT_{14}	B8	RXOUT_{1}	C10	GND	E13	$\overline{\text{OERX}}$	H3	V_{DD}	K13	XRIN_{6}	M2	YPIN_{9}	N4	YPIN_{15}
A7	PYOUT_{15}	B9	RXOUT_{3}	C11	V_{DD}	F1	TCXY	H11	XRIN_{9}	L1	YPIN_{5}	M3	YPIN_{11}	N5	YPIN_{17}
A8	RXOUT_{0}	B10	RXOUT_{5}	C12	RXOUT_{11}	F2	GND	H12	XRIN_{10}	L2	YPIN_{7}	M4	YPIN_{13}	N6	YPIN_{19}
A9	RXOUT_{2}	B11	RXOUT_{7}	C13	RXOUT_{13}	F3	CLK	H13	XRIN_{11}	L3	GND	M5	YPIN_{16}	N7	YPIN_{21}
A10	RXOUT_{4}	B12	RXOUT_{9}	D1	$\overline{\text{OEPY}}$	F11	VDD	J1	YPIN_{0}	L4	V_{DD}	M6	YPIN_{18}	N8	YPIN_{22}
A11	RXOUT_{6}	B13	RXOUT_{12}	D2	PYOUT_{0}	F12	XRIN_{15}	J2	YPIN_{1}	L5	YPIN_{14}	M7	YPIN_{20}	N9	YPIN_{24}
A12	RXOUT_{8}	C1	PYOUT_{1}	D3	GND	F13	XRIN_{14}	J3	YPIN_{3}	L6	V_{DD}	M8	YPIN_{23}	N10	YPIN_{26}
A13	RXOUT_{10}	C2	PYOUT_{2}	D11	GND	G1	ENYP_{1}	J11	GND	L7	GND	M9	YPIN_{25}	N11	YPIN_{29}
B1	PYOUT_{3}	C3	V_{DD}	D12	RXOUT_{14}	G2	ENYP_{0}	J12	XRIN_{7}	L8	V_{DD}	M10	YPIN_{28}	N12	YPIN_{30}
B2	PYOUT_{4}	C4	GND	D13	RXOUT_{15}	G3	GND	J13	XRIN_{8}	L9	YPIN_{27}	M11	ENXR	N13	XRIN_{0}

CASE OUTLINE Y

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	V_{DD}	23	YPIN_{1}	45	VDD	67	V_{DD}	89	GND	111	RXOUT_{2}
2	NC	24	YPIN_{2}	46	YPIN_{18}	68	XRIN_{1}	90	RXOUT_{15}	112	VDD
3	PYOUT_{4}	25	YPIN_{3}	47	YPIN_{19}	69	XRIN_{2}	91	V_{DD}	113	RXOUT_{1}
4	PYOUT_{3}	26	YPIN_{4}	48	YPIN_{20}	70	GND	92	RXOUT_{14}	114	RXOUT_{0}
5	GND	27	YPIN_{5}	49	GND	71	XRIN_{3}	93	RXOUT_{13}	115	OVF
6	PYOUT_{2}	28	YPIN_{6}	50	YPIN_{21}	72	NC	94	RXOUT_{12}	116	GND
7	PYOUT_{1}	29	GND	51	YPIN_{22}	73	XRIN_{4}	95	GND	117	PYOUT_{15}
8	PYOUT_{0}	30	YPIN_{7}	52	YPIN_{23}	74	XRIN_{5}	96	RXOUT_{11}	118	PYOUT_{14}
9	VDD	31	YPIN_{8}	53	VDD	75	GND	97	RXOUT_{10}	119	PYOUT_{13}
10	$\overline{\text{OEPY}}$	32	NC	54	YPIN_{24}	76	XRIN_{6}	98	NC	120	V_{DD}
11	GND	33	GND	55	YPIN_{25}	77	XRIN_{7}	99	V_{DD}	121	PYOUT_{12}
12	RTP	34	YPIN_{9}	56	YPIN_{26}	78	XRIN_{8}	100	RXOUT_{9}	122	PYOUT_{11}
13	CLK	35	NC	57	YPIN_{27}	79	XRIN_{9}	101	NC	123	PYOUT_{10}
14	GND	36	YPIN_{10}	58	YPIN_{28}	80	XRIN_{10}	102	RXOUT_{8}	124	GND
15	TCXY	37	VDD	59	YPIN_{29}	81	XRIN_{11}	103	NC	125	PYOUT_{9}
16	ENYP_{0}	38	YPIN_{11}	60	YPIN_{30}	82	XRIN_{12}	104	GND	126	PYOUT_{8}
17	GND	39	YPIN_{12}	61	YPIN_{31}	83	GND	105	RXOUT_{7}	127	PYOUT_{7}
18	ENYP_{1}	40	YPIN_{13}	62	NC	84	XRIN_{13}	106	RXOUT_{6}	128	NC
19	ACC_{0}	41	YPIN_{14}	63	ENXR	85	XRIN_{14}	107	RXOUT_{5}	129	GND
20	ACC_{1}	42	YPIN_{15}	64	NC	86	XRIN_{15}	108	GND	130	PYOUT_{6}
21	V_{DD}	43	YPIN_{16}	65	NC	87	V_{DD}	109	RXOUT_{4}	131	NC
22	YPIN_{0}	44	YPIN_{17}	66	XRIN_{0}	88	$\overline{\text{OERX}}$	110	RXOUT_{3}	132	PYOUT_{5}

FIGURE 1. Terminal connections.

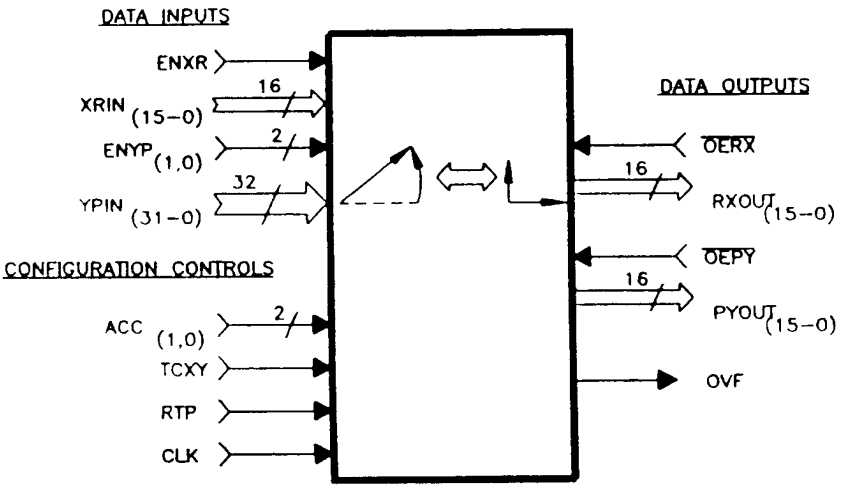


FIGURE 2. Logic diagram.

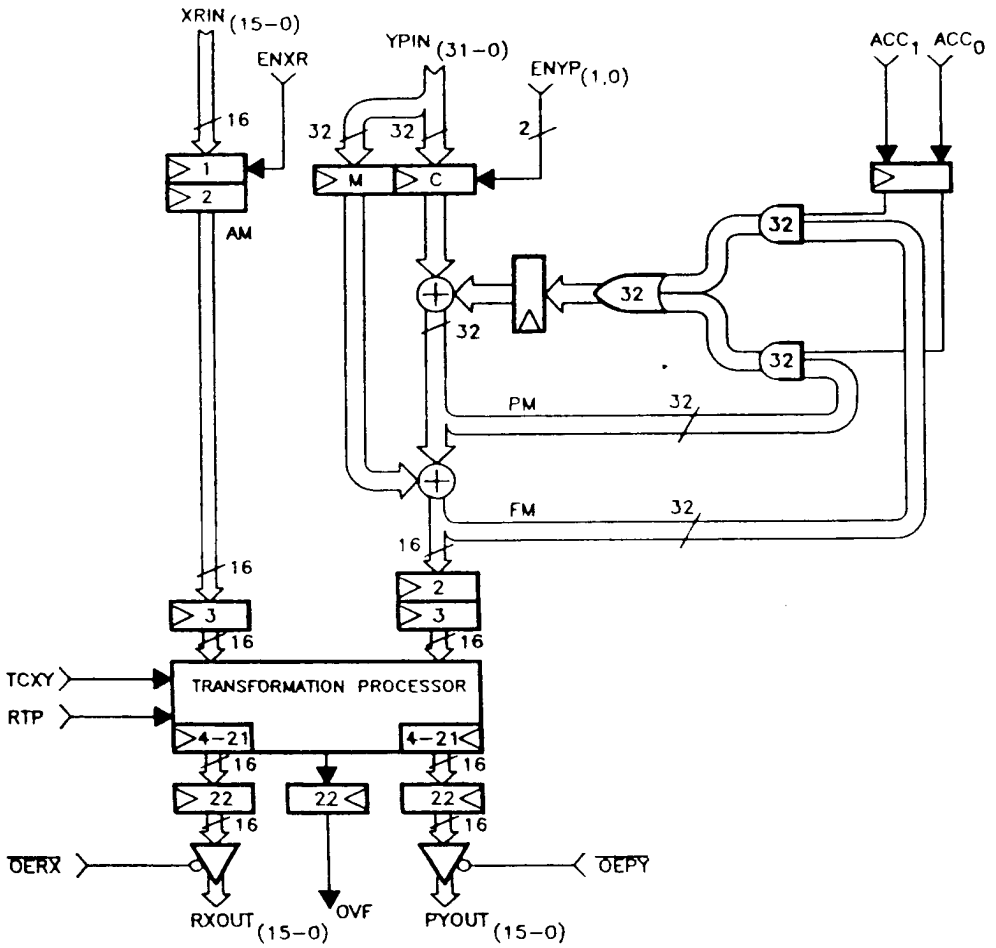


FIGURE 3. Block diagram.

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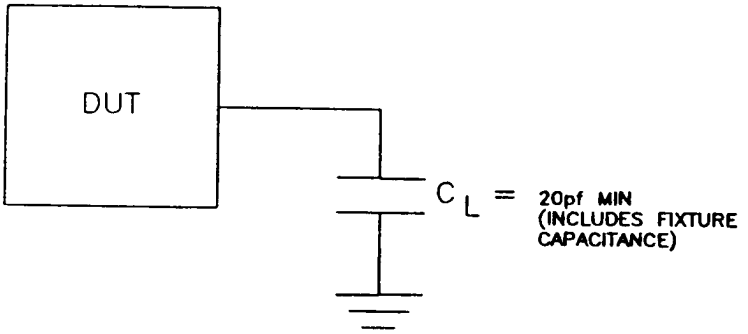

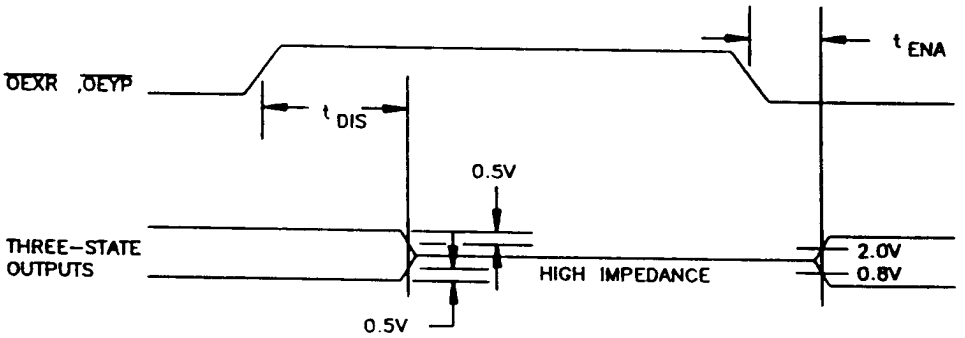

FIGURE 4. Switching waveforms and load circuit.

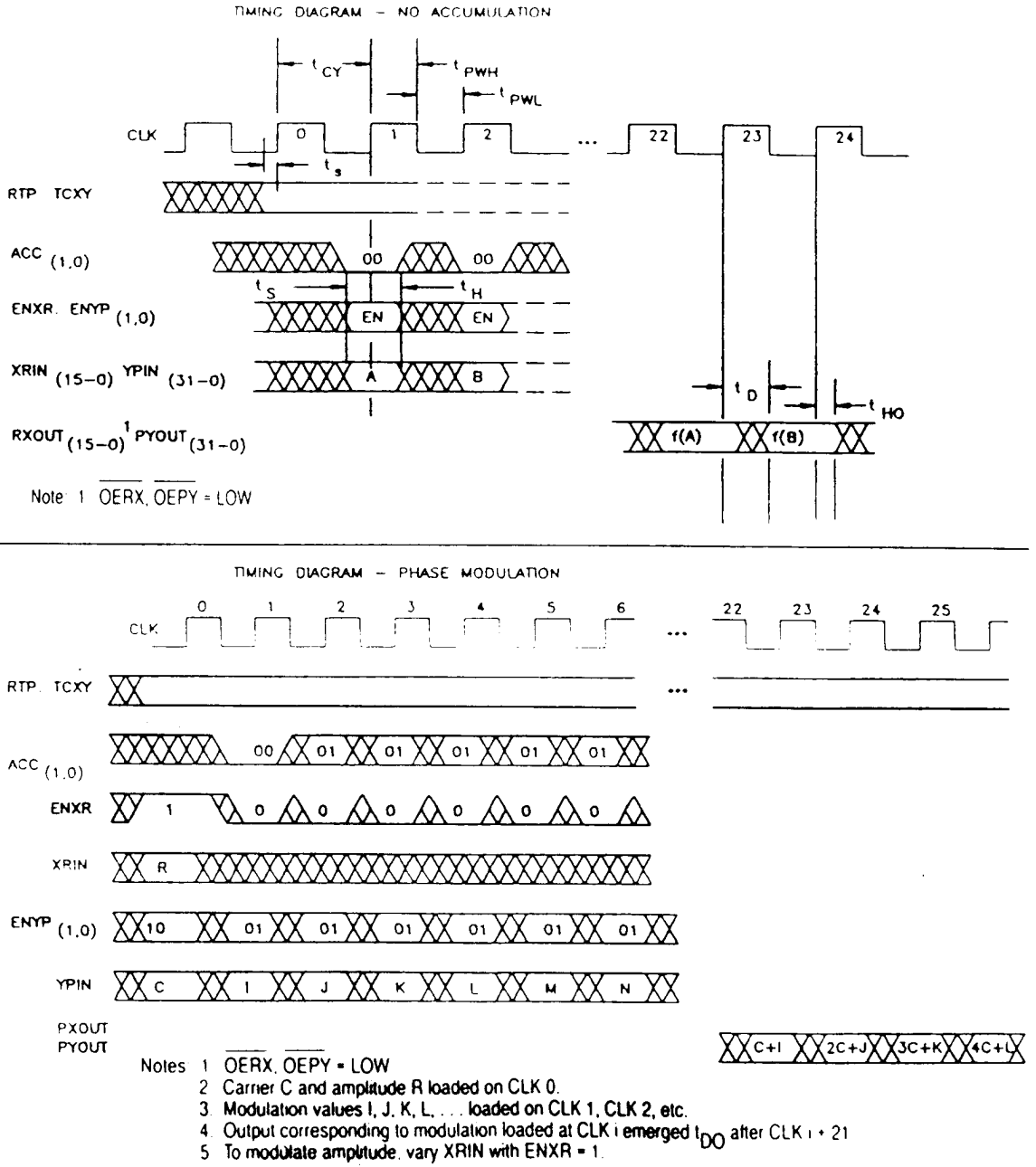

FIGURE 4. Switching waveforms and load circuit. - Continued

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4(C_{IN} and C_{OUT} measurements) shall be measured only for the initial design and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 1/ 9, 10, 11	1, 2, 3, 7, 1/ 8, 9, 10, 11	1, 2, 3, 7, 2/ 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 7, 9	1, 2, 7, 9	1, 2, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 2, 7, 9	1, 2, 7, 9	1, 2, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535, MIL-STD-1331 and Table III.

TABLE III. PIN FUNCTIONS.

V_{DD}, GND	The device operates from a single +5V supply. All power and ground pins must be connected.
CLOCK	
CLK	The device operates from a single clock. All enabled registers are strobed on the rising edge of CLK, which is the reference for all timing specifications.
INPUTS/OUTPUTS	
$XRIN_{15-0}$	$XRIN_{15-0}$ is the registered Cartesian X-coordinate or Polar Magnitude (Radius) 16-bit input data port. $XRIN_{15-0}$ is the MSB.
$YPIN_{31-0}$	$YPIN_{31-0}$ is the registered Cartesian Y-coordinate or Polar Phase angle 32-bit input data port. $YPIN_{31}$ is the MSB.
$RXOUT_{15-0}$	$RXOUT_{15-0}$ is the registered Polar Magnitude (Radius) or X-coordinate 16-bit output data port. $RXOUT_{15}$ is the MSB.
$PYOUT_{15-0}$	$PYOUT_{15-0}$ is the registered Polar Phase angle or Cartesian Y-coordinate 16-bit output data port. $PYOUT_{15}$ is the MSB.
CONTROLS	
ENXR	The value presented to the input port XRIN is latched into the input registers on the current clock when ENXR is HIGH. When ENXR is LOW, the value stored in the register remains unchanged.
$ENYP_{1,0}$	The value presented to the YPIN input port is latched into the phase accumulator input registers on the current clock, as determined by the control inputs $ENYP_{1,0}$ as shown below:

$ENYP_{1,0}$	INSTRUCTION
00	No registers enabled, current data held
01	M register input enabled, C data held
10	C register input enabled, M data held
11	M register set to 0, C register input enabled

where C is the Carrier register and M is the Modulation register, and 0=LOW, 1=HIGH.

RTP	This registered input selects the current transformation mode of the device. When RTP is HIGH, the device executes a Rectangular-To-Polar conversion. When RTP is LOW, a Polar-To-Rectangular conversion will be performed. The input and output ports are then configured to handle data in the appropriate coordinate system. This is a static input.

TABLE III. PIN FUNCTIONS (cont.)

$ACC_{1,0}$	In applications utilizing the device to perform waveform synthesis and modulation in the Polar-To-Rectangular mode (RTP=LOW), the user determines the internal phase Accumulator structure implemented on the next clock by setting the accumulator control word $ACC_{1,0}$, as shown below: $ACC_{1,0}$ | CONFIGURATION 00 | No accumulation performed 01 | PM accumulator path enabled 10 | FM accumulator path enabled 11 | (Nonsensical) logical OR of PM and FM where 0=LOW, 1=HIGH. The accumulator will roll over correctly when full scale is exceeded, allowing the user to perform continuous phase accumulation through 2π radians, or 360 degrees. Note that the accumulators will also function when RTP = HIGH (Retangular-To-Polar), which is useful when performing backward mapping from Cartesian to polar coordinates; however, most applications will require that $ACC_{1,0}$ be set to 00 to avoid accumulating the Cartesian Y input data.
TCXY	The format select control sets the numeric format of the Rectangular data, whether input (RTP=HIGH) or output (RTP=LOW). This control indicates two's complement format when TCXY=HIGH, and sign-and-magnitude when LOW. This is a static input.
OVF	When RTP=LOW (Polar-To-Rectangular), the Overflow Flag will go HIGH on the clock that the magnitude of either of the current Cartesian coordinate outputs exceeds the maximum range. It will return LOW on the clock that the Cartesian out-put values(s) return to full-scale or less.
$\overline{OERX}$, $\overline{OEPY}$	Data in the output registers are available at the outputs of the device when the respective asynchronous Output Enables are LOW. When OERX or OEPY is HIGH, the respective output port(s) is in the high-impedance state.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirement documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.