Revision History

No.	History	Draft Date	Remark
0.1	Defined Target Spec.	May 2004	Preliminary

DESCRIPTION

Preliminary

Hynix HYMD564G726B(L)F8N-D43/J series is registered 184-pin double data rate Synchronous DRAM Dual In-Line Memory Modules (DIMMs) which are organized as 64M x 72 high-speed memory arrays.

Hynix HYMD564G726B(L)F8N-D43/J series consists of nine 64M x 8 DDR SDRAM in FBGA packages on a 184pin glass-epoxy substrate. Hynix HYMD564G726B(L)F8N-D43/J series provide a high performance 8-byte interface in 5.25" width form factor of industry standard. It is suitable for easy interchange and addition.

Hynix HYMD564G726B(L)F8N-D43/J series is designed for high speed of up to 166/200MHz and offers fully synchronous operations referenced to both rising and falling edges of differential clock inputs. While all addresses and control inputs are latched on the rising edges of the clock, Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2. High speed frequencies, programmable latencies and burst lengths allow variety of device operation in high performance memory system.

Hynix HYMD564G726B(L)F8N-D43/J series incorporates SPD(serial presence detect). Serial presence detect function is implemented via a serial 2,048-bit EEPROM. The first 128 bytes of serial PD data are programmed by Hynix to identify DIMM type, capacity and other the information of DIMM and the last 128 bytes are available to the customer.

FEATURES

- 512MB (64M x 72) Registered DDR DIMM based on 64M x 8 DDR SDRAM
- JEDEC Standard 184-pin dual in-line memory module (DIMM)
- Error Check Correction (ECC) Capability
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- 2.6V +/- 0.1V VDD and VDDQ Power supply for DDR400, 2.5V +/- 0.2V VDD and VDDQ for DDR333 supported
- All inputs and outputs are compatible with SSTL_2 interface
- Fully differential clock operations (CK & /CK) with 166/200MHz
- Programmable CAS Latency 3 for DDR400, 2.5 for DDR333 supported
- Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
- tRAS Lock-out function supported
- Internal four bank operations with single pulsed RAS
- Auto refresh and self refresh supported
- 8192 refresh cycles / 64ms

ORDERING INFORMATION

Part No.	Power Supply	Clock Frequency	Interface	Form Factor
HYMD564G726B(L)F8N-D43	VDD=2.6V VDDQ=2.6V	200MHz (*DDR400)	SSTL_2	184pin Registered DIMM 5.25 x 1.125 x 0.15 inch
HYMD564G726B(L)F8N-J	VDD=2.5V VDDQ=2.5V	166MHz (*DDR333)		

** JEDEC Defined Specifications compliant*

PIN DESCRIPTION

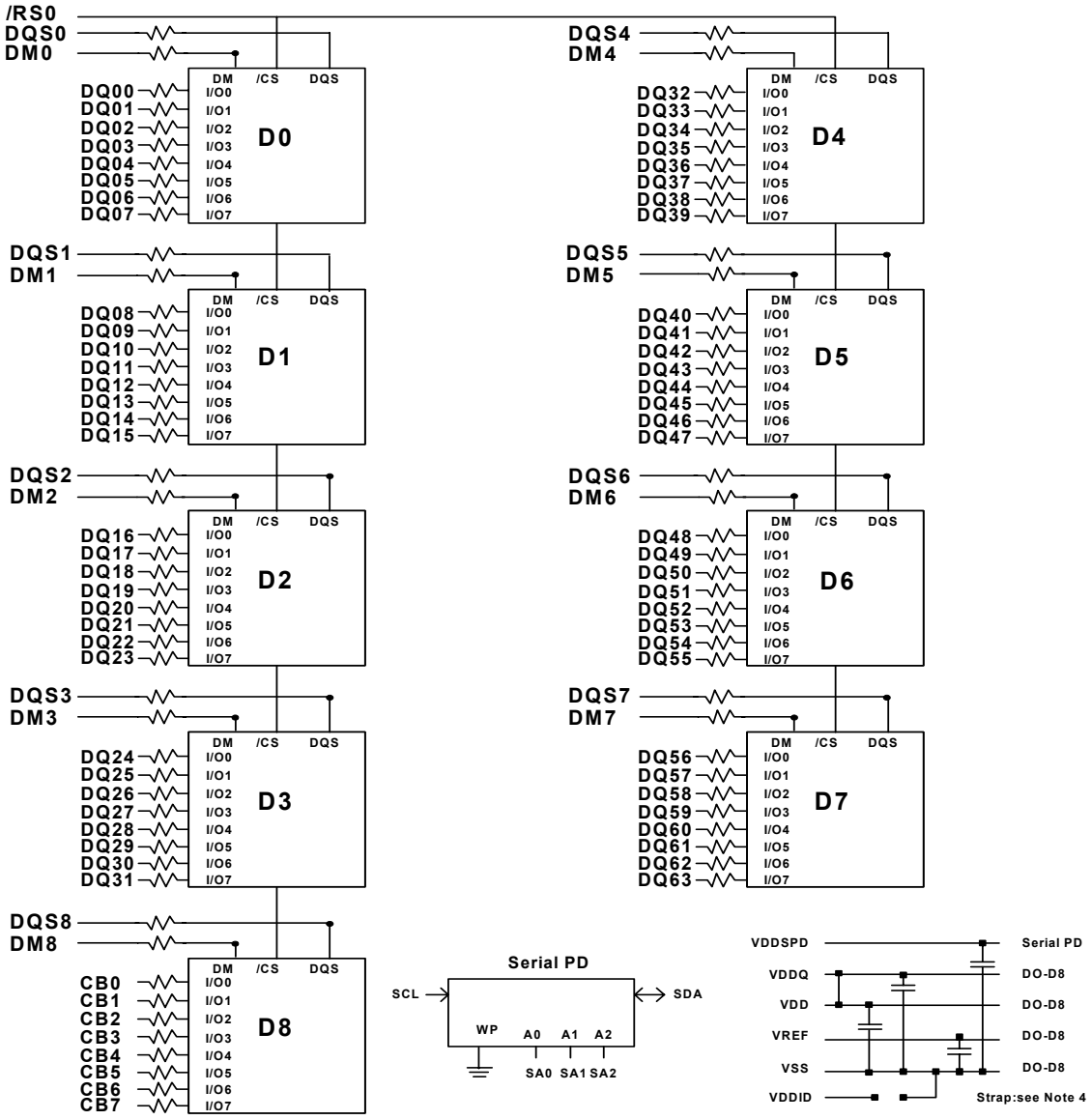
Pin	Pin Description	Pin	Pin Description
CK0, /CK0	Differential Clock Inputs	VDDQ	DQs Power Supply
CS0	Chip Select Input	VSS	Ground
CKE0	Clock Enable Input	VREF	Reference Power Supply
/RAS, /CAS, /WE	Commend Sets Inputs	VDDSPD	Power Supply for SPD
A0 ~ A12	Address	SA0~SA2	E^2PROM Address Inputs
BA0, BA1	Bank Address	SCL	E^2PROM Clock
DQ0~DQ63	Data Inputs/Outputs	SDA	E^2PROM Data I/O
CB0~CB7	Data Strobe Inputs/Outputs	WP	Write Protect Flag
DQS0~DQS17	Data Strobe Inputs/Outputs	VDDID	VDD Identification Flag
DM0~7	Data-in Mask	DU	Do not Use
VDD	Power Supply	NC	No Connection
/RESET	Reset Enable	FETEN	FET Enable

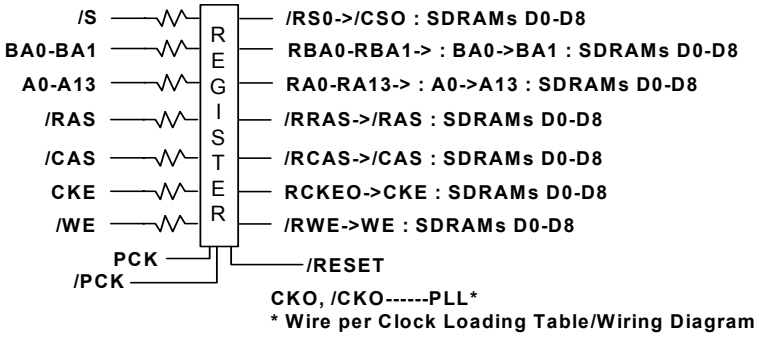
PIN ASSIGNMENT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	/CS1*
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	/RESET	41	A2	71	NC	102	NC	133	DQ31	163	NC
11	VSS	42	Vss	72	DQ48	103	NC	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	DU	106	DQ13	137	CK0	167	A13, FETEN*
15	VDDQ	46	VDD	76	DU	107	DM1	138	/CK0	168	VDD
16	NC	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	NC	48	A0	78	DQS6	109	DQ14	140	DM8	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1*	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	BA2*	144	CB7	174	DQ60
22	VDDQ	Key		83	DQ56	114	CB7	key		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NU	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

* These are not used on this module but may be used for other module in 184pin DIMM family

FUNCTIONAL BLOCK DIAGRAM





Note :

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}) : STRAP OUT (OPEN) : $V_{DD} = V_{DDQ}$ STRAP IN (V_{SS}) : $V_{DD} \neq V_{DDQ}$
5. SDRAM placement alternates between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Operating Temperature (Ambient)	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on VDD relative to VSS	VDD	-0.5 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDDQ	-0.5 ~ 3.6	V
Output Short Circuit Current	IOS	50	mA
Power Dissipation	PD	1.0 x # of Components	W
Soldering Temperature Þ Time	TSOLDER	260 / 10	°C / Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS= 0V)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD	2.3	2.5	2.7	V	
Power Supply Voltage	VDD	2.5	2.6	2.7	V	4
Power Supply Voltage	VDDQ	2.3	2.5	2.7	V	1
Power Supply Voltage	VDD	2.5	2.6	2.7	V	1,4
Input High Voltage	VIH	VREF + 0.15	-	VDDQ + 0.3	V	
Input Low Voltage	VIL	-0.3	-	VREF - 0.15	V	2
Termination Voltage	VTT	VREF - 0.04	VREF	VREF + 0.04	V	
Reference Voltage	VREF	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V	3

Note :

1. VDDQ must not exceed the level of VDD.
2. VIL (min) is acceptable -1.5V AC pulse width with $\leq$ 5ns of duration.
3. The value of VREF is approximately equal to 0.5VDDQ.
4. For DDR400, VDD=2.6V +/- 0.1V, VDDQ=2.6V+/-0.1V

AC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)		VREF - 0.31	V	
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ + 0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note :

1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Value	Unit
Reference Voltage	VDDQ x 0.5	V
Termination Voltage	VDDQ x 0.5	V
AC Input High Level Voltage (VIH, min)	VREF + 0.31	V
AC Input Low Level Voltage (VIL, max)	VREF - 0.31	V
Input Timing Measurement Reference Level Voltage	VREF	V
Output Timing Measurement Reference Level Voltage	VTT	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (RT)	50	Ω
Series Resistor (RS)	25	Ω
Output Load Capacitance for Access Time Measurement (CL)	30	pF

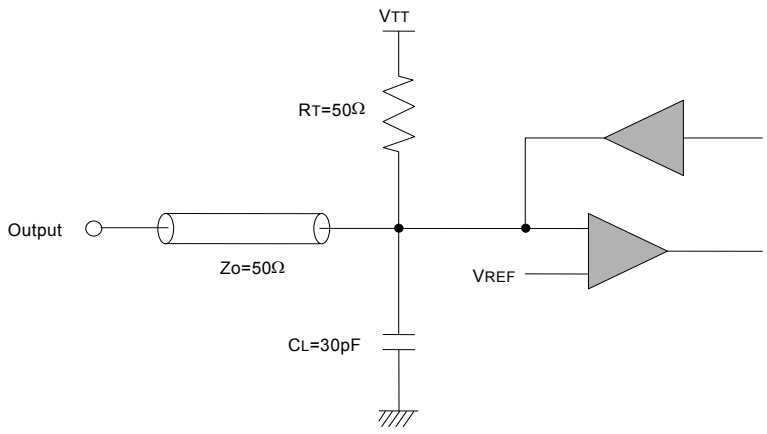
CAPACITANCE (T_A=25°C, f=100MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input Capacitance	A0 ~ A12, BA0, BA1	CIN1	7	12	pF
Input Capacitance	/RAS, /CAS, /WE	CIN2	7	12	pF
Input Capacitance	CKE0	CIN3	7	12	pF
Input Capacitance	CS0	CIN4	7	12	pF
Input Capacitance	CK0, /CK0	CIN5	7	14	pF
Data Input / Output Capacitance	DQ0 ~ DQ63, DQS0 ~ DQS17	CIO1	6	11	pF
Data Input / Output Capacitance	CB0 ~ CB7	CIO2	6	11	pF

Note :

1. VDD = min. to max., VDDQ = 2.5V to 2.7V, VODC = VDDQ/2, VOpeak-to-peak = 0.2V
2. Pins not under test are tied to GND.
3. These values are guaranteed by design and are tested on a sample basis only.

OUTPUT LOAD CIRCUIT



DC CHARACTERISTICS I (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter		Symbol	Min.	Max	Unit	Note
Input Leakage Current	Add, CMD, /CS, /CKE	ILI	-2	2	uA	1
	CK, /CK		-4	4		
Output Leakage Current		ILO	-10	10	uA	2
Output High Voltage		VOH	VTT + 0.76	-	V	IOH = -15.2mA
Output Low Voltage		VOL	-	VTT - 0.76	V	IOL = +15.2mA

Note :

1. VIN = 0 to 3.6V, All other pins are not tested under VIN =0V
2. DOUT is disabled, VOUT=0 to 2.7V

DC CHARACTERISTICS II (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Test Condition		Speed		Unit	Note
				-D43	-J		
Operating Current	IDD0	One bank; Active - Precharge ; tRC=tRC(min); tCK= tCK(min) ; DQ,DM and DQS inputs changing twice per clock cycle ; address and control inputs changing once per clock cycle		2000	1910	mA	
Operating Current	IDD1	One bank ; Active - Read - Precharge ; Burst Length = 4 ; tRC=tRC(min); tCK= tCK(min) ; address and control inputs changing once per clock cycle		2450	2270	mA	
Precharge Power Down Standby Current	IDD2P	All banks idle ; Power down mode ; CKE= Low, tCK= tCK(min)		740		mA	
Idle Standby Current	IDD2F	/CS = High, All banks idle ; tCK= tCK(min) ; CKE = High ; address and control inputs changing once per clock cycle. VIN = VREF for DQ, DQS and DM		965		mA	
Active Power Down Standby Current	IDD3P	One bank active ; Power down mode ; CKE= Low, tCK= tCK(min)		758		mA	
Active Standby Current	IDD3N	/CS= HIGH; CKE = HIGH; One bank; Active-Precharge; tRC = tRAS(max); tCK = t CK (max); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		1100	1055	mA	
Operating Current	IDD4R	Burst = 2 ; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK= tCK (min); IOUT = 0mA		3170	2900	mA	
Operating Current	IDD4W	Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK (min); DQ, DM, and DQS inputs changing twice per clock cycle		3170	2900		
Auto Refresh Current	IDD5	tRC = tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh		3050	2870		
Self Refresh Current	IDD6	CKE =< 0.2V; External clock on; tCK = tCK(min)	Normal	395		mA	
			Low Power	373		mA	
Operating Current - Four Bank Operation	IDD7	Four bank interleaving with BL=4 Refer to the following page for detailed test condition		5510	4790	mA	

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-D43		-J		Unit	Note
			Min	Max	Min	Max		
Row Cycle Time		tRC	55	-	60	-	ns	
Auto Refresh Row Cycle Time		tRFC	70	-	72	-	ns	
Row Active Time		tRAS	40	70K	42	70K	ns	
Active to Read with Auto Precharge Delay		tRAP	tRCD or tRP(min)	-	tRCD or tRP(min)	-	ns	16
Row Address to Column Address Delay		tRCD	15	-	18	-	ns	
Row Active to Row Active Delay		tRRD	10	-	12	-	ns	
Column Address to Column Address Delay		tCCD	1	-	1	-	CK	
Row Precharge Time		tRP	15	-	18	-	ns	
Write Recovery Time		tWR	15	-	15	-	ns	
Write to Read Command Delay		tWTR	2	-	1	-	CK	
Auto Precharge Write Recovery + Precharge Time		tDAL	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)		CK	15
System Clock Cycle Time	CL = 3	tCK	5	10	-	-	ns	
	CL = 2.5		6	12	6	12		
Clock High Level Width		tCH	0.45	0.55	0.45	0.55	CK	
Clock Low Level Width		tCL	0.45	0.55	0.45	0.55	CK	
Data-Out edge to Clock edge Skew		tAC	-0.7	0.7	-0.7	0.7	ns	
DQS-Out edge to Clock edge Skew		tDQSCK	-0.55	0.55	-0.6	0.6	ns	
DQS-Out edge to Data-Out edge Skew		tDQSQ	-	0.4		0.4	ns	
Data-Out hold time from DQS		tQH	tHP -tQHS	-	tHP -tQHS	-	ns	1, 10
Clock Half Period		tHP	min (tCL,tCH)	-	min (tCL,tCH)	-	ns	1,9
Data Hold Skew Factor		tQHS	-	0.5	-	0.55	ns	10
Data-out high-impedance window from CK, /CK		tHZ		tAC(Max)	-0.7	0.7	ns	17
Data-out low-impedance window from CK, /CK		tLZ	-0.7	0.7	-0.7	0.7	ns	17
Input Setup Time (fast slew rate)		tIS	0.6	-	0.75	-	ns	2,3,5,6
Input Hold Time (fast slew rate)		tIH	0.6	-	0.75	-	ns	2,3,5,6
Input Setup Time (slow slew rate)		tIS	0.7	-	0.8	-	ns	2,4,5,6
Input Hold Time (slow slew rate)		tIH	0.7	-	0.8	-	ns	2,4,5,6
Input Pulse Width		tIPW	2.2	-	2.2	-	ns	6
Write DQS High Level Width		tDQSH	0.35	-	0.35	-	CK	

AC CHARACTERISTICS (AC operating conditions unless otherwise noted) *- continued -*

Parameter	Symbol	-D43		-J		Unit	Note
		Min	Max	Min	Max		
Write DQS Low Level Width	tDQSL	0.35	-	0.35	-	CK	
Clock to First Rising edge of DQS-In	tDQSS	0.72	1.28	0.75	1.25	CK	
Data-In Setup Time to DQS-In (DQ & DM)	tDS	0.4	-	0.45	-	ns	6,7,11~13
Data-in Hold Time to DQS-In (DQ & DM)	tDH	0.4	-	0.45	-	ns	
DQ & DM Input Pulse Width	tDIPW	1.75	-	1.75	-	ns	6
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	CK	
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	CK	
Write DQS Preamble Setup Time	tWPRES	0	-	0	-	CK	
Write DQS Preamble Hold Time	tWPREH	0.25	-	0.25	-	CK	
Write DQS Postamble Time	tWPST	0.4	0.6	0.4	0.6	CK	
Mode Register Set Delay	tMRD	2	-	2	-	CK	
Exit self refresh to Any Executable Command	tXSC	200	-	200	-	CK	8
Average Periodic Refresh Interval	tREFI	-	7.8	-	7.8	us	

Note :

1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock : A0~A12, BA0~BA1, CKE, /CS, /RAS, /CAS, /WE.
3. For command/address input slew rate >=1.0V/ns
4. For command/address input slew rate >=0.5V/ns and <1.0V/ns
   This derating table is used to increase tIS/tIH in case where the input slew-rate is below 0.5V/ns.
   Input Setup / Hold Slew-rate Derating Table.

Input Setup / Hold Slew-rate	Delta tIS	Delta tIH
V/ns	ps	ps
0.5	0	0
0.4	+50	0
0.3	+100	0

5. CK, /CK slew rates are >=1.0V/ns, ie, >=2.0V/ns differential.
6. These parameters quarantee device timing, but they are not necessarily tested on each device, and they may be quaranteed by design or tester correlation.
7. Data latched at both rising and falling edges of Data Strobes(LDQS/UDQS) : DQ, LDM/UDM.
8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.
9. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).

10. tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS consists of tDQSQmax, the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects and p-channel to n-channel variation of the output drivers.

11. This derating table is used to increase tDS/tDH in case where the input slew-rate is below 0.5V/ns.

Input Setup / Hold Slew-rate Derating Table.

Input Setup / Hold Slew-rate	Delta tDS	Delta tDH
V/ns	ps	ps
0.5	0	0
0.4	+75	+75
0.3	+150	+150

12. I/O Setup/Hold Plateau Derating. This derating table is used to increase tDS/tDH in case where the input level is flat below VREF +/-310mV for a duration of up to 2ns.

I/O Input Level	Delta tDS	Delta tDH
mV	ps	ps
+280	+50	+50

13. I/O Setup/Hold Delta Inverse Slew Rate Derating. This derating table is used to increase tDS/tDH in case where the DQ and DQS slew rates differ. The Delta Inverse Slew Rate is calculated as (1/SlewRate1)-(1/SlewRate2). For example, if slew rate 1=0.5V/ns and Slew Rate2 = 0.4V/n then the Delta Inverse Slew Rate = -0.5ns/V.

(1/SlewRate1)-(1/SlewRate2)	Delta tDS	Delta tDH
ns/V	ps	ps
0	0	0
+/-0.25	+50	+50
+/- 0.5	+100	+100

14. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transi tions through the DC region must be monotonic.

15. tDAL = (tWR / tCK) + (tRP / tCK). For each of the terms above, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time.
Example: For DDR266B at CL=2.5 and tCK = 7.5 ns,
tDAL = (15 ns / 7.5 ns) + (20 ns / 7.5 ns) = (2.00) + (2.67)
Round up each non-integer to the next highest integer: = (2) + (3), tDAL = 5 clock

16. For the parts which do not has internal RAS lockout circuit, Active to Read with Auto precharge delay should be tRAS - BL/2 x tCK.

17. tHZ and tLZ transitions occur in the same access time windows as valid data trasitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).

SIMPLIFIED COMMAND TRUTH TABLE

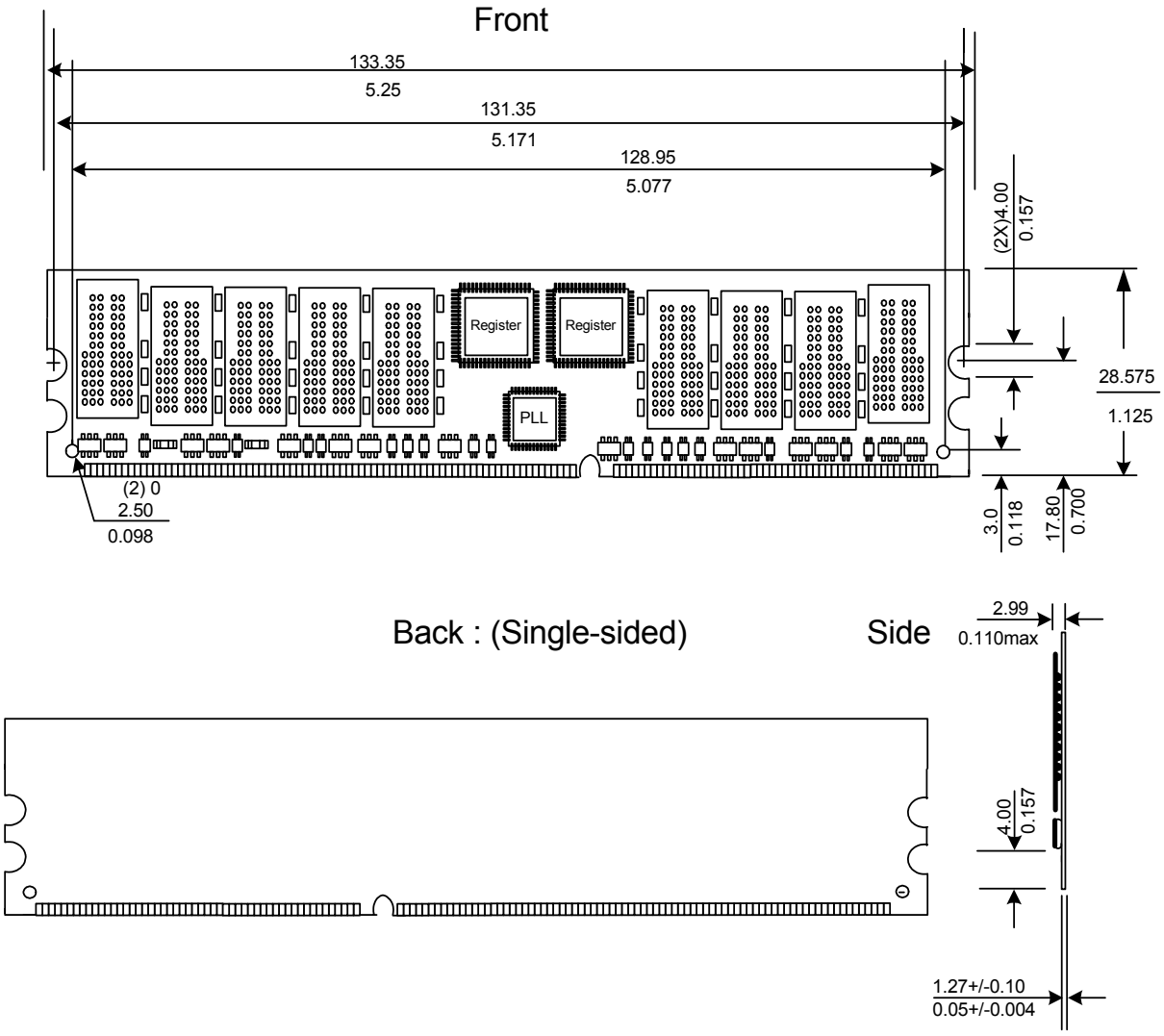
Command		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	ADDR	A10/AP	BA	Note
Extended Mode Register Set		H	X	L	L	L	L	OP code			1,2
Mode Register Set		H	X	L	L	L	L	OP code			1,2
Device Deselect		H	X	H	X	X	X	X			1
No Operation				L	H	H	H				
Bank Active		H	X	L	L	H	H	RA		V	1
Read		H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge									H		1,3
Write		H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge									H		1,4
Precharge All Banks		H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank									L	V	1
Read Burst Stop		H	X	L	H	H	L	X			1
Auto Refresh		H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X			1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	H	H	H				1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				1
Active Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	V	V	V				1
	Exit	L	H	X							1

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

Note :

1. LDM/ UDM states are Don't Care. Refer to below Write Mask Truth Table.
2. OP Code(Operand Code) consists of A_0~A_{12} and BA_0~BA_1 used for Mode Registering duing Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
3. If a Read with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+t_{RP}).
4. If a Write with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+1+t_{DPL}+t_{RP}). Last Data-In to Prechage delay(t_{DPL}) which is also called Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
5. If A_{10}/AP is High when Row Precharge command being issued, BA_0/BA_1 are ignored and all banks are selected to be precharged.

PACKAGE DIMENSIONS



Note) All dimension are typical unless otherwise stated. Millimeters / Inches

SPD SPECIFICATION

(64M x 72 Registered DDR DIMM)

SERIAL PRESENCE DETECT

Byte#	Function Description	Function Supported		Hexa Value		Note
		-D43	-J	-D43	-J	
0	Number of Bytes written into serial memory at module manufacturer	128 Bytes		80h		
1	Total number of Bytes in SPD device	256 Bytes		08h		
2	Fundamental memory type	DDR SDRAM		07h		
3	Number of row address on this assembly	13		0Dh		1
4	Number of column address on this assembly	11		0Bh		1
5	Number of physical banks on DIMM	1Bank		01h		
6	Module data width	72 Bits		48h		
7	Module data width (continued)	-		00h		
8	Module voltage Interface levels(VDDQ)	SSTL 2.5V		04h		
9	DDR SDRAM cycle time at CAS Latency=2.5(tCK)	5.0ns	6.0ns	50h	60h	2
10	DDR SDRAM access time from clock at CL=2.5 (tAC)	+/-0.7ns		70h		2
11	Module configuration type	ECC		02h		
12	Refresh rate and type	7.8us & Self refresh		82h		
13	Primary DDR SDRAM width	x8		08h		
14	Error checking DDR SDRAM data width	x8		08h		
15	Minimum clock delay for back-to-back random column address(tCCD)	1 CLK		01h		
16	Burst lengths supported	2,4,8		0Eh		
17	Number of banks on each DDR SDRAM	4 Banks		04h		
18	CAS latency supported	2, 2.5, 3	2, 2.5	1Ch	0Ch	
19	CS latency	0		01h		
20	WE latency	1		02h		
21	DDR SDRAM module attributes	Registered, PLL		26h		
22	DDR SDRAM device attributes : General	+/-0.2Voltage tolerance, Concurrent Auto Precharge tRAS Lock Out		C0h		
23	DDR SDRAM cycle time at CL=2.0(tCK)	6.0ns	7.5ns	60h	75h	2
24	DDR SDRAM access time from clock at CL=2.0(tAC)	+/-0.7ns		70h		2
25	DDR SDRAM cycle time at CL=1.5(tCK), 2.0(tCK)	7.5ns	-	75h	-	2
26	DDR SDRAM access time from clock at CL=1.5(tAC)	+/-0.75ns	-	75h	-	2
27	Minimum row precharge time(tRP)	15ns	18ns	3Ch	48h	
28	Minimum row activate to row active delay(tRRD)	10ns	12ns	28h	30h	
29	Minimum RAS to CAS delay(tRCD)	15ns	18ns	3Ch	48h	
30	Minimum active to precharge time(tRAS)	40ns	42ns	28h	2Ah	
31	Module row density	512MB		80h		
32	Command and address signal input setup time(tIS)	0.60ns	0.75ns	60h	75h	
33	Command and address signal input hold time(tIH)	0.60ns	0.75ns	60h	75h	
34	Data signal input setup time(tDS)	0.40ns	0.45ns	40h	45h	
35	Data signal input hold time(tDH)	0.40ns	0.45ns	40h	45h	
36~40	Reserved for VCSDRAM	Undefined		00h		
41	Minimum active / auto-refresh time (tRC)	55ns	60ns	37h	3Ch	
42	Minimum auto-refresh to active/auto-refresh command period(tRFC)	70ns	72ns	46h	48h	
43	Maximum cycle time (tCK max)	10ns	12ns	28h	30h	
44	Maximim DQS-DQ skew time(tDQSQ)	0.4ns		28h		
45	Maximum read data hold skew factor(tQHS)	0.5ns		50h		
46~61	Superset information(may be used in future)	Undefined		00h		
62	SPD Revision code	Initial release		00h		
63	Checksum for Bytes 0~62	-		BFh	4Fh	

SERIAL PRESENCE DETECT

- continued -

Byte#	Function Description	Function Supported		Hexa Value		Note
		D43	J	D43	J	
64	Manufacturer JEDEC ID Code	Hynix JEDEC ID		ADh		
65~71	--------- Manufacturer JEDEC ID Code	-		00h		
72	Manufacturing location	Hynix(Korea Area) HSA(United States Area) HSE(Europe Area) HSJ(Japan Area) Singapore Asia Area		0*h 1*h 2*h 3*h 4*h 5*h		6
73	Manufacture part number(Hynix Memory Module)	H		48h		
74	-------- Manufacture part number(Hynix Memory Module)	Y		59h		
75	-------- Manufacture part number(Hynix Memory Module)	M		4Dh		
76	Manufacture part number (DDR SDRAM)	D		44h		
77	Manufacture part number(Memory density)	5		35h		
78	Manufacture part number(Module Depth)	6		36h		
79	------- Manufacture part number(Module Depth)	4		34h		
80	Manufacture part number(Module type)	G		47h		
81	Manufacture part number(Data width)	7		37h		
82	-------Manufacture part number(Data width)	2		32h		
83	Manufacture part number(Refresh, # of Bank.)	6(8K refresh,4Bank)		36h		
84	Manufacture part number(Component Generation)	B		42h		
85	Manufacture part number(Component Package Type)	F		46h		
86	Manufacture part number(Component configuration)	8		38h		
87	Manufacture part number(Module Revision)	N		4Eh		
88	Manufacture part number(Minimum cycle time)	D	J	44h	4Ah	
89	Manufacture part number(Minimum cycle time)	4	-	34h	-	
90	Manufacture part number(Minimum cycle time)	3	-	33h	-	
91	Manufacture revision code(for Component)	-	-	-	-	
92	Manufacture revision code (for PCB)	-	-	-	-	
93	Manufacturing date(Year)	-	-	-	-	3
94	Manufacturing date(Week)	-	-	-	-	3
95~98	Module serial number	-	-	-	-	4
99~127	Manufacturer specific data (may be used in future)	Undefined		00h		5
128~255	Open for customer use	Undefined		00h		5

Note :

1. The bank address is excluded
2. This value is based on the component specification
3. These bytes are programmed by code of date week & date year
4. These bytes apply to Hynix's own Module Serial Number System
5. These bytes undefined and coded as '00h'
6. Refer to Hynix Web Site

Byte 85~86, Low power part

Byte #	Function Description	Function Supported	Hexa Value	Note
85	Manufacture part number(Low power part)	L	4Ch	
86	Manufacture part number(Component configuration)	F	46h	