19-0777; Rev 0; 4/07

600mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

General Description

The MAX8805Y/MAX8805Z high-frequency step-down converters are optimized for dynamically powering the power amplifier (PA) in WCDMA or NCDMA handsets. The devices integrate a high-efficiency PWM step-down converter for medium- and low-power transmission, and a 60mΩ typical bypass FET to power the PA directly from the battery during high-power transmission. Dual 200mA low-noise, high-PSRR low-dropout regulators (LDOs) for PA biasing are also integrated.

Two switching frequency options are available—2MHz (MAX8805Y) and 4MHz (MAX8805Z)—allowing optimization for smallest solution size or highest efficiency. Fast switching allows the use of small ceramic 2.2µF input and output capacitors while maintaining low ripple voltage. The feedback network is integrated, further reducing external component count and total solution size.

The MAX8805Y/MAX8805Z use an analog input driven by an external DAC to control the output voltage linearly for continuous PA power adjustment. At high duty cycle, the MAX8805Y/MAX8805Z automatically switch to the bypass mode, connecting the input to the output through a low-impedance (60mΩ typ) MOSFET. The user can also enable the bypass mode directly through a logic-control input.

The LDOs in the MAX8805Y/MAX8805Z are designed for low-noise operation (35µV_{RMS} typ). Each LDO is individually enabled through its own logic control interface.

The MAX8805Y/MAX8805Z are available in a 16-bump, 2mm x 2mm WLP package (0.7mm max height).

Applications

WCDMA/NCDMA Cellular Handsets

Wireless PDAs

Smartphones

Ordering Information

PART	PIN-PACKAGE	PKG CODE	SWITCHING FREQUENCY (MHz)
MAX8805YEWExy+T*	16 WLP-16	W162B2+1	2
MAX8805ZEWExy+T*	16 WLP-16	W162B2+1	4

+Denotes a lead-free package.

T = *Tape and reel package.*

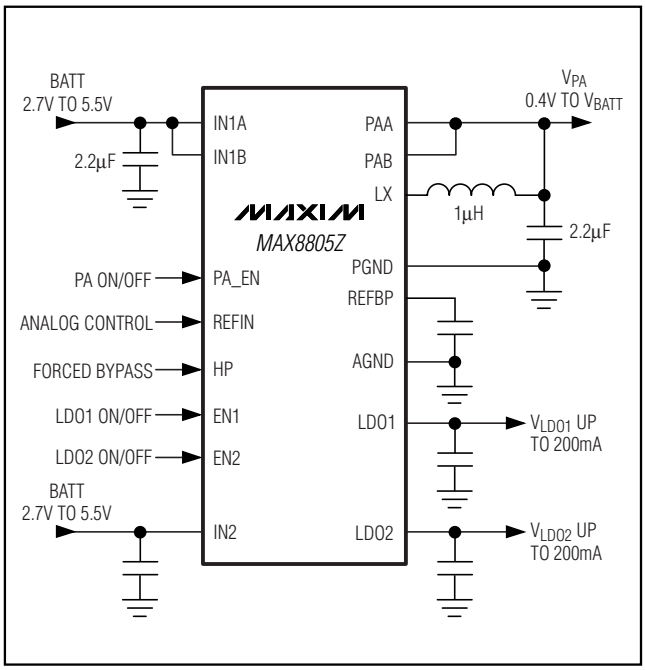
**xy is the output voltage code (see Table 1 in the Output Voltages section).*

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

Features

- **PA Step-Down Converter**
  - **7.5µs (typ) Settling Time for 0.8V to 3.4V Output Voltage Change**
  - **Dynamic Output Voltage Setting from 0.4V to V_{BATT}**
  - **60mΩ pFET and 100% Duty Cycle for Low Dropout**
  - **2MHz or 4MHz Switching Frequency**
  - **Low Output-Voltage Ripple**
  - **600mA Output Drive Capability**
  - **2% Maximum Accuracy**
  - **Tiny External Components**
- **Dual Low-Noise LDOs**
  - **Low 35µV_{RMS} (typ) Output Noise**
  - **High 70dB (typ) PSRR**
  - **Guaranteed 200mA Output Drive Capability**
  - **Individual ON/OFF Control**
- **Low 0.1µA Shutdown Current**
- **2.7V to 5.5V Supply Voltage Range**
- **Thermal Shutdown**
- **Tiny 2mm x 2mm x 0.7mm WLP Package (4 x 4 Grid)**

Typical Operating Circuit



Pin Configuration appears at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

IN1A, IN1B, IN2, REFIN, EN2, REFBP to AGND ...-0.3V to +6.0V
PAA, PAB, PA_EN, HP to AGND....-0.3V to (V_{IN1A}/V_{IN1B} + 0.3V)
LDO1, LDO2, EN1 to AGND .....-0.3V to (V_{IN2} + 0.3V)
IN2 to IN1B/IN1A .....-0.3V to +0.3V
PGND to AGND .....-0.3V to +0.3V
LX Current .....0.7A_{RMS}
IN1A/IN1B and PAA/PAB Current .....2A_{RMS}
PAA and PAB Short Circuit to GND or IN.....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Bump WLP (derate 12.5mW/°C above +70°C).....1W
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Bump Temperature (soldering, reflow).....+235°C

Note: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN1A} = V_{IN1B} = V_{IN2} = V_{PA_EN} = V_{EN1} = V_{EN2} = 3.6V, V_{HP} = 0V, V_{REFIN} = 0.9V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage	V_{IN1A}, V_{IN1B}, V_{IN2}		2.7		5.5	V
Input Undervoltage Threshold	V_{IN1A}, V_{IN1B}, V_{IN2} rising, 180mV typical hysteresis		2.52	2.63	2.70	V
Shutdown Supply Current	V_{PA_EN} = V_{EN1} = V_{EN2} = 0V	T_A = +25°C		0.1	4	µA
		T_A = +85°C		0.1		
No-Load Supply Current	V_{PA_EN} = 0V, I_{LDO1} = I_{LDO2} = 0A			150	250	µA
	V_{EN1} = V_{EN2} = 0V, I_{PA} = 0A, switching	MAX8805Y		3500		
		MAX8805Z		5000		
	V_{EN1} = V_{EN2} = 0V, V_{HP} = 3.6V			150		
THERMAL PROTECTION						
Thermal Shutdown	T_A rising, 20°C typical hysteresis			+160		°C
LOGIC CONTROL						
PA_EN, EN1, EN2, HP Logic-Input High Voltage	2.7V ≤ V_{IN1A} = V_{IN1B} = V_{IN2} ≤ 5.5V		1.4			V
PA_EN, EN1, EN2, HP Logic-Input Low Voltage	2.7V ≤ V_{IN1A} = V_{IN1B} = V_{IN2} ≤ 5.5V				0.4	V
Logic-Input Current (PA_EN, EN1, EN2, HP)	V_{IL} = 0V or V_{IH} = V_{IN1A} = 5.5V	T_A = +25°C		0.01	1	µA
		T_A = +85°C		0.1		
REFIN						
REFIN Common-Mode Range			0.1		2.2	V
REFIN to PA_ Gain (Falling Edge)	V_{REFIN} = 0.4V, 0.9V, 1.7V, 2.2V		1.96	2.00	2.04	V/V
REFIN Input Resistance				540		kΩ
REFIN Dual Mode™ Threshold	V_{REFIN} rising, 50mV hysteresis		0.45 x V_{IN2}	0.465 x V_{IN2}	0.48 x V_{IN2}	V

Dual Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1A} = V_{IN1B} = V_{IN2} = V_{PA_EN} = V_{EN1} = V_{EN2} = 3.6V, V_{HP} = 0V, V_{REFIN} = 0.9V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LX						
On-Resistance	p-channel MOSFET switch, I_{LX} = -40mA			0.18	0.6	Ω
	n-channel MOSFET rectifier, I_{LX} = 40mA			0.15	0.6	
LX Leakage Current	V_{IN1A} = V_{IN1B} = V_{IN2} = 5.5V, V_{LX} = 0V	T_A = +25°C		0.1	5	µA
		T_A = +85°C		1		
p-Channel MOSFET Peak Current Limit	V_{LX} = 0V		0.7	0.9	1.1	A
n-Channel MOSFET Valley Current Limit			0.5	0.7	0.9	A
Minimum On- and Off-Times				0.1		µs
Power-Up Delay	From PA_EN rising to LX rising			150	250	µs
BYPASS						
On-Resistance	p-channel MOSFET bypass, I_{OUT} = -90mA	T_A = +25°C		0.060	0.1	Ω
		T_A = +85°C		0.1		
Bypass Current Limit	V_{PA} = 0		0.8	1.2	1.8	A
Step-Down Current Limit in Bypass	V_{LX} = 0		0.7	0.9	1.1	A
Total Bypass Current Limit	V_{LX} = V_{PA} = 0		1.5	2.1	2.9	A
Bypass Off-Leakage Current	V_{IN1A} = V_{IN1B} = V_{IN2} = 5.5V, V_{PAA} = V_{PAB} = 0V	T_A = +25°C		0.01	10	µA
		T_A = +85°C		1		
LDO1						
Output Voltage V_{LDO1}	V_{IN2} = 5.5V, I_{LDO1} = 1mA; V_{IN2} = 3.4V, I_{LDO1} = 100mA	MAX8805YEWEAA+T	1.746	1.8	1.854	V
		MAX8805YEWEBC+T	2.425	2.5	2.575	
		MAX8805YEWECC+T	2.619	2.7	2.781	
		MAX8805YEWEDD+T	2.716	2.8	2.884	
		MAX8805YEWEEE+T	2.765	2.85	2.936	
		MAX8805YEWEGG+T	2.910	3.0	3.090	
Output Current			200			mA
Current Limit	V_{LDO1} = 0V		250	550	750	mA
Dropout Voltage	I_{LDO1} = 100mA, T_A = +25°C (V_{LDO1} ≥ 2.5V)			70	200	mV
Line Regulation	V_{IN2} stepped from 3.5V to 5.5V, I_{LDO1} = 100mA			2.4		mV
Load Regulation	I_{LDO1} stepped from 50µA to 200mA			25		mV
Power-Supply Rejection ΔV_{LDO1} / ΔV_{IN2}	10Hz to 10kHz, C_{LDO1} = 1µF, I_{LDO1} = 30mA			70		dB
Output Noise	100Hz to 100kHz, C_{LDO1} = 1µF, I_{LDO1} = 30mA			35		$µV_{RMS}$
Output Capacitor for Stable Operation	0 < I_{LDO1} < 10mA			100		nF
	0 < I_{LDO1} < 200mA			1		µF
Shutdown Output Impedance	V_{EN1} = 0V			1		kΩ

600mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1A} = V_{IN1B} = V_{IN2} = V_{PA_EN} = V_{EN1} = V_{EN2} = 3.6V, V_{HP} = 0V, V_{REFIN} = 0.9V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

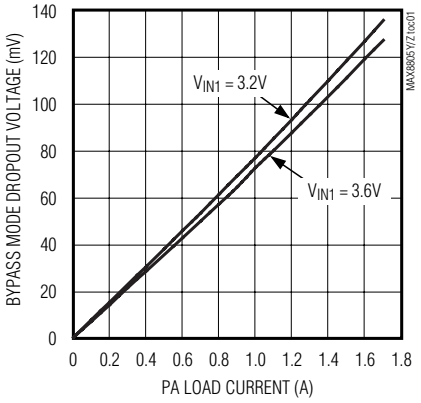
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LDO2						
Output Voltage V_{LDO2}	V_{IN2} = 5.5V, I_{LDO2} = 1mA; V_{IN2} = 3.4V, I_{LDO2} = 100mA	MAX8805YEWEAA+T	1.746	1.8	1.854	V
		MAX8805YEWEAC+T	2.619	2.7	2.781	
		MAX8805YEWEAD+T	2.716	2.8	2.884	
		MAX8805YEWEBE+T	2.765	2.85	2.936	
		MAX8805YEWEGG+T	2.910	3.0	3.090	
Output Current			200			mA
Current Limit	V_{LDO2} = 0V		250	550	750	mA
Dropout Voltage	I_{LDO2} = 100mA, T_A = +25°C			70	200	mV
Line Regulation	V_{IN2} stepped from 3.5V to 5.5V, I_{LDO2} = 100mA			2.4		mV
Load Regulation	I_{LDO2} stepped from 50µA to 200mA			25		mV
Power-Supply Rejection $\Delta V_{LDO2} / \Delta V_{IN2}$	10Hz to 10kHz, C_{LDO2} = 1µF, I_{LDO2} = 30mA			70		dB
Output Noise	100Hz to 100kHz, C_{LDO2} = 1µF, I_{LDO2} = 30mA			35		μV_{RMS}
Output Capacitor for Stable Operation	0µA < I_{LDO2} < 10mA			100		nF
	0µA < I_{LDO2} < 200mA			1		µF
Shutdown Output Impedance	V_{EN2} = 0V			1		kΩ
REFBP						
REFBP Output Voltage	0 ≤ I_{REFBP} ≤ 1µA		1.237	1.250	1.263	V
REFBP Supply Rejection	V_{IN2} stepped from 2.55V to 5.5V			0.2	5	mV

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

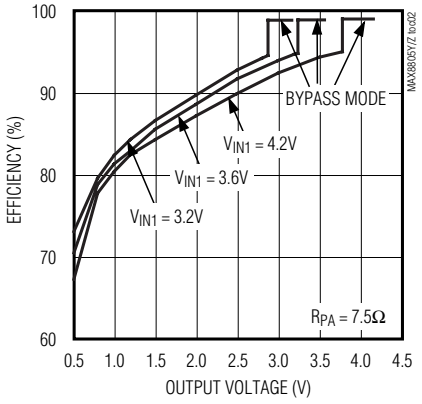
Typical Operating Characteristics

(V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V, V_{PA} = 1.2V, V_{LDO1} = 2.85V, V_{LDO2} = 2.85V, R_{PA} = 7.5Ω, circuit of Figure 5, T_A = +25°C, unless otherwise noted.)

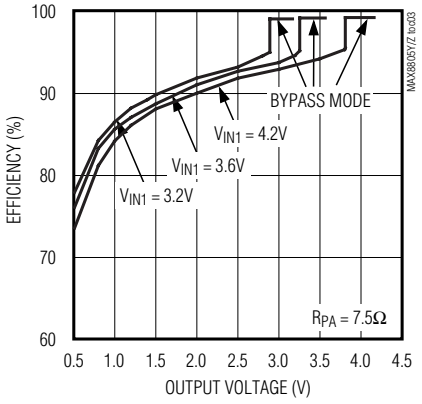
BYPASS MODE DROPOUT VOLTAGE vs. PA LOAD CURRENT



PA STEP-DOWN CONVERTER EFFICIENCY vs. OUTPUT VOLTAGE (MAX8805Z)



PA STEP-DOWN CONVERTER EFFICIENCY vs. OUTPUT VOLTAGE (MAX8805Y)



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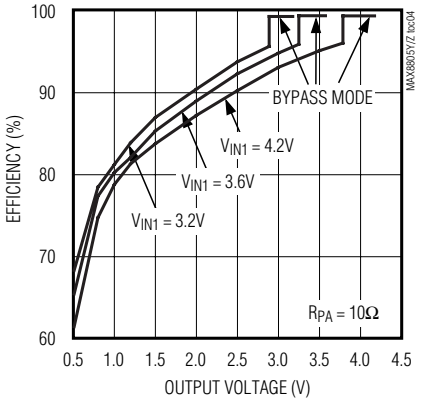

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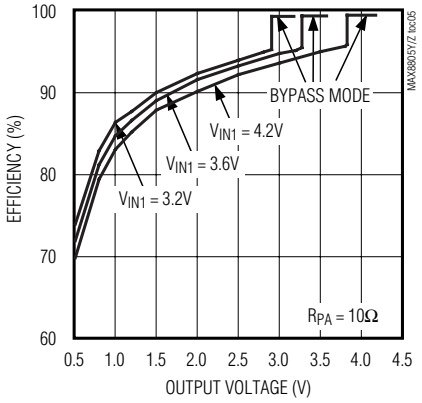
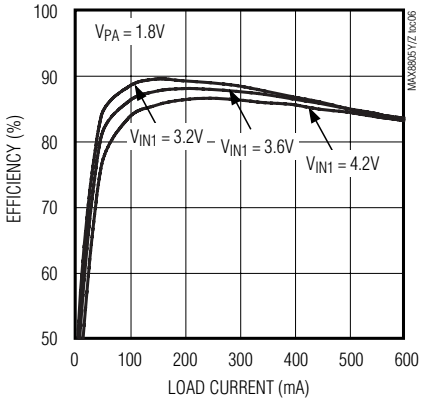
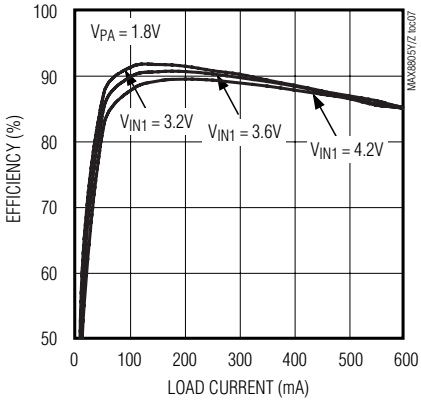


PA STEP-DOWN CONVERTER EFFICIENCY vs. LOAD CURRENT (MAX8805Z)



PA STEP-DOWN CONVERTER EFFICIENCY vs. LOAD CURRENT (MAX8805Y)



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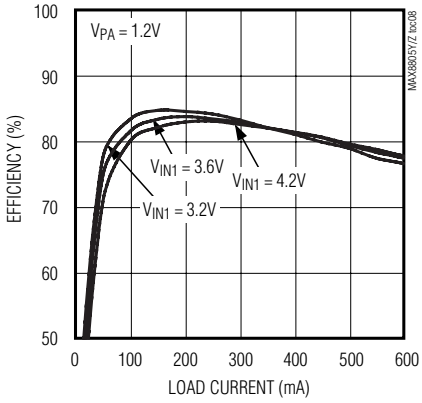
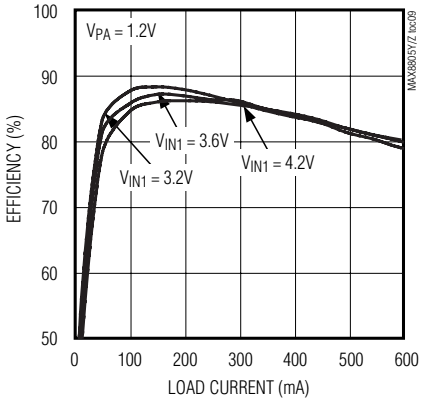


PA STEP-DOWN CONVERTER EFFICIENCY vs. LOAD CURRENT (MAX8805Y)

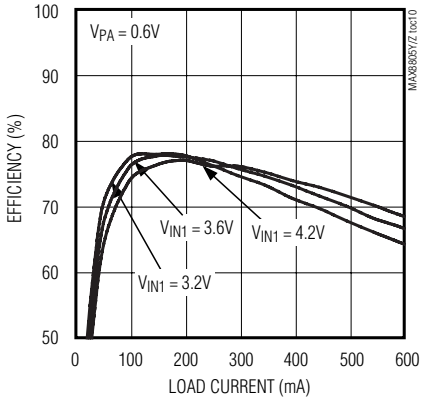


600mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

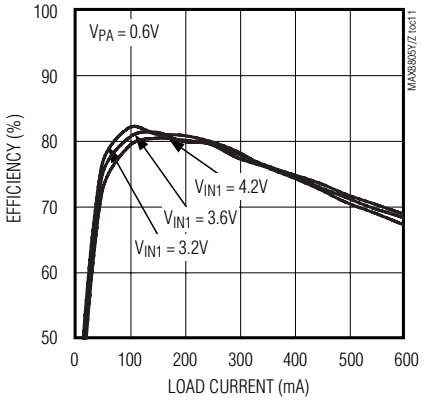
Typical Operating Characteristics (continued)

(V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V, V_{PA} = 1.2V, V_{LDO1} = 2.85V, V_{LDO2} = 2.85V, R_{PA} = 7.5Ω, circuit of Figure 5, T_A = +25°C, unless otherwise noted.)

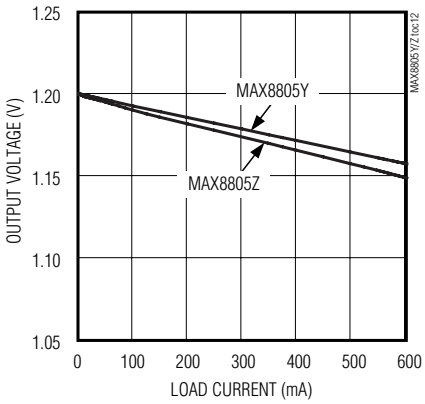
PA STEP-DOWN CONVERTER EFFICIENCY vs. LOAD CURRENT (MAX8805Z)



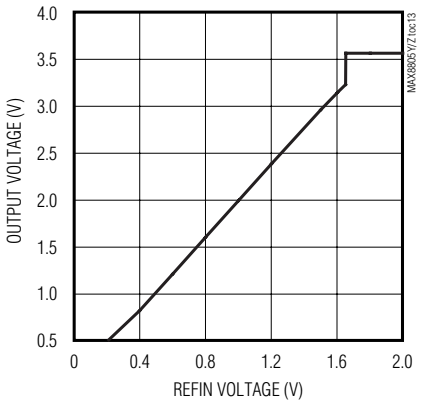
PA STEP-DOWN CONVERTER EFFICIENCY vs. LOAD CURRENT (MAX8805Y)



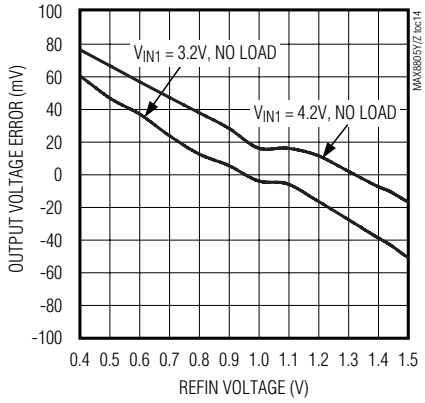
PA STEP-DOWN CONVERTER OUTPUT VOLTAGE vs. LOAD CURRENT



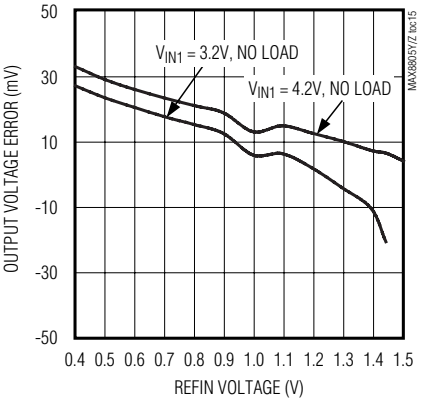
PA STEP-DOWN CONVERTER OUTPUT VOLTAGE vs. REFIN VOLTAGE



REFIN vs. REFIN TO OUT GAIN (MAX8805Z)



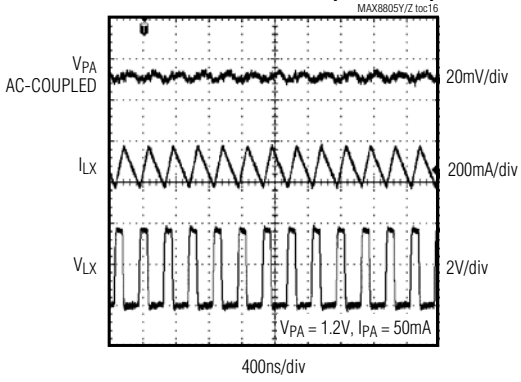
REFIN vs. REFIN TO OUT GAIN (MAX8805Y)



Typical Operating Characteristics (continued)

(V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V, V_{PA} = 1.2V, V_{LDO1} = 2.85V, V_{LDO2} = 2.85V, R_{PA} = 7.5Ω, circuit of Figure 5, T_A = +25°C, unless otherwise noted.)

PA STEP-DOWN CONVERTER LIGHT-LOAD SWITCHING WAVEFORMS (MAX8805Z)



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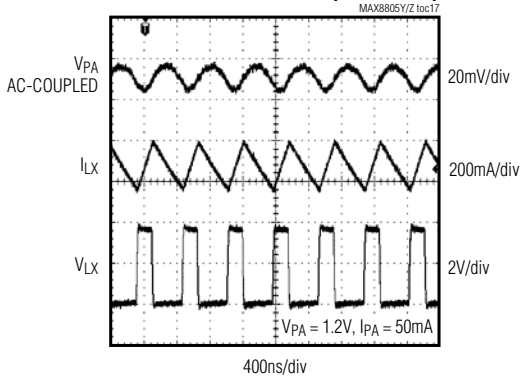
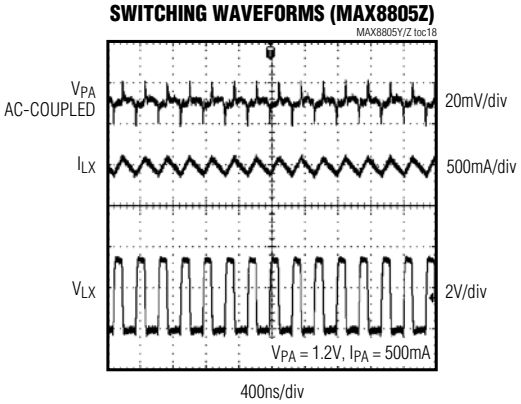
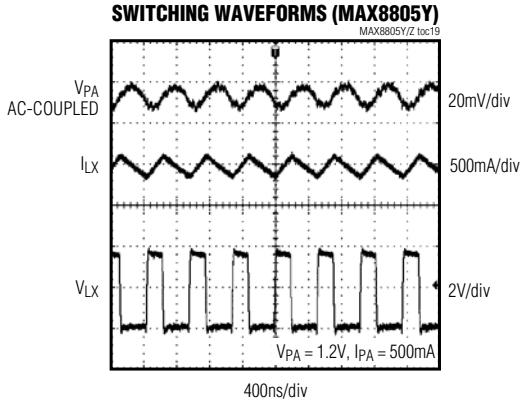


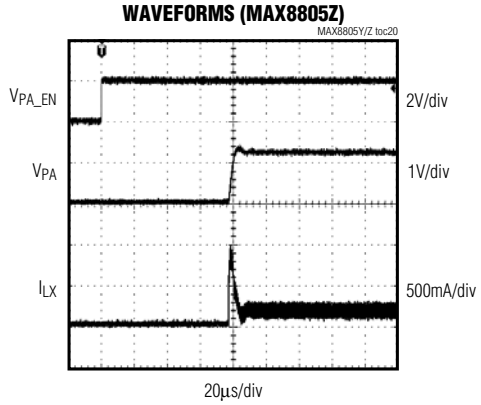
PA STEP-DOWN HEAVY-LOAD SWITCHING WAVEFORMS (MAX8805Z)



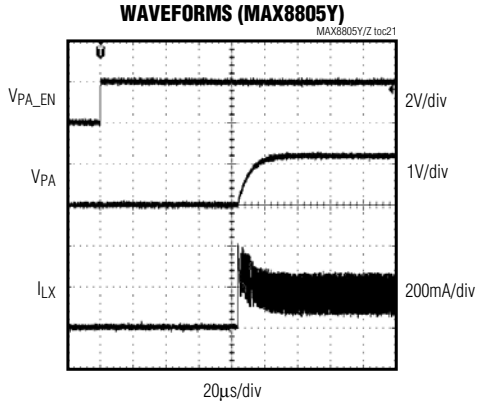
PA STEP-DOWN HEAVY-LOAD SWITCHING WAVEFORMS (MAX8805Y)



PA STEP-DOWN SOFT-START WAVEFORMS (MAX8805Z)



PA STEP-DOWN SOFT-START WAVEFORMS (MAX8805Y)

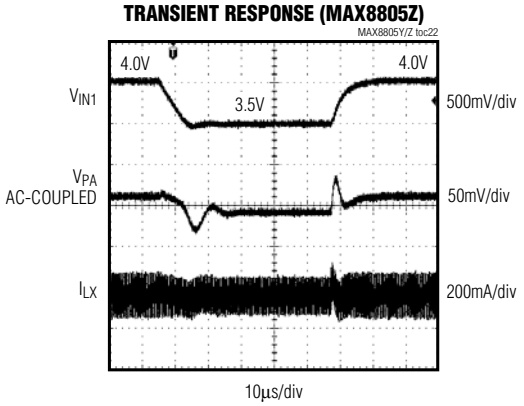


600mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

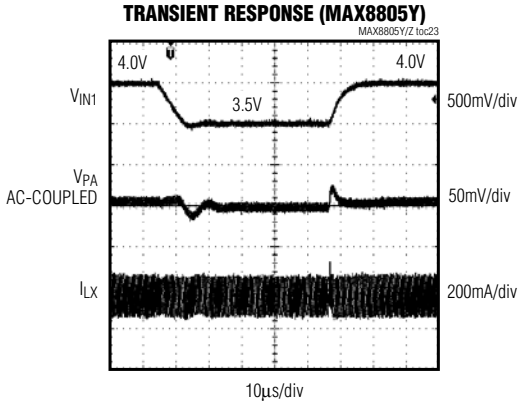
Typical Operating Characteristics (continued)

(V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V, V_{PA} = 1.2V, V_{LDO1} = 2.85V, V_{LDO2} = 2.85V, R_{PA} = 7.5Ω, circuit of Figure 5, T_A = +25°C, unless otherwise noted.)

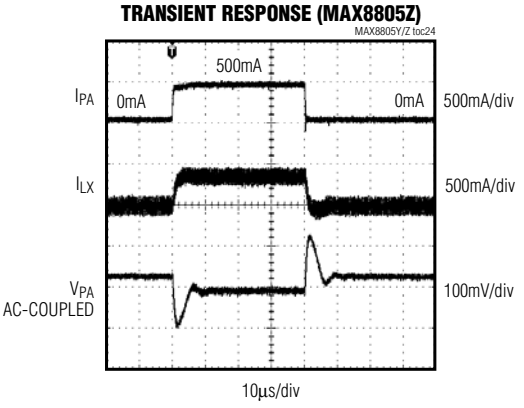
PA STEP-DOWN CONVERTER LINE TRANSIENT RESPONSE (MAX8805Z)



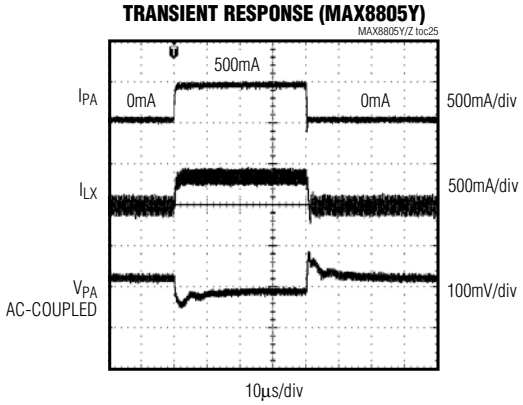
PA STEP-DOWN CONVERTER LINE TRANSIENT RESPONSE (MAX8805Y)



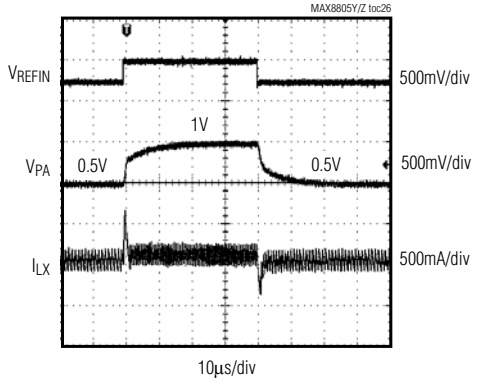
PA STEP-DOWN CONVERTER LOAD TRANSIENT RESPONSE (MAX8805Z)



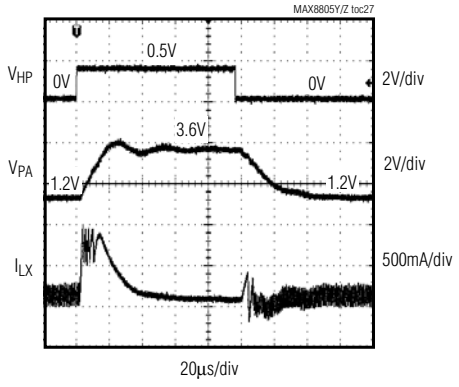
PA STEP-DOWN CONVERTER LOAD TRANSIENT RESPONSE (MAX8805Y)



PA STEP-DOWN CONVERTER OUTPUT VOLTAGE TRANSIENT RESPONSE



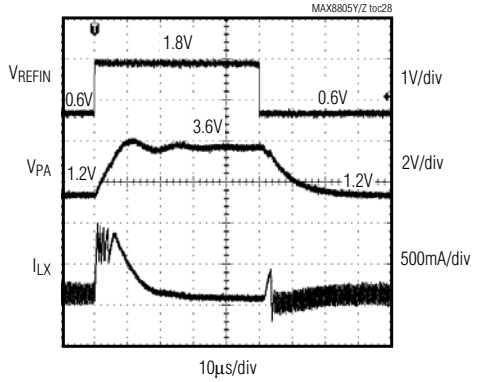
PA STEP-DOWN CONVERTER FORCED BYPASS-FET TRANSIENT RESPONSE



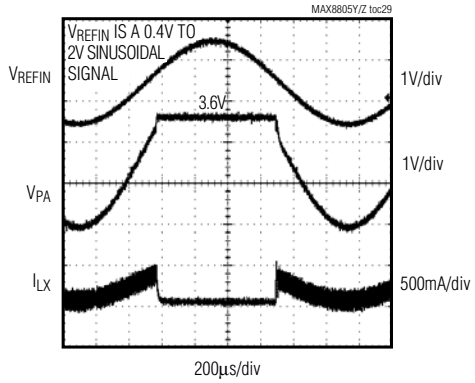
Typical Operating Characteristics (continued)

(V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V, V_{PA} = 1.2V, V_{LDO1} = 2.85V, V_{LDO2} = 2.85V, R_{PA} = 7.5Ω, circuit of Figure 5, T_A = +25°C, unless otherwise noted.)

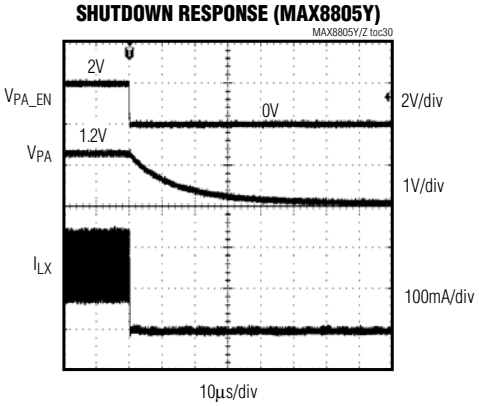
PA STEP-DOWN CONVERTER AUTOMATIC BYPASS-FET TRANSIENT RESPONSE



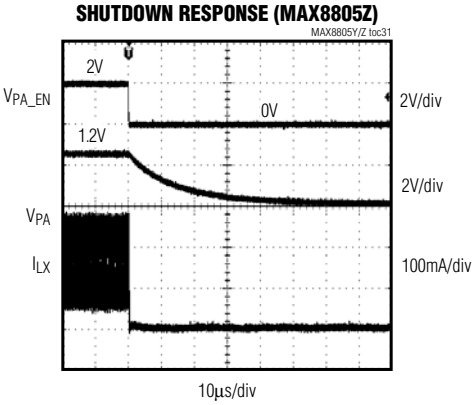
PA STEP-DOWN CONVERTER AUTOMATIC BYPASS-FET TRANSIENT RESPONSE



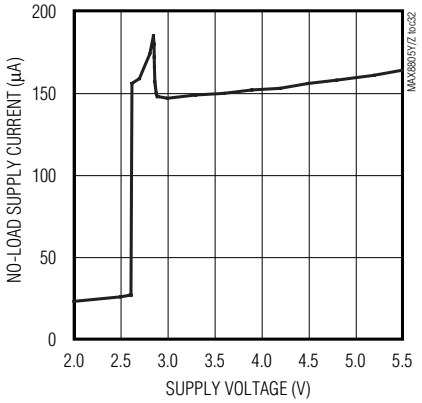
PA STEP-DOWN CONVERTER SHUTDOWN RESPONSE (MAX8805Y)



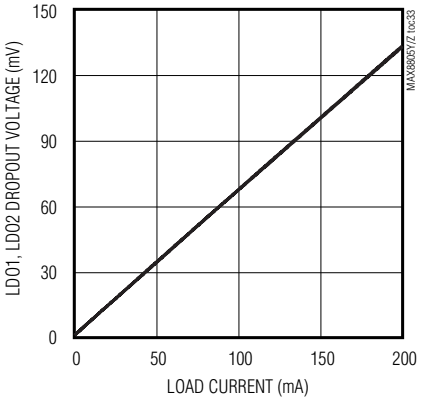
PA STEP-DOWN CONVERTER SHUTDOWN RESPONSE (MAX8805Z)



LDO1, LDO2 SUPPLY CURRENT vs. SUPPLY VOLTAGE



LDO1, LDO2 DROPOUT VOLTAGE vs. LOAD CURRENT

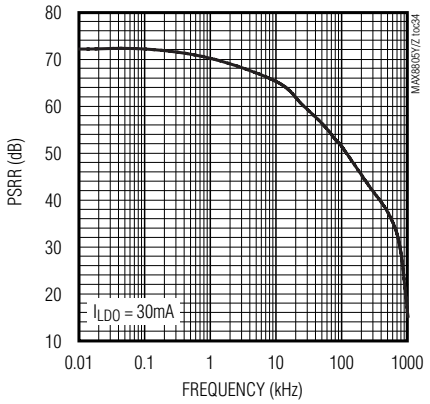


600mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

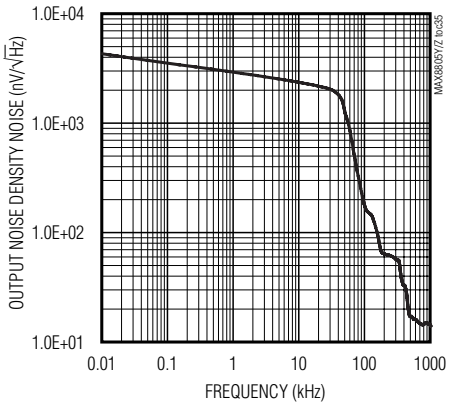
Typical Operating Characteristics (continued)

(V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V, V_{PA} = 1.2V, V_{LDO1} = 2.85V, V_{LDO2} = 2.85V, R_{PA} = 7.5Ω, circuit of Figure 5, T_A = +25°C, unless otherwise noted.)

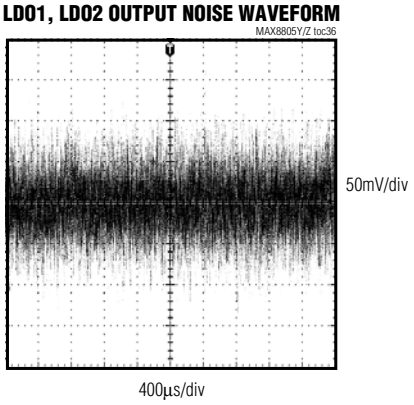
LDO PSRR vs. FREQUENCY



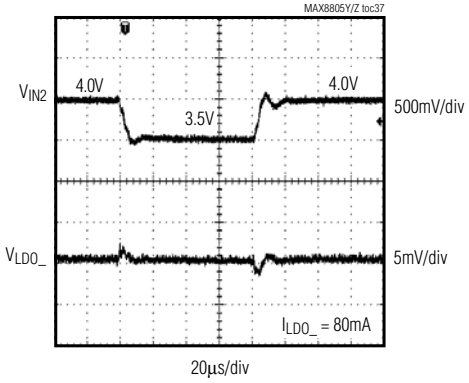
LDO OUTPUT NOISE SPECTRAL DENSITY vs. FREQUENCY



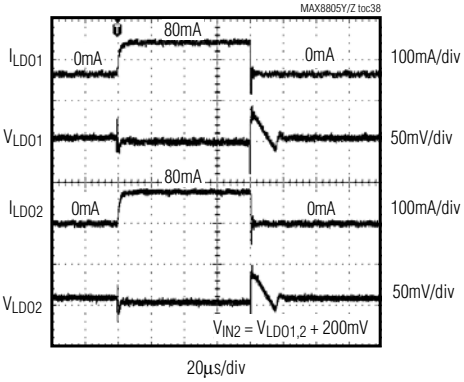
LDO1, LDO2 OUTPUT NOISE WAVEFORM



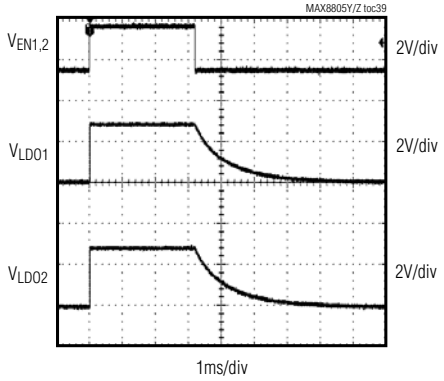
LDO LINE TRANSIENT RESPONSE



LDO1, LDO2 LOAD TRANSIENT RESPONSE NEAR DROPOUT



LDO1, LDO2 TURN ON AND SHUTDOWN RESPONSE



Pin Description

PIN	NAME	FUNCTION
A1	REFBP	Reference Noise Bypass. Bypass REFBP to AGND with a 0.22µF ceramic capacitor to reduce noise on the LDO outputs. REFBP is internally pulled down through a 1kΩ resistor during shutdown.
A2	AGND	Low-Noise Analog Ground
A3	REFIN	DAC-Controlled Input. The output of the PA step-down converter is regulated to 2 x V_{REFIN}. When V_{REFIN} reaches 0.465 x V_{IN2}, bypass mode is enabled.
A4	PGND	Power Ground for PA Step-Down Converter
B1	LDO2	200mA LDO Regulator 2 Output. Bypass LDO2 with a 1µF ceramic capacitor as close as possible to LDO2 and AGND. LDO2 is internally pulled down through a 1kΩ resistor when this regulator is disabled.
B2	PA_EN	PA Step-Down Converter Enable Input. Connect to IN_ or logic-high for normal operation. Connect to GND or logic-low for shutdown mode.
B3	EN2	LDO2 Enable Input. Connect to IN2 or logic-high for normal operation. Connect to AGND or logic-low for shutdown mode.
B4	LX	Inductor Connection. Connect an inductor from LX to the output of the PA step-down converter.
C1	IN2	Supply Voltage Input for LDO1, LDO2, and Internal Reference. Connect IN2 to a battery or supply voltage from 2.7V to 5.5V. Bypass IN2 with a 2.2µF ceramic capacitor as close as possible to IN2 and AGND. Connect IN2 to the same source as IN1A and IN1B.
C2	HP	High-Power Mode Set Input. Drive HP high to invoke forced bypass mode. Bypass mode connects the input of the PA step-down converter directly to its output through the internal bypass MOSFET. Drive HP low to disable the forced bypass mode.
C3, C4	IN1B, IN1A	Supply Voltage Input for PA Step-Down Converter. Connect IN1_ to a battery or supply voltage from 2.7V to 5.5V. Bypass the connection of IN1_ with a 2.2µF ceramic capacitor as close as possible to IN1_, and PGND. IN1A and IN1B are internally connected together. Connect IN1_ to the same source as IN2.
D1	LDO1	200mA LDO Regulator 1 Output. Bypass LDO1 with a 1µF ceramic capacitor as close as possible to LDO1 and AGND. LDO1 is internally pulled down through a 1kΩ resistor when this regulator is disabled.
D2	EN1	LDO1 Enable Input. Connect to IN2 or logic-high for normal operation. Connect to AGND or logic-low for shutdown mode.
D3, D4	PAB, PAA	PA Connection for Bypass Mode. Internally connected to IN1_ using the internal bypass MOSFET during bypass mode. PA_ is connected to the internal feedback network. Bypass PA_ with a 2.2µF ceramic capacitor as close as possible to PA_ and PGND.

600mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

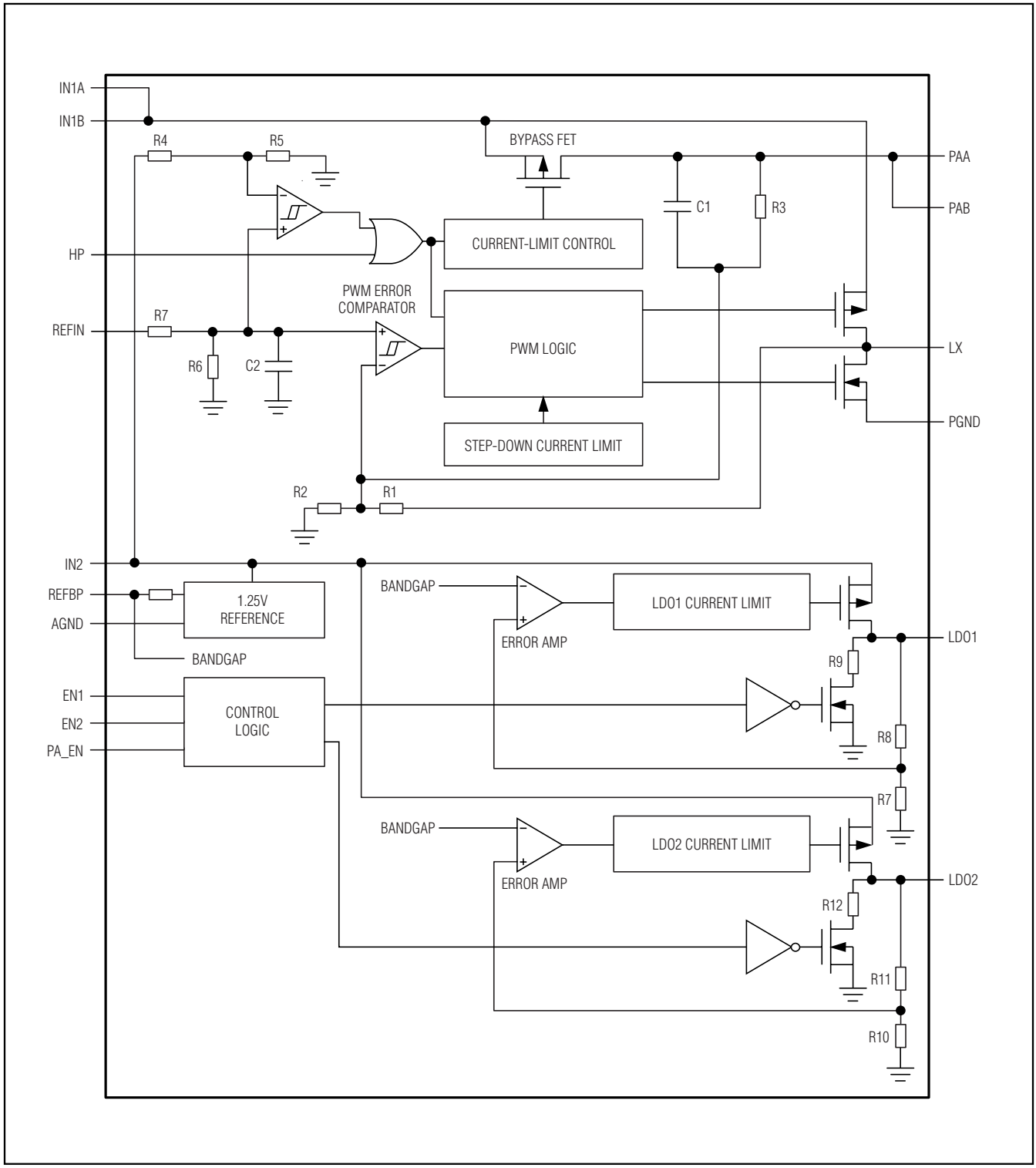


Figure 1. Block Diagram

Detailed Description

The MAX8805Y/MAX8805Z are designed to dynamically power the PA in WCDMA and NCDMA handsets. The devices contain a high-frequency, high-efficiency step-down converter, and two LDOs. The step-down converter delivers over 600mA. The hysteretic PWM control scheme provides extremely fast transient response, while 2MHz and 4MHz switching-frequency options allow the trade-off between efficiency and the smallest external components. A 60mΩ bypass FET connects the PA directly to the battery during high-power transmission.

Step-Down Converter Control Scheme

A hysteretic PWM control scheme ensures high efficiency, fast switching, fast transient response, low-output ripple, and physically tiny external components. The control scheme is simple: when the output voltage is below the regulation threshold, the error comparator begins a switching cycle by turning on the high-side switch. This high-side switch remains on until the minimum on-time expires and the output voltage is within regulation, or the inductor current is above the current-limit threshold. Once off, the high-side switch remains off until the minimum off-time expires and the output voltage falls again below the regulation threshold. During the off period, the low-side synchronous rectifier turns on and remains on until the high-side switch turns on again. The internal synchronous rectifier eliminates the need for an external Schottky diode.

Voltage-Positioning Load Regulation

The MAX8805Y/MAX8805Z step-down converters utilize a unique feedback network. By taking DC feedback from the LX node through R1 in Figure 1, the usual phase lag due to the output capacitor is removed, making the loop exceedingly stable and allowing the use of very small ceramic output capacitors. To improve the load regulation, resistor R3 is included in the feedback. This configuration yields load regulation equal to half of the inductor's series resistance multiplied by the load current. This voltage-positioning load regulation greatly reduces overshoot during load transients or when changing the output voltage from one level to another. However, when calculating the required REFIN voltage, the load regulation should be considered. Because inductor resistance is typically well specified and the typical PA is a resistive load, the MAX8805Y/MAX8805Z V_{REFIN} to V_{OUT} gain is slightly less than 2V/V.

Step-Down Converter Bypass Mode

During high-power transmission, the bypass mode connects IN1A and IN1B directly to PAA and PAB with the internal 60mΩ (typ) bypass FET, while the step-down converter is forced into 100% duty-cycle operation. The low on-resistance in this mode provides low dropout, long battery life, and high output current capability.

Forced and Automatic Bypass Mode

Invoke forced bypass mode by driving HP high or invoke automatic bypass mode by applying a high voltage to REFIN. To prevent excessive output ripple as the step-down converter approaches dropout, the MAX8805Y/MAX8805Z enter bypass mode automatically when $V_{REFIN} > 0.465 \times V_{IN2}$ (see Figure 2). Note that IN2 is used instead of IN1 to prevent switching noise from causing false enagement of automatic bypass mode. For this reason, IN2 must be connected to the same source as IN1.

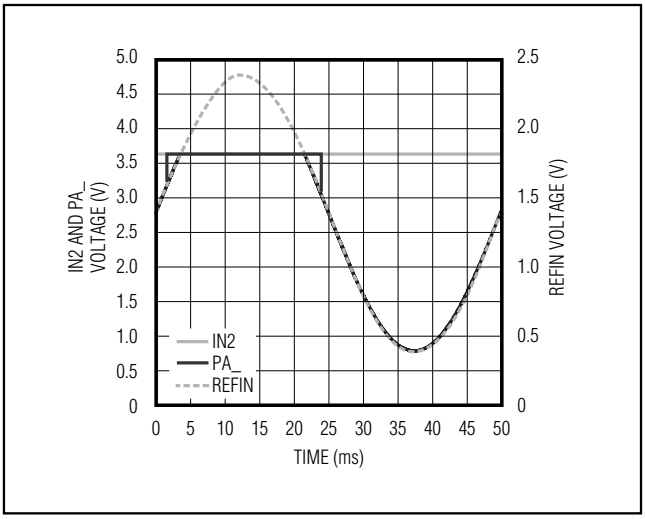


Figure 2. V_{IN2} and $V_{PA\_}$ with Automatic Entry/Exit into Bypass Mode

Shutdown Mode

Connect PA_EN to GND or logic-low to place the MAX8805Y/MAX8805Z PA step-down converter in shutdown mode. In shutdown, the control circuitry, internal switching MOSFET, and synchronous rectifier turn off and LX becomes high impedance. Connect PA_EN to IN1_ or logic-high for normal operation.

Connect EN1 or EN2 to GND or logic-low to place LDO1 or LDO2, respectively, in shutdown mode. In shutdown, the outputs of the LDOs are pulled to ground through an internal 1kΩ resistor.

When the PA step-down and LDOs are all in shutdown, the MAX8805Y/MAX8805Z enter a very low power state, where the input current drops to 0.1µA (typ).

600mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

Step-Down Converter Soft-Start

The MAX8805Y/MAX8805Z PA step-down converter has internal soft-start circuitry that limits inrush current at startup, reducing transients on the input source. Soft-start is particularly useful for supplies with high output impedance such as Li+ and alkaline cells. See the Soft-Start Waveforms in the *Typical Operating Characteristics.*

Analog REFIN Control

The MAX8805Y/MAX8805Z PA step-down converter uses REFIN to set the output voltage. The output voltage is regulated at twice the voltage applied at REFIN minus the load regulation. This allows the converter to operate in applications where dynamic voltage control is required.

Thermal Shutdown

Thermal shutdown limits total power dissipation in the MAX8805Y/MAX8805Z. If the junction temperature exceeds +160°C, thermal-shutdown circuitry turns off the IC, allowing it to cool. The IC turns on and begins soft-start after the junction temperature cools by 20°C. This results in a pulsed output during continuous thermal-overload conditions.

Applications Information

Output Voltages

The MAX8805Y/MAX8805Z PA step-down converters set the PA_ output voltage to twice the voltage applied to REFIN.

LDO1 and LDO2 output voltages are determined by the part number suffix, as shown in Table 1.

LDO Dropout Voltage

The regulator's minimum input/output differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the MAX8805Y/MAX8805Z LDOs use a p-channel MOSFET pass transistor, their dropout voltages are a function of drain-to-source on-resistance ($R_{DS}(ON)$) multiplied by the load current (see the *Typical Operating Characteristics*).

Inductor Selection

The MAX8805Y operates with a switching frequency of 2MHz and utilizes a 2.2µH inductor. The MAX8805Z operates with a switching frequency of 4MHz and utilizes a 1µH inductor. The higher switching frequency of the MAX8805Z allows the use of physically smaller inductors at the cost of slightly lower efficiency. The lower switching frequency of the MAX8805Y results in greater efficiency at the cost of a physically larger inductor. See the *Typical Operating Characteristics* for efficiency graphs for both the MAX8805Y and MAX8805Z.

Table 1. LDO1 and LDO2 Output Voltage Selection

PART	FREQUENCY (MHz)	LDO1 (V)	LDO2 (V)
MAX8805YEWEAA+T	2	1.80	1.80
MAX8805YEWEAE+T	2	1.80	2.85
MAX8805YEWEEE+T	2	2.85	2.85
MAX8805ZEWEAA+T	4	1.80	1.80
MAX8805ZEWEAE+T	4	1.80	2.85
MAX8805ZEWEEE+T	4	2.85	2.85

Note: *Contact the factory for other output-voltage options.*

The inductor's DC current rating only needs to match the maximum load of the application because the MAX8805Y/MAX8805Z feature zero current overshoot during startup and load transients. For optimum transient response and high efficiency, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range. See Table 2 for suggested inductors and manufacturers.

Output Capacitor Selection

For the PA step-down converter, the output capacitor (C_{PA}) is required to keep the output voltage ripple small and ensure regulation loop stability. C_{PA} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. A 2.2µF capacitor is recommended for most applications. For optimum load-transient performance and very low output ripple, the output capacitor value can be increased.

For LDO1 and LDO2, the minimum output capacitance required is dependent on the load currents. For loads less than 10mA, it is sufficient to use a 0.1µF capacitor for stable operation over the full temperature range. With rated maximum load currents, a minimum of 1µF is recommended. Reduce output noise and improve load-transient response, stability, and power-supply rejection by using larger output capacitors.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it is necessary to use 2.2µF or larger to ensure stability at temperatures below -10°C. With X7R or X5R dielectrics, 1µF is sufficient at all operating temperatures. These regulators are optimized for ceramic capacitors. Tantalum capacitors are not recommended.

Table 2. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	ESR (Ω)	CURRENT RATING (mA)	DIMENSIONS (mm)
Coilcraft	LPO3310	1.0 1.5 2.2	0.07 0.10 0.13	1600 1400 1100	3.3 x 3.3 x 1.0 = 11mm^3
FDK	MIPF2520	1.0 1.5 2.2	0.05 0.07 0.08	1500 1500 1300	2.5 x 2.0 x 1.0 = 5mm^3
	MIPS2520	1.3 2.0	0.09 0.11	1500 1200	2.5 x 2.0 x 1.0 = 5mm^3
	MIPF2016	1.0 2.2	0.11	1100	2.0 x 1.6 x 1.0 = 3.2mm^3
Hitachi	KSLI-252010	1.5 2.2	0.115 0.080	—	2.5 x 2.0 x 1.0 = 5mm^3
Murata	LQH32C_53	1.0 2.2	0.06 0.10	1000 790	3.2 x 2.5 x 1.7 = 14mm^3
Sumida	CDRH2D09	1.2 1.5 2.2	0.08 0.09 0.12	590 520 440	3.0 x 3.0 x 1.0 = 9mm^3
Taiyo Yuden	CDRH2D11	1.5 2.2 3.3	0.05 0.08 0.10	680 580 450	3.2 x 3.2 x 1.2 = 12mm^3
	CB2518T	2.2 4.7	0.09 0.13	510 340	2.5 x 1.8 x 2.0 = 9mm^3
TOKO	D3010FB	1.0	0.20	1170	3.0 x 3.0 x 1.0 = 9mm^3
	D2812C	1.2 2.2	0.09 0.15	860 640	3.0 x 3.0 x 1.2 = 11mm^3
	D310F	1.5 2.2	0.13 0.17	1230 1080	3.6 x 3.6 x 1.0 = 13mm^3
	D312C	1.5 2.2	0.10 0.12	1290 1140	3.6 x 3.6 x 1.2 = 16mm^3

Input Capacitor Selection

The input capacitor (C_{IN1}) of the PA converter reduces the current peaks drawn from the battery or input power source and reduces switching noise in the MAX8805Y/MAX8805Z. The impedance of C_{IN1} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. A 2.2µF capacitor is recommended for most applications. For optimum noise immunity and low input ripple, the input capacitor value can be increased.

For the LDOs, use an input capacitance equal to the value of the sum of the output capacitance of LDO1 and LDO2. Larger input capacitor values and lower ESR provide better noise rejection and line transient response.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it may be necessary to use two times the sum of the output capacitor values of LDO1 and LDO2 (or larger) to ensure stability at temperatures below -10°C. With X7R or X5R dielectrics, a capacitance equal to the sum is sufficient at all operating temperatures.

600mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

Thermal Considerations

In most applications, the MAX8805Y/MAX8805Z do not dissipate much heat due to their high efficiency. However, in applications where the MAX8805Y/MAX8805Z run at high ambient temperature with heavy loads, the heat dissipated may exceed the maximum junction temperature of the IC. If the junction temperature reaches approximately +160°C, all power switches are turned off and LX and PA_ become high impedance, and LDO1 and LDO2 are pulled down to ground through an internal 1kΩ pulldown resistor.

The MAX8805Y/MAX8805Z maximum power dissipation depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The power dissipated in the device is:

$$P_{DISS} = P_{PA} \times (1/\eta_{PA} - 1) + I_{LDO1} \times (V_{IN2} - V_{LDO1}) + I_{LDO2} \times (V_{IN2} - V_{LDO2})$$

where η_{PA} is the efficiency of the PA step-down converter and P_{PA} is the output power of the PA step-down converter.

The maximum allowed power dissipation is:

$$P_{MAX} = (T_{JMAX} - T_A) / \theta_{JA}$$

where $(T_{JMAX} - T_A)$ is the temperature difference between the MAX8805Y/MAX8805Z die junction and the surrounding air; θ_{JA} is the thermal resistance of the junction through the PCB, copper traces, and other materials to the surrounding air.

PCB Layout

High switching frequencies and relatively large peak currents make the PCB layout a very important part of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, resulting in a stable and well-regulated output. Connect C_{IN1} close to IN1A/IN1B and PGND. Connect the inductor and output capacitor as close as possible to the IC and keep their traces short, direct, and wide. Keep noisy traces, such as the LX node, as short as possible. Figure 3 illustrates an example PCB layout and routing scheme.

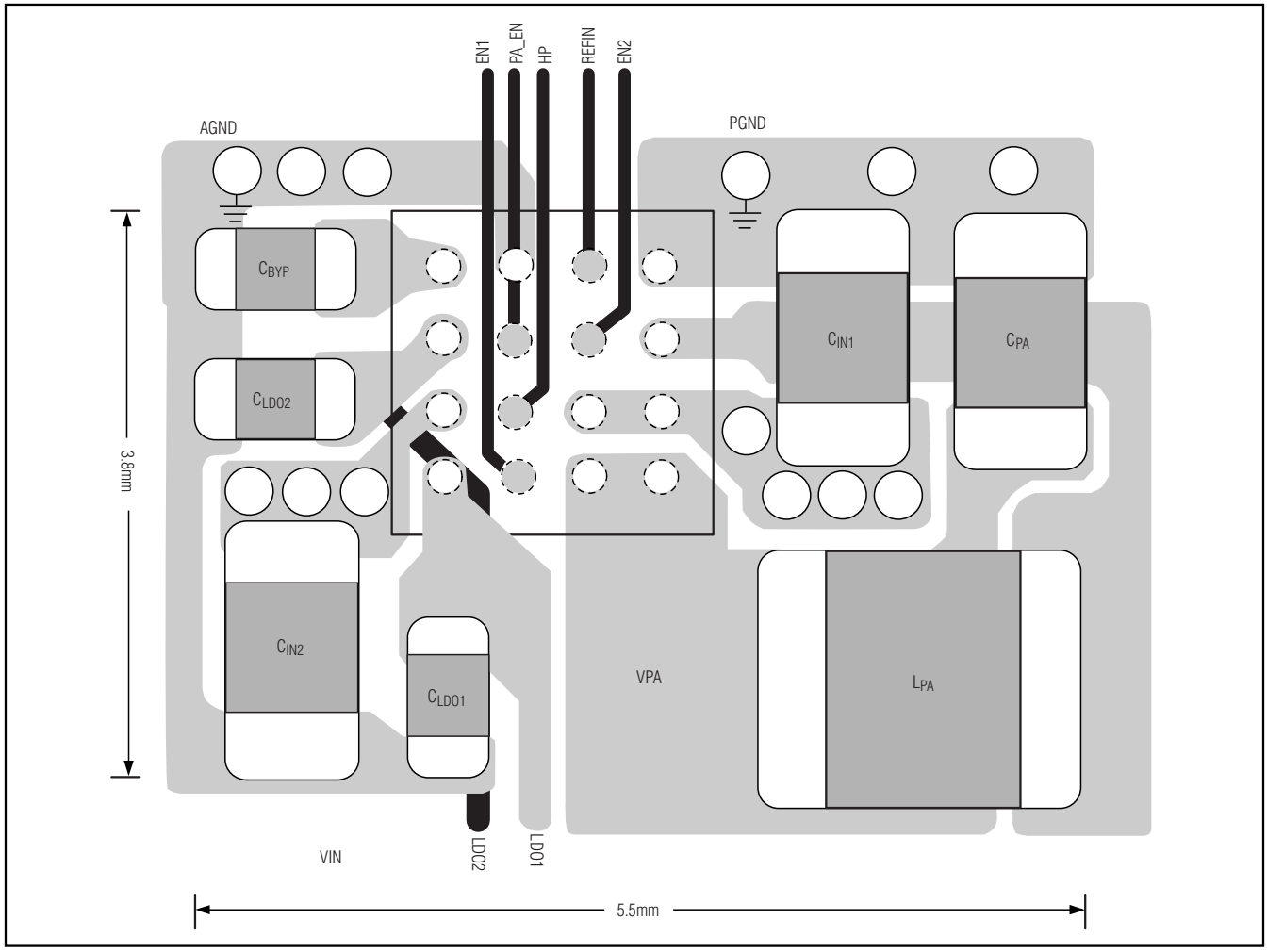


Figure 3. Recommended PCB Layout

600mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

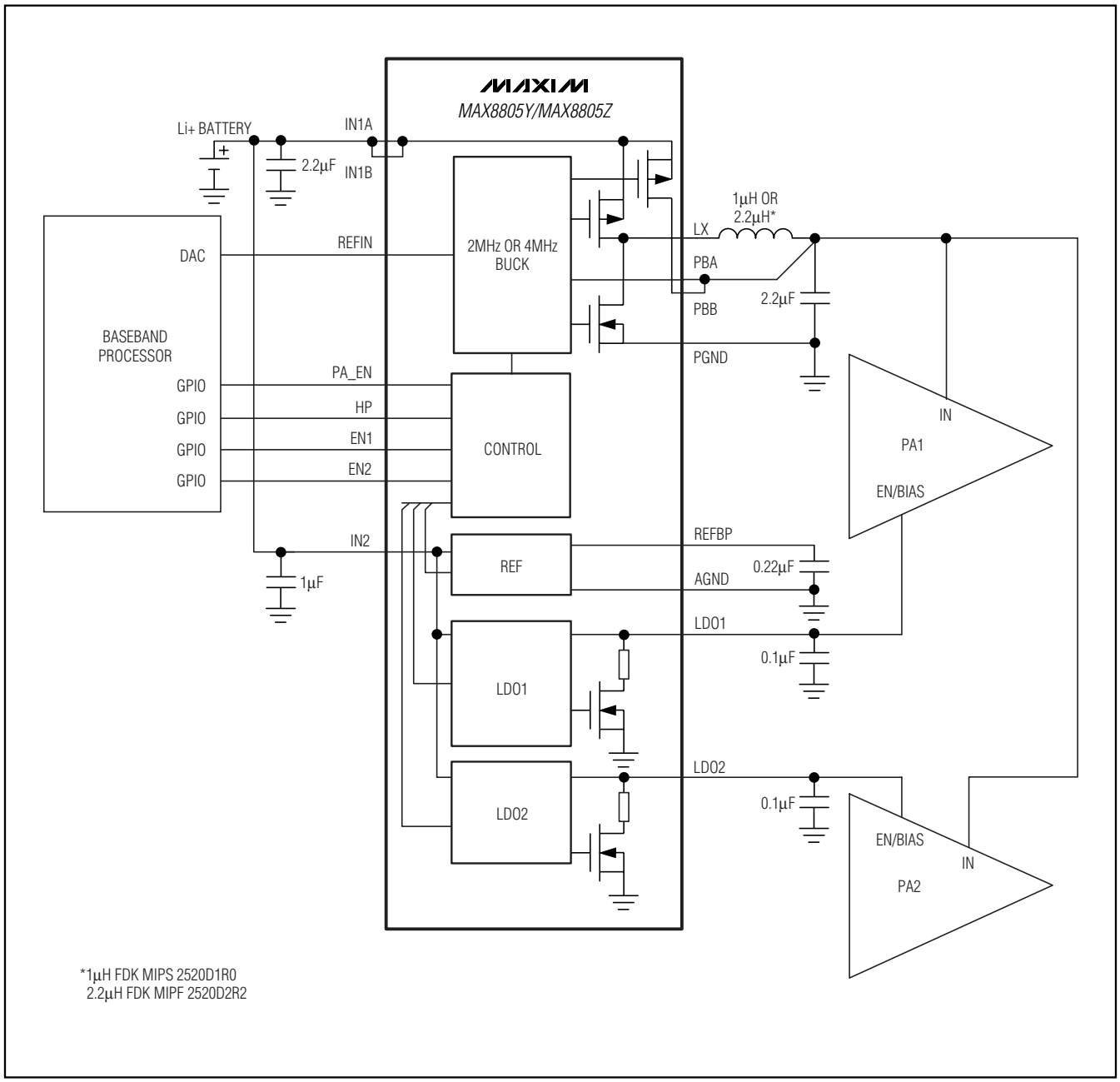


Figure 4. Typical Application Circuit Using LDOs for PA Enable/Bias

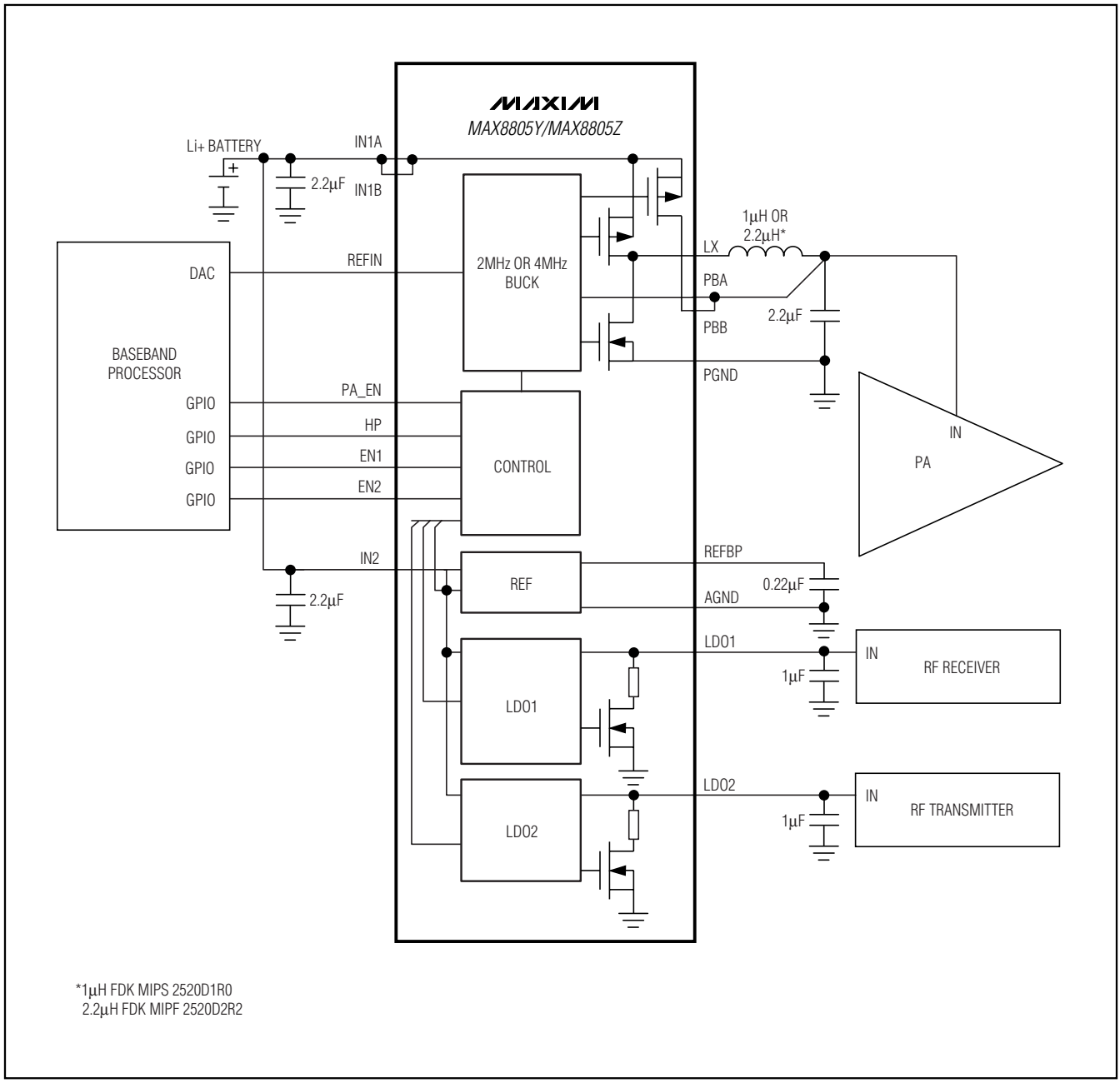
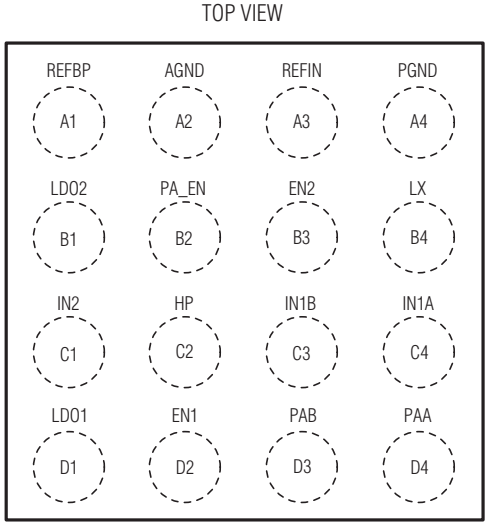


Figure 5. Typical Application Circuit Using LDOs for RF Power

600mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power

Pin Configuration



(BUMP IN BOTTOM)
16-Bump, 2mm × 2mm WLP

Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)