

MV65030

64-WORD x 9-BIT FIRST-IN FIRST-OUT MEMORY

(SUPERSEDES MARCH 1987 EDITION)

The MV65030 is an asynchronous first-in first-out memory, organised as 64 9-bit words. The device accepts a 9-bit parallel word, D0 - D8, under control of the shift in (SI) input. Multiple devices can be used in parallel to satisfy wider data requirements. Data entered into the FIFO ripples through the device to the outputs Q0 - Q8. Up to 64 words may be entered before any words are read from the memory. The stored words stack up at the output in the order in which they were entered.

Activating the shift out control (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals respectively indicate that the device can accept new data or that the output contains valid data. If the input ready output remains inactive, the device is full. If the output ready signal remains inactive, the device is empty.

Since reading and writing operations are completely independent, the device can be used as a buffer between two digital systems operating asynchronously and with widely differing clock frequencies.

- 35MHz Guaranteed Data Rate, 40MHz Typical (MV65030-35)
- < 200mW at 40MHz
- < 55mW Standby
- Operating Temperature Range:
 - 40°C to +85°C Industrial
 - 55°C to +125°C Military
- Single 5V Supply, ±10% Tolerance
- Tri-State Outputs

APPLICATIONS

- Asynchronous Buffer between Digital Systems
- I/O Formatting in DSP Systems
- Video Time Base Correction
- Printer Buffers
- Disk or Tape Interfaces

ASSOCIATED PRODUCTS

- MV65401/2/3/4** 64 by 4/5, Bistate/Tristate Stand-alone FIFOs
- MV66401/2/3/4** 64 by 4/5, Bistate/Tristate Cascadable FIFOs
- MV68030** 64 by 9, Tristate Cascadable FIFO
- MV61901/2/3** 1K by 9 FIFOs

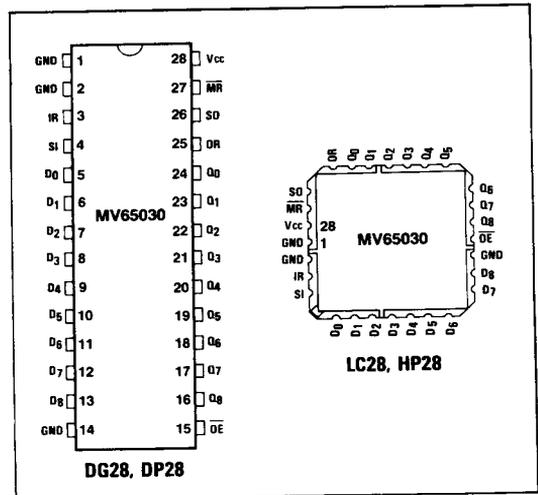


Fig.1 Pin connections - top view

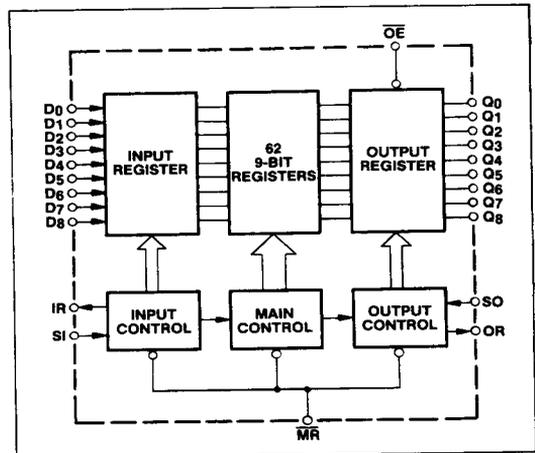


Fig.2 Block diagram

FIFO OPERATION

The MV65030 FIFO contain 64 nine bit data registers. Data is initially loaded from the data inputs D0 - D8 by applying a low to high transition on the shift in (SI) input. IR goes low indicating that data has been entered into the first data register and the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the IR goes high indicating the inputs are available for another data word.

The data falling through the registers stacks up at the output end. A high on OR indicates there is valid data on the data outputs Q0 - Q8. A shift out (SO) can then be used to shift the data out of the FIFO. A low to high transition on SO causes OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the data in the next to last register position moves into the last register position and on to the outputs. If the memory is emptied by reading out all of the data, then, when the last word is being read out and SO goes high, OR will go low as before. When SO next goes low however, there is no data to move into the last location so OR will remain low until more data is entered. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The data word can be extended in width by using more than one FIFO as shown in Fig.10. The status flags must be gated as shown to allow for possible delay variations between devices.

An overriding master reset (\overline{MR}) is used to reset all control register bits and remove the data from the output (i.e. reset the output to all low).

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_{IN} (see Note 3)	-0.9V to $V_{CC} + 0.9V$
DC voltage applied to output when high impedance	-0.5V to 7.0V
Clamp diode current per pin (see Note 2)	+18mA
Storage temperature T_s	-65°C to +150°C
Ambient temperature with power applied T_{amb}	-55°C to +125°C
Package power dissipation DP	450mW
DG	1000mW
LC	1000mW
HP	500mW

NOTES

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Input voltages more negative than -0.9V cause clamp diode current to flow. The maximum negative voltage depends on the source impedance.

RECOMMENDED OPERATING CONDITIONS

Supply voltage V_{CC}	$5V \pm 10\%$
Min. input high level V_{IH}	+2V
Max. input low level V_{IL}	+0.8V
Ambient temperature	
Industrial	-40°C to 85°C
Military	-55°C to 125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Under Recommended operating conditions

DC Characteristics

Characteristic	Symbol	INDUSTRIAL				MILITARY		Unit	Conditions
		MV65030-25		MV65030-35		Min.	Max.		
		Min.	Max.	Min.	Max.				
Output high level $V_{IN} = V_{IH}$ or V_{IL} , $I_{OH} = -1mA$	V_{OH}	2.4		2.4				V	Note 2 $V_{CC} = \text{max.}$ $T_{amb} = 85^\circ C$ $I_{LOAD} = 0mA$ $V_{CC} = \text{max.}$ $I_{LOAD} = 0mA$ All inputs at V_{IL}
Output low level $V_{IN} = V_{IH}$ or V_{IL} , $I_{OL} = 8mA$	V_{OL}		0.5		0.5			V	
Input leakage $V_{IN} = V_{IH}$ or V_{IL}	I_{IN}	-10	+10	-10	+10			μA	
Output leakage $GND \leq V_{OUT} \leq V_{CC}$ $V_{CC} = V_{CC \text{ max.}}$	I_{OZ}	-50	+50	-50	+50			μA	
Short circuit current	I_{OS}		80		80			mA	
Supply current	I_{CC}		30		40			mA	
Standby current			10		10				

AC Characteristics - Using test circuit

Characteristic	Symbol	INDUSTRIAL				MILITARY		Unit	Condition
		MV65030-25		MV65030-35		Min.	Max.		
		Min.	Max.	Min.	Max.				
Maximum operating frequency	f _o	25		35				MHz	Note 4
SI HIGH time	t _{PHSI}	15		10				ns	
SI LOW time	t _{PLSI}	20		15				ns	
Data setup to SI	t _{SSI}	0		0				ns	Note 5
Data hold from SI	t _{HSI} (a)	30		20				ns	Note 5,6
	t _{HSI} (b)	t _{PHSI} + 5		t _{PHSI} + 5				ns	
Delay, SI HIGH to IR LOW	t _{DLIR}		21		15			ns	
Delay, SI LOW to IR HIGH	t _{DHIR}		25		18			ns	
SO HIGH time	t _{PHSO}	15		8				ns	
SO LOW time	t _{PLSO}	20		15				ns	
Delay, SO HIGH to OR LOW	t _{DLOR}		21		15			ns	
Delay, SO LOW to OR HIGH	t _{DHOR}		25		20			ns	
Data setup to OR HIGH	t _{SOR}	-15		-12				ns	
Data hold from SO LOW	t _{HSO}	8		5				ns	
Bubble through time	t _{BT}		1200		1000			ns	
MR pulse width	t _{PMR}	50		30				ns	
MR HIGH to SI HIGH	t _{DSI}	50		30				ns	
MR LOW to OR LOW	t _{DOR}		50		30			ns	
MR LOW to IR HIGH	t _{DIR}		50		30			ns	
MR LOW to output LOW	t _{LZMR}		50		30			ns	Note 7
Output valid from OE LOW	t _{OOE}		40		28			ns	
Output HIGH-Z from OE HIGH	t _{HZOE}		40		28			ns	

NOTES

- 1/f_o > t_{PHSI} + t_{DHIR} 1/f_o > t_{PHSO} + t_{DHOR}.
- t_{SSI} and t_{HSI} apply when memory is not full.
- Hold time is the lesser of the two parameters (a) and (b).
- All data outputs will be at LOW level after reset goes high until data is entered into the FIFO.

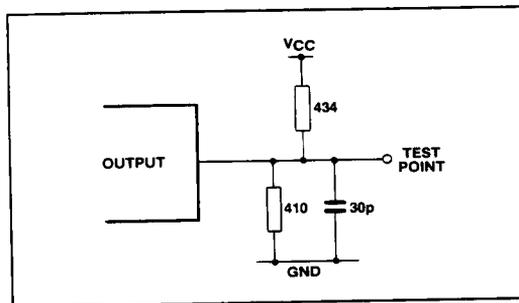


Fig.3 Test circuit

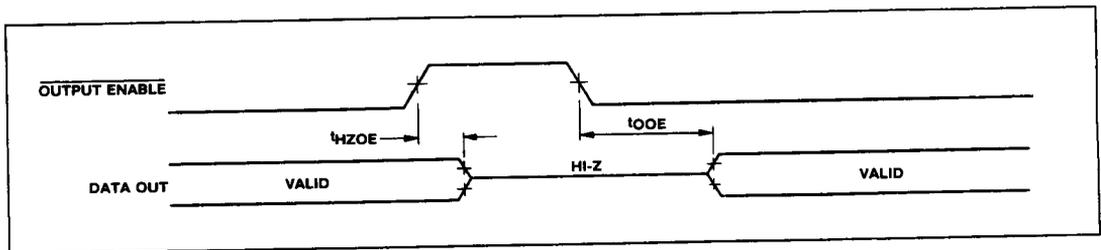


Fig.4 Output enable timing

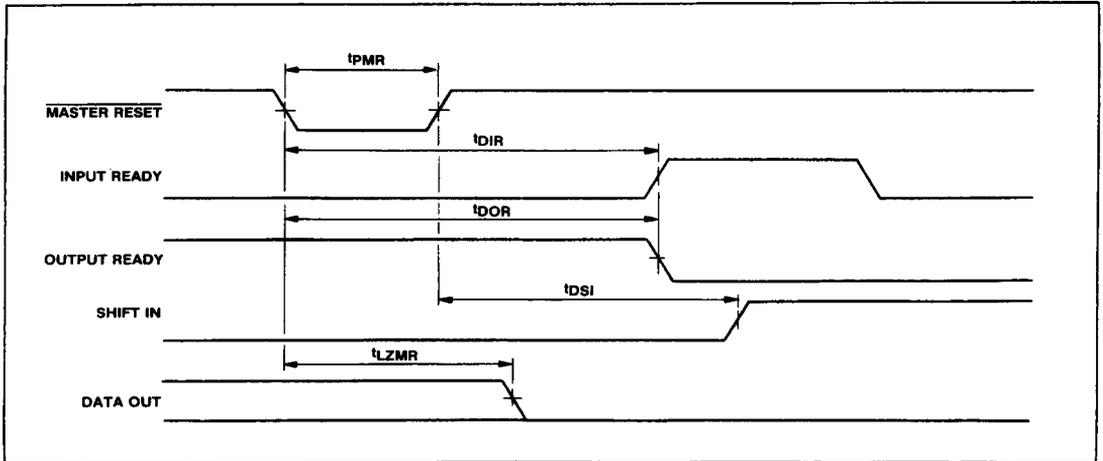


Fig.5 Master reset timing

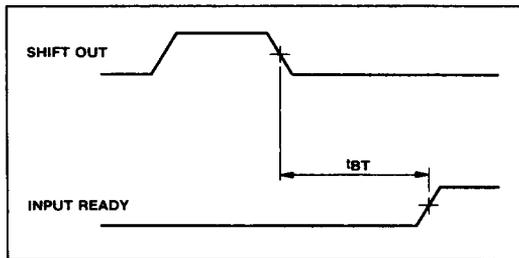


Fig.6 Bubble through time - device full

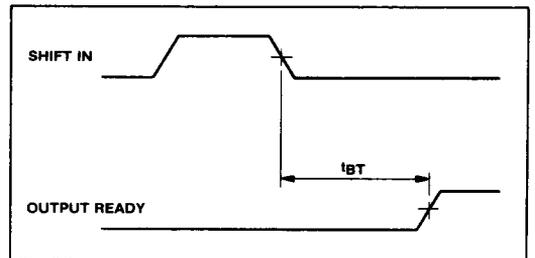


Fig.7 Fall through time - device empty

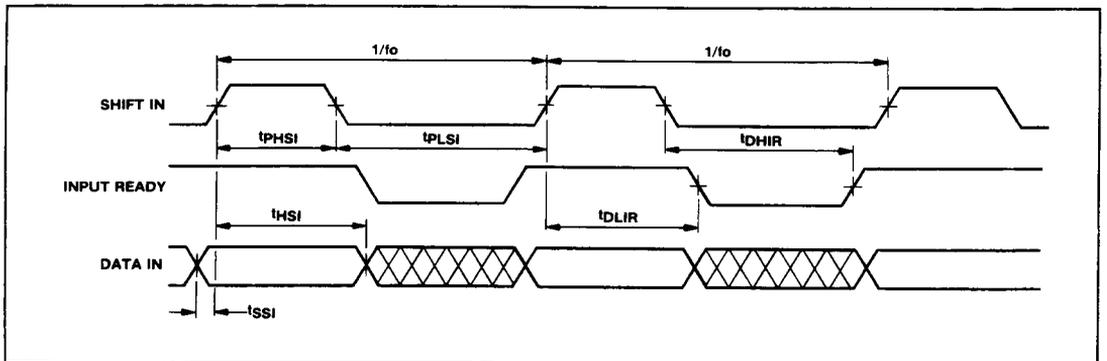


Fig.8 Switching waveforms - Data In timing

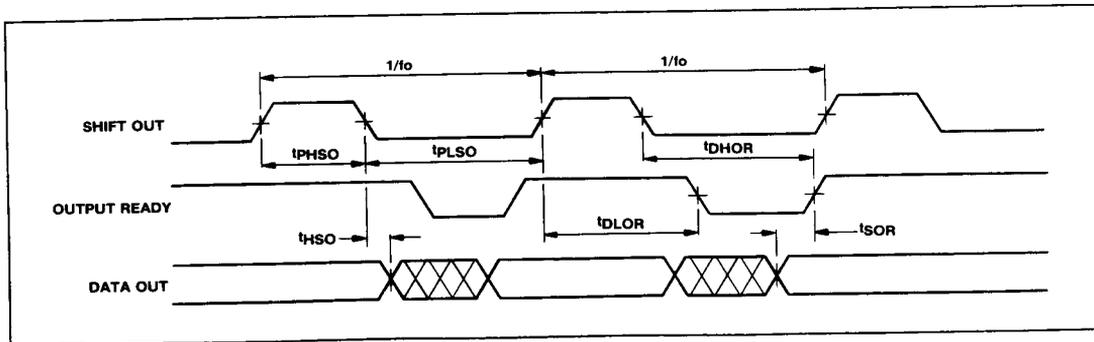


Fig.9 Switching waveforms - Data Out timing

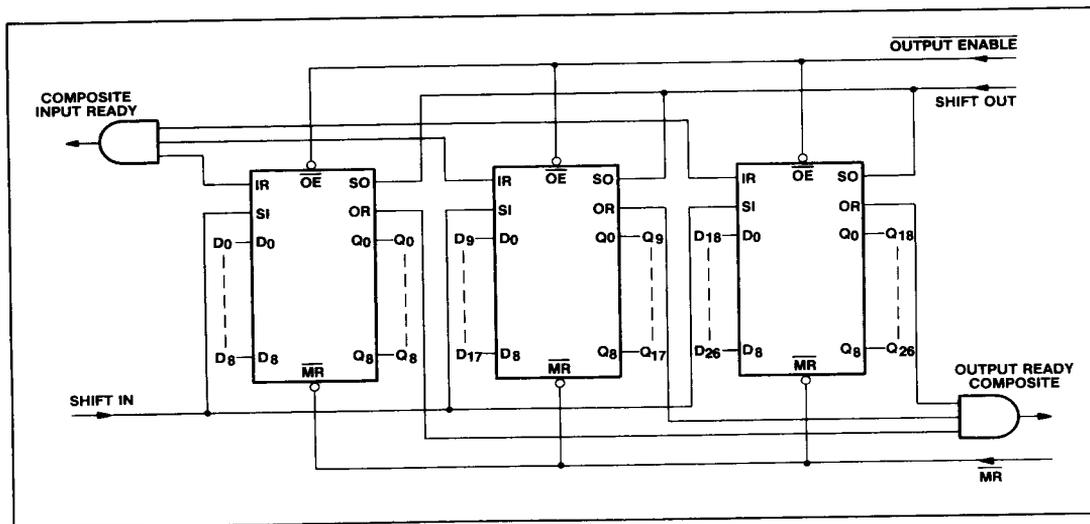


Fig.10 64 x 27 application

USER NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle and then go back LOW again. The stored word will remain on

- the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, the IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.

TYPICAL CHARACTERISTICS

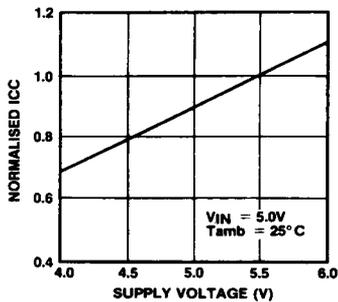


Fig.11 Normalised supply current vs. supply voltage

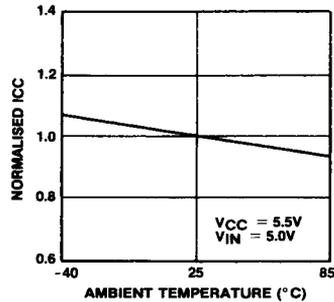


Fig.12 Normalised supply current vs. ambient temperature

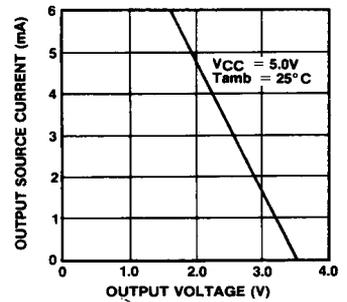


Fig.13 Output source current vs. output voltage

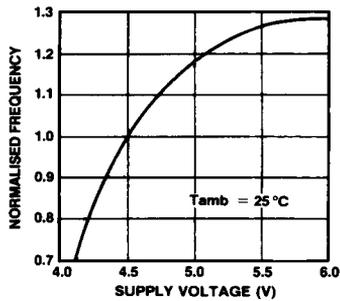


Fig.14 Normalised frequency vs. supply voltage

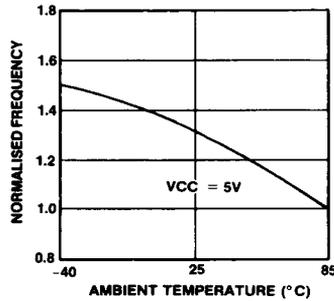


Fig.15 Normalised frequency vs. ambient temperature

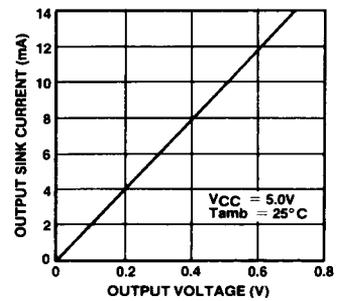


Fig.16 Output sink current vs. output voltage

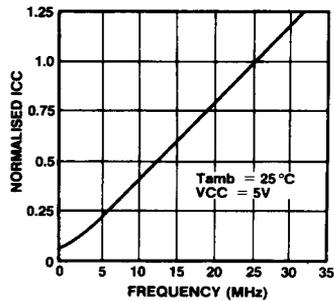


Fig.17 Normalised Icc vs. frequency

ORDERING INFORMATION

Industrial

- MV65030-25 B0 DG (Industrial - Ceramic DIL package)
- MV65030-35 B0 DG (Industrial - Ceramic DIL package)
- MV65030-25 B0 DP (Industrial - Plastic DIL package)
- MV65030-35 B0 DP (Industrial - Plastic DIL package)
- MV65030-25 B0 LC (Industrial - LCC package)
- MV65030-35 B0 LC (Industrial - LCC package)
- MV65030-25 B0 HP (Industrial - Quad package)
- MV65030-35 B0 HP (Industrial - Quad package)

Military

Call for availability on High Reliability parts and MIL 883C screening.

- MV65030 A0 DG (Military - Ceramic DIL package)
- MV65030 A0 LC (Military - LCC package)