

POWER MANAGEMENT

Features

- Input supply voltage range — 2.9V to 5.5V
- Very high efficiency charge pump driver system with three modes — 1x, 1.5x and 2x
- Six programmable current sinks — 0mA to 25mA
- Up to three LED grouping options
- Fade-in/fade-out feature for main LED bank
- Selectable charge pump frequency — 250kHz/1MHz
- SemPulse® single wire interface
- Backlight current accuracy — $\pm 1.5\%$ typical
- Backlight current matching — $\pm 0.5\%$ typical
- LED float detection
- Automatic sleep mode with all LEDs off
- Sleep mode quiescent current — 60 μ A typical
- Shutdown current — 0.1 μ A typical
- Ultra-thin package — 2 x 2 x 0.6 (mm)
- Lead-free and halogen-free
- WEEE and RoHS compliant

Applications

- Cellular phones, smart phones, and PDAs
- LCD modules
- Portable media players
- Digital cameras
- Personal navigation devices
- Display/keypad backlighting and LED indicators

Description

The SC662 is a high efficiency charge pump LED driver using Semtech's proprietary charge pump technology. Performance is optimized for use in single-cell Li-ion battery applications.

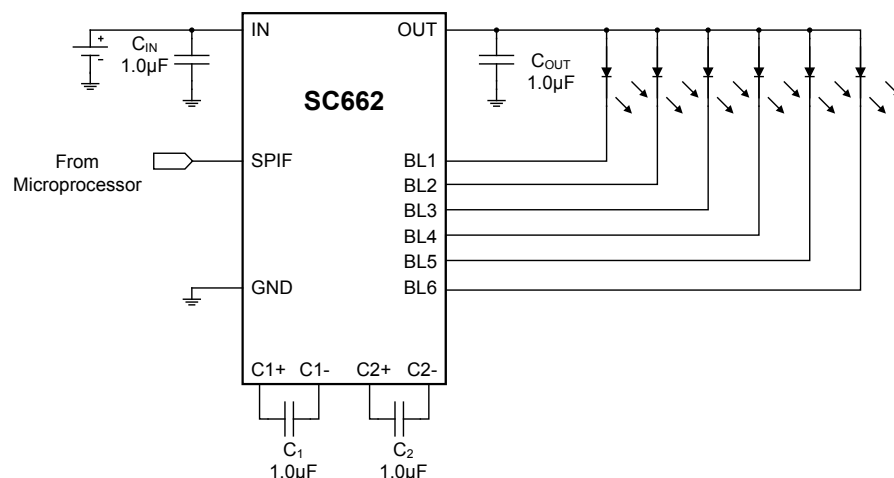
The charge pump provides backlight current utilizing six matched current sinks. The load and supply conditions determine whether the charge pump operates in 1x, 1.5x, or 2x mode. An optional fading feature that gradually adjusts the backlight current is provided to simplify control software.

The SC662 uses the proprietary SemPulse® single wire interface to control all functions of the device, including backlight currents. The single wire interface minimizes microcontroller and interface pin counts. The six LEDs can be grouped in up to three separate banks that can be independently controlled.

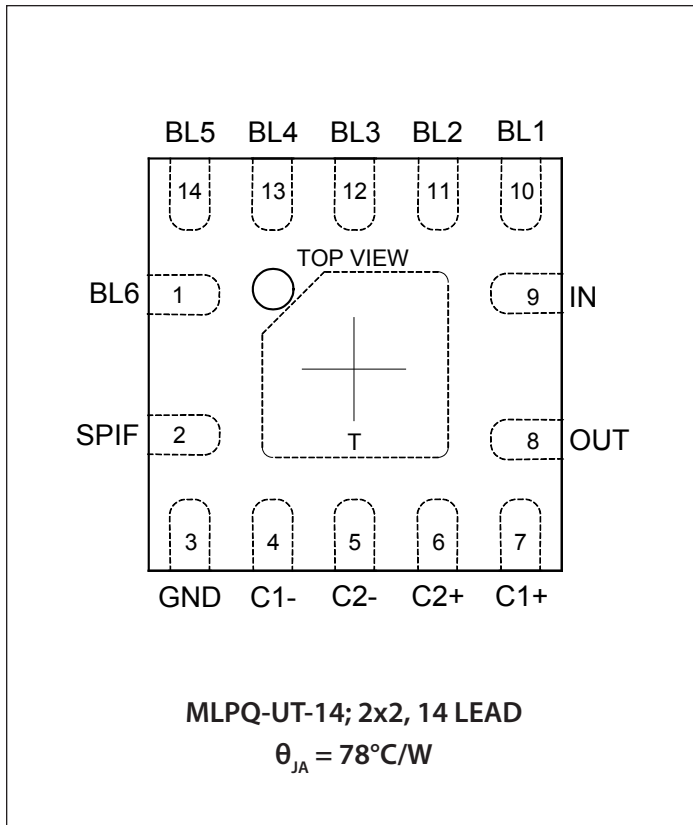
The charge pump switches at 1MHz or 250kHz, and the frequency is selectable using the SemPulse interface. Both 1MHz and 250kHz frequencies are supported by 0402 size (1005 metric) ceramic capacitors.

The SC662 enters sleep mode when all the LED drivers are disabled. In this mode, the quiescent current is reduced while the device continues to monitor the SemPulse interface.

Typical Application Circuit



Pin Configuration



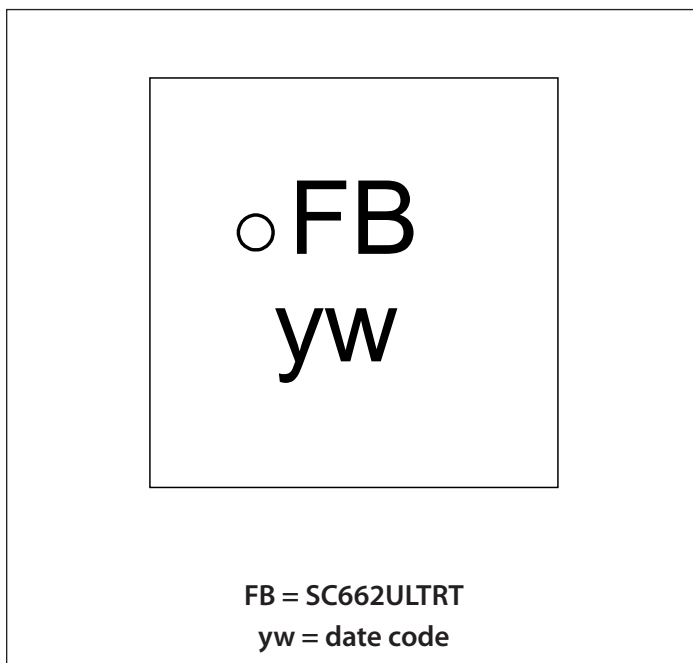
Ordering Information

Device	Package
SC662ULTRT ⁽¹⁾⁽²⁾	MLPQ-UT-14 2x2
SC662EVB	Evaluation Board

Notes:

- (1) Available in tape and reel only. A reel contains 3,000 devices.
- (2) Lead-free packaging only. Device is WEEE and RoHS compliant, and halogen-free.

Marking Information



Absolute Maximum Ratings

IN, OUT (V)	-0.3 to +6.0
C1+, C2+ (V)	-0.3 to (V _{OUT} +0.3)
Pin Voltage — All Other Pins (V)	-0.3 to (V _{IN} +0.3)
OUT Short Circuit Duration	Continuous
ESD Protection Level ⁽¹⁾ (kV)	4

Recommended Operating Conditions

Ambient Temperature Range (°C).....	-40 ≤ T _A ≤ +85
Input Voltage (V)	2.9 ≤ V _{IN} ≤ 5.5
Output Voltage (V)	2.5 ≤ V _{OUT} ≤ 5.25

Thermal Information

Thermal Resistance, Junction to Ambient ⁽²⁾ (°C/W) ..	78
Storage Temperature Range (°C).....	-65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C)	+260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:

- (1) Tested according to JEDEC standard JESD22-A114
- (2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB per JESD51 standards.

Electrical Characteristics

Unless otherwise noted, T_A = +25°C for Typ, -40°C to +85°C for Min and Max, T_{J(MAX)} = 125°C, V_{IN} = 3.7 V, C_{IN} = C₁ = C₂ = C_{OUT} = 1.0μF (ESR = 0.03Ω)⁽¹⁾

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Specifications						
Shutdown Current	I _{Q(OFF)}			0.1	2	μA
Total Quiescent Current	I _Q	All outputs disabled, SPIF = V _{IN} ⁽²⁾		60		μA
		1x mode, all LEDs on, I _{BLn} = 0.5mA		0.9		mA
		1x mode, all LEDs on, I _{BLn} = 25mA		1.5		
		1.5x or 2x charge pump mode, all LEDs on, I _{BLn} = 25mA		2		
Charge Pump Electrical Specifications						
Maximum Total Output Current	I _{OUT(MAX)}	V _{IN} > 2.9V, sum of all active LED currents, V _{OUT(MAX)} = 4.2V	150			mA
Backlight Current Setting	I _{BLn}	Nominal setting for BL1 thru BL6	0		25	mA
Backlight Current Matching	I _{BL-BL}	I _{BLn} = 12mA ⁽³⁾	-3.5	±0.5	+3.5	%
Backlight Current Accuracy	I _{BL-ACC}	I _{BLn} = 12mA		±1.5		%
Mode Transition (Falling) Input Voltage — 1x Mode to 1.5x Mode	V _{TRANS1x}	I _{OUT} = 72mA, I _{BLn} = 12mA, V _{OUT} = 3.22V		3.28		V
1.5x Mode to 1x Mode Hysteresis	V _{HYST1x}	I _{OUT} = 72mA, I _{BLn} = 12mA, V _{OUT} = 3.22V, f _{PUMP} = 250kHz		250		mV

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Charge Pump Electrical Specifications (continued)						
Mode Transition (Falling) Input Voltage — 1.5x Mode to 2x Mode	$V_{\text{TRANS1.5x}}$	$I_{\text{OUT}} = 72\text{mA}$, $I_{\text{BLn}} = 12\text{mA}$, $V_{\text{OUT}} = 4.2\text{V}^{(4)}$, $f_{\text{PUMP}} = 250\text{kHz}$		3.14		V
Current Sink Off-State Leakage Current	$I_{\text{BLn(off)}}$	$V_{\text{IN}} = V_{\text{BLn}} = 4.2\text{V}$		0.1	1	μA
Charge Pump Frequency	f_{PUMP}	Bit FSEL = 0		250		kHz
		Bit FSEL = 1		1		MHz
Fault Protection Specifications						
Output Short Circuit Current Limit	$I_{\text{OUT(SC)}}$	OUT pin shorted to GND		125		mA
		$V_{\text{OUT}} > 2.5\text{V}$		300		
Under Voltage Lockout	$V_{\text{UVLO-OFF}}$	Increasing V_{IN}		2.3		V
	$V_{\text{UVLO-HYS}}$	Hysteresis		75		mV
Over-Voltage Protection	V_{OVP}	OUT pin open circuit, $V_{\text{OUT}} = V_{\text{OVP}}$ rising threshold		5.7	6.0	V
Over-Temperature Threshold	T_{OT}	Rising temperature		165		$^{\circ}\text{C}$
	$T_{\text{OT-HYS}}$	Hysteresis		20		$^{\circ}\text{C}$

Electrical Characteristics (continued)

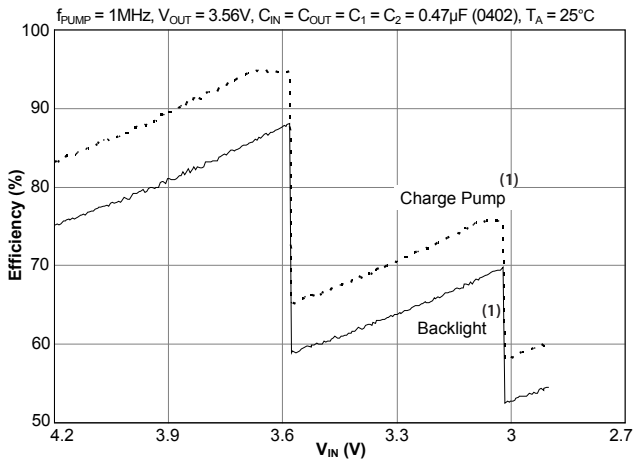
Parameter	Symbol	Conditions	Min	Typ	Max	Units
SemPulse Interface						
Input High Threshold	V_{IH}	$V_{IN} = 5.5V$	1.4			V
Input Low Threshold	V_{IL}	$V_{IN} = 2.9V$			0.4	V
Input High Current	I_{IH}	$V_{IN} = 5.5V$	-1		+1	μA
Input Low Current	I_{IL}	$V_{IN} = 5.5V$	-1		+1	μA
Start up Time ⁽⁵⁾	t_{SU}	Only required when leaving shutdown mode	1			ms
Bit Pulse Duration ⁽⁶⁾	t_{HI}		0.75		250	μs
Duration Between Pulses ⁽⁶⁾	t_{LO}		0.75		250	μs
Hold Time - Address ⁽⁶⁾	t_{HOLDA}		550		5000	μs
Hold Time - Data ⁽⁶⁾	t_{HOLDD}		550			μs
Bus Reset Time ⁽⁶⁾	t_{BR}		10			ms
Shutdown Time ⁽⁷⁾	t_{SD}		10			ms

Notes:

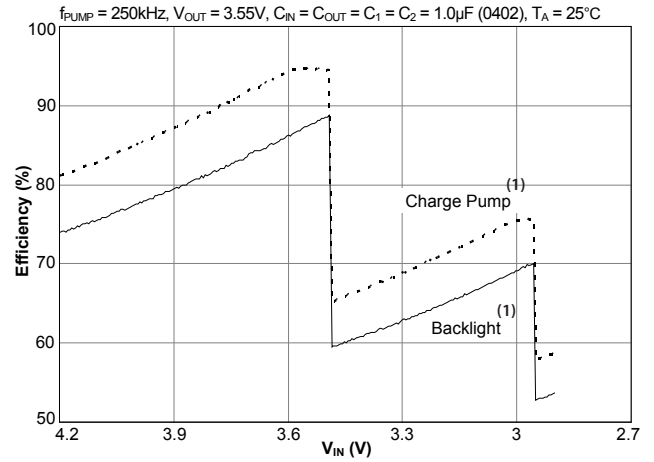
- (1) Capacitors are MLCC of X5R type.
- (2) SPIF is high for more than 10ms to place the serial bus in standby mode.
- (3) Current matching is defined as $\pm [I_{BL(MAX)} - I_{BL(MIN)}] / [I_{BL(MAX)} + I_{BL(MIN)}]$.
- (4) Test voltage is $V_{OUT} = 4.2V$ — a relatively extreme LED voltage — to force a transition during test. Typically $V_F = 3.2V$ for white LEDs.
- (5) The SemPulse start-up time is the minimum time that the SPIF pin must be held high to enable the part before starting communication.
- (6) The source driver used to provide the SemPulse output must meet these limits.
- (7) The SemPulse shutdown time is the minimum time that the SPIF pin must be pulled low to shut the part down.

Typical Characteristics

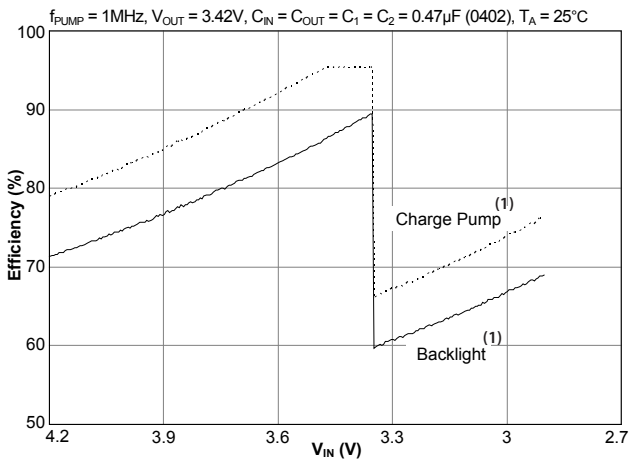
Charge Pump Efficiency (6 LEDs) — 25mA Each



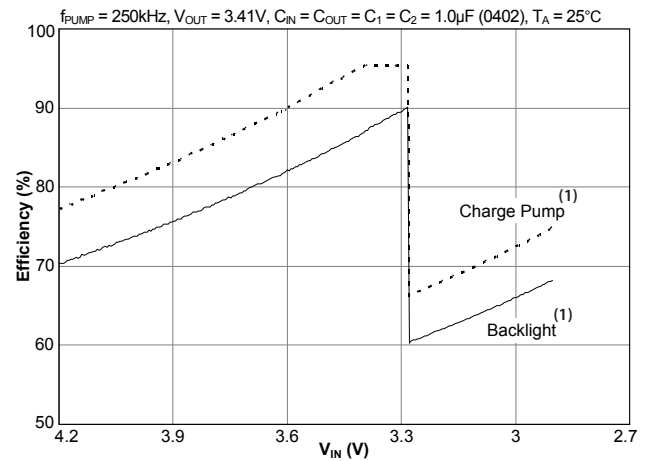
Charge Pump Efficiency (6 LEDs) — 25mA Each



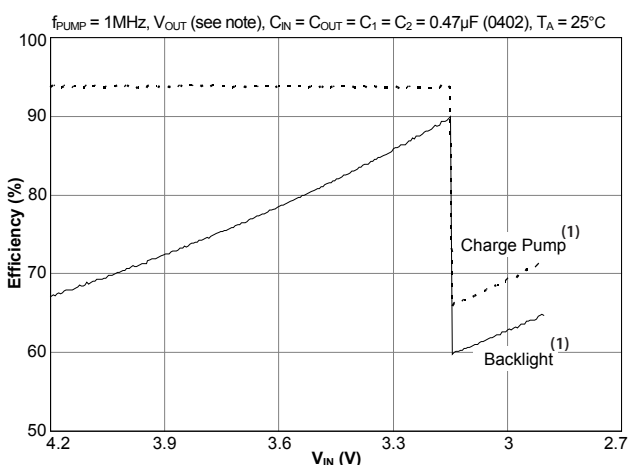
Charge Pump Efficiency (6 LEDs) — 12mA Each



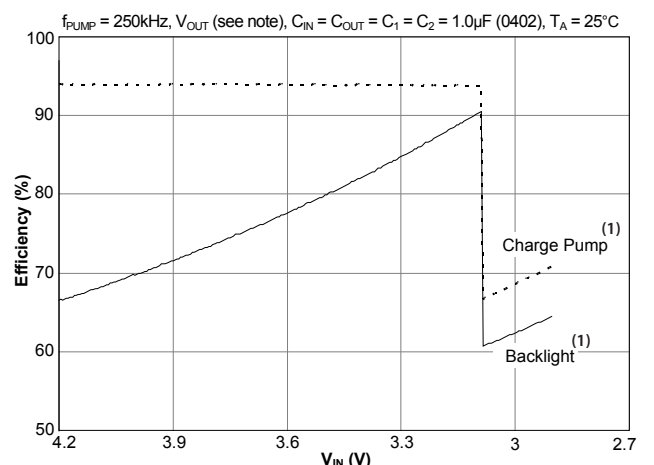
Charge Pump Efficiency (6 LEDs) — 12mA Each



Charge Pump Efficiency (6 LEDs) — 5mA Each ⁽²⁾



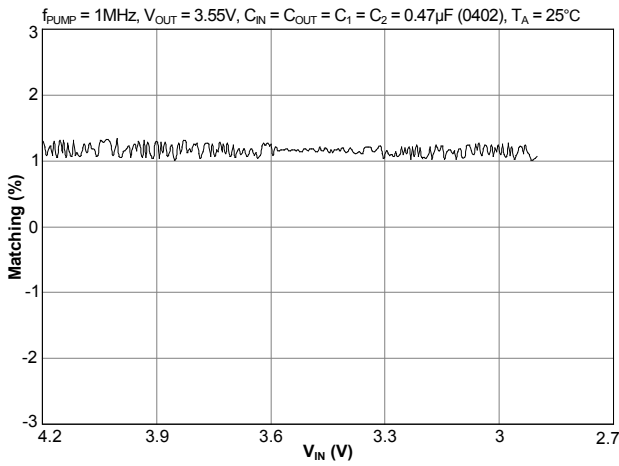
Charge Pump Efficiency (6 LEDs) — 5mA Each ⁽²⁾



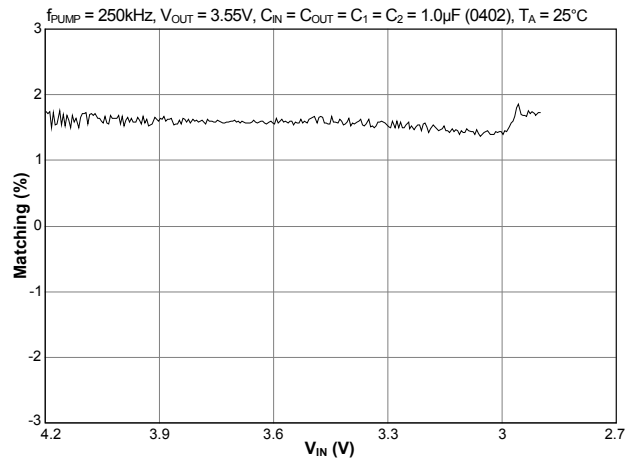
Notes: (1) Efficiency labels "Charge Pump" and "Backlight" are defined on page 13 under the sub-heading Charge Pump Efficiency.
 (2) Plots shown for 5mA data have $V_{OUT} = 3.27\text{V}$ when in 1.5X and 2X modes, and $V_{OUT} = V_{IN} - 55\text{mV}$ when in 1X mode. V_{OUT} is connected internally to V_{IN} only when the charge pump is in 1X mode and $I_{BL} \leq 5\text{mA}$.

Typical Characteristics (continued)

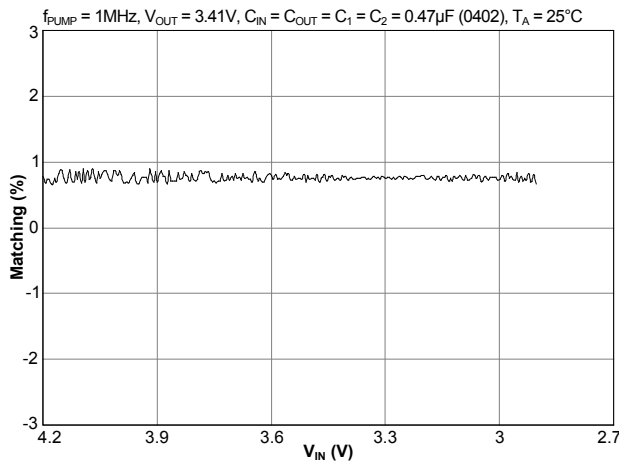
Backlight Matching (6 LEDs) — 25mA Each



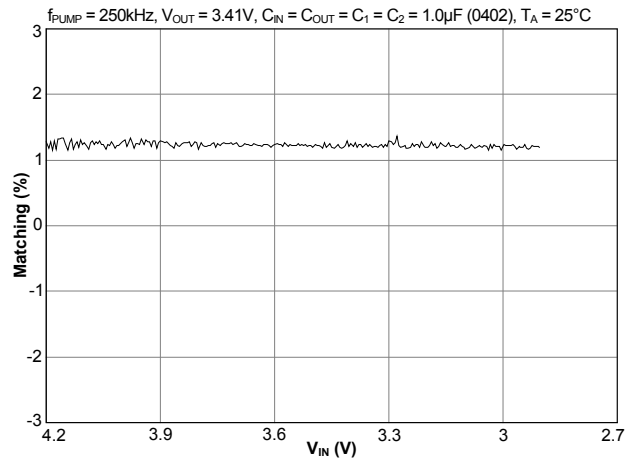
Backlight Matching (6 LEDs) — 25mA Each



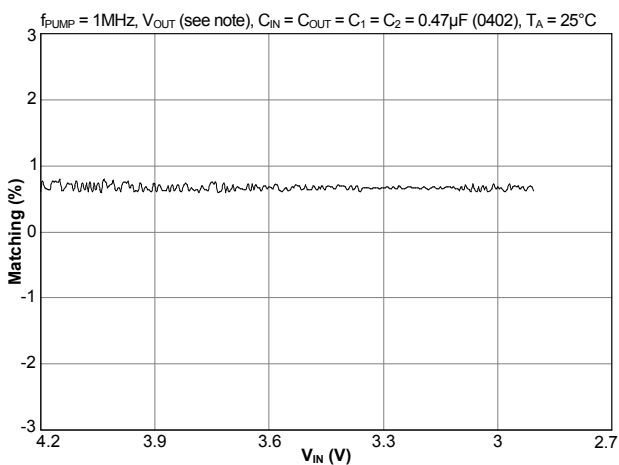
Backlight Matching (6 LEDs) — 12mA Each



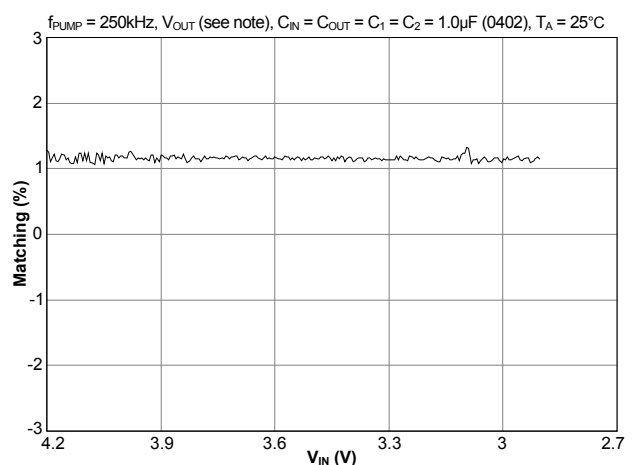
Backlight Matching (6 LEDs) — 12mA Each



Backlight Matching (6 LEDs) — 5mA Each ⁽²⁾



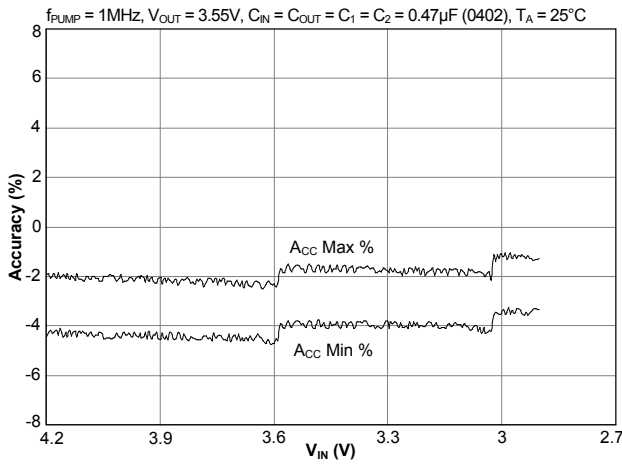
Backlight Matching (6 LEDs) — 5mA Each ⁽²⁾



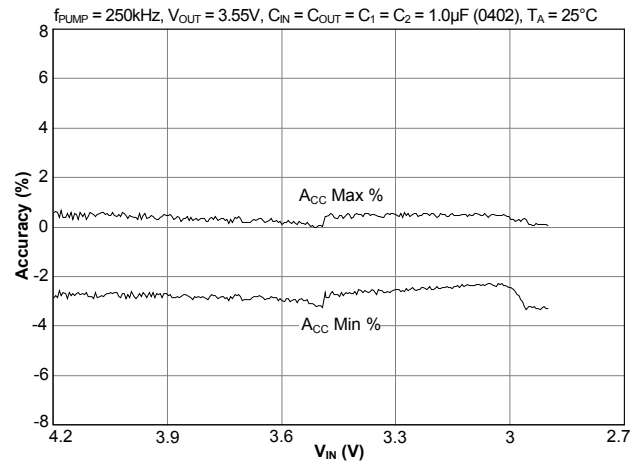
Notes: (1) Efficiency labels “Charge Pump” and “Backlight” are defined on page 13 under the sub-heading Charge Pump Efficiency.
 (2) Plots shown for 5mA data have — $V_{OUT} = 3.27\text{V}$ when in 1.5X and 2X modes, and $V_{OUT} = V_{IN} - 55\text{mV}$ when in 1X mode. V_{OUT} is connected internally to V_{IN} only when the charge pump is in 1X mode and $I_{BL} \leq 5\text{mA}$.

Typical Characteristics (continued)

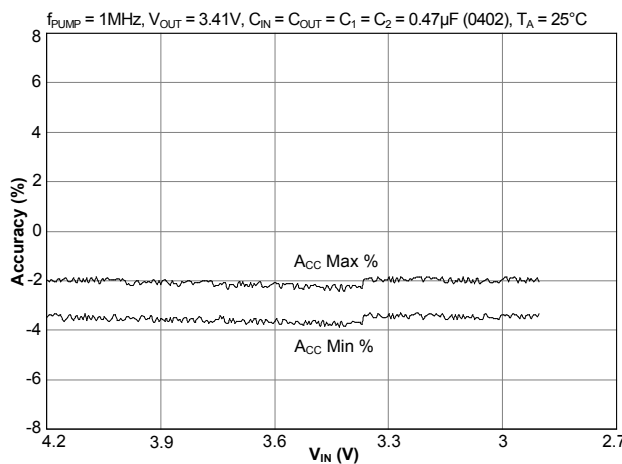
Backlight Accuracy (6 LEDs) — 25mA Each



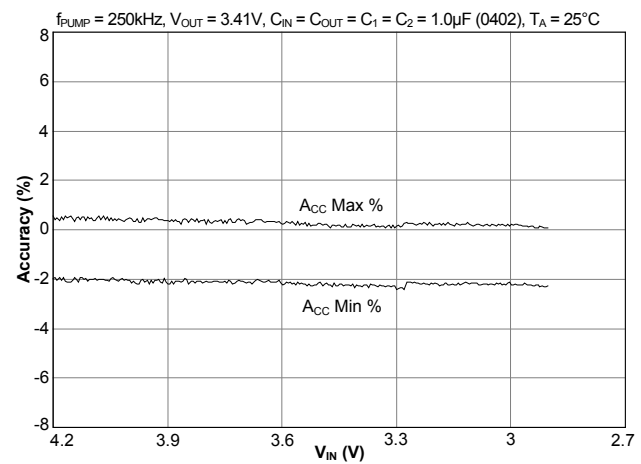
Backlight Accuracy (6 LEDs) — 25mA Each



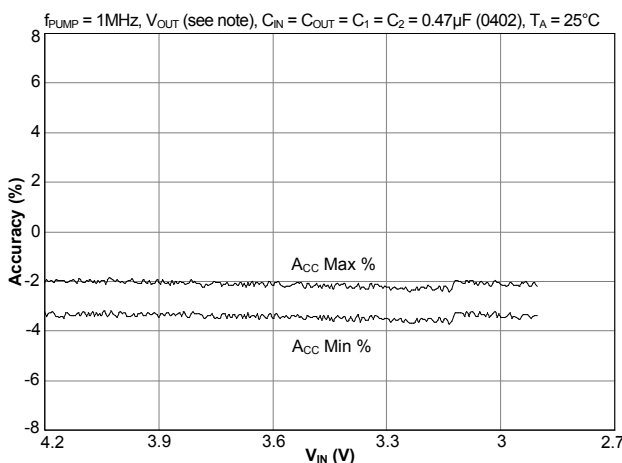
Backlight Accuracy (6 LEDs) — 12mA Each



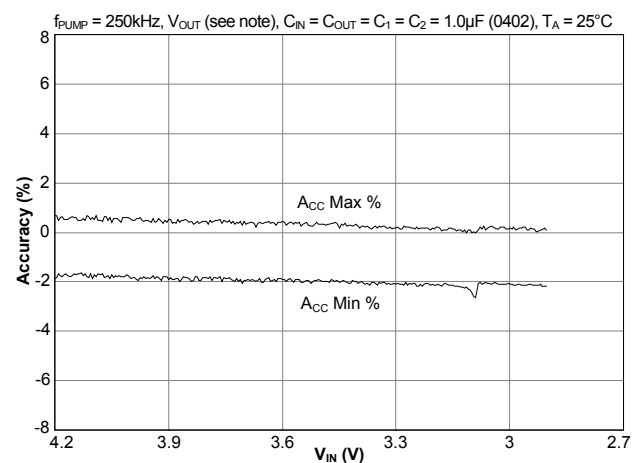
Backlight Accuracy (6 LEDs) — 12mA Each



Backlight Accuracy (6 LEDs) — 5mA Each ⁽²⁾



Backlight Accuracy (6 LEDs) — 5mA Each ⁽²⁾

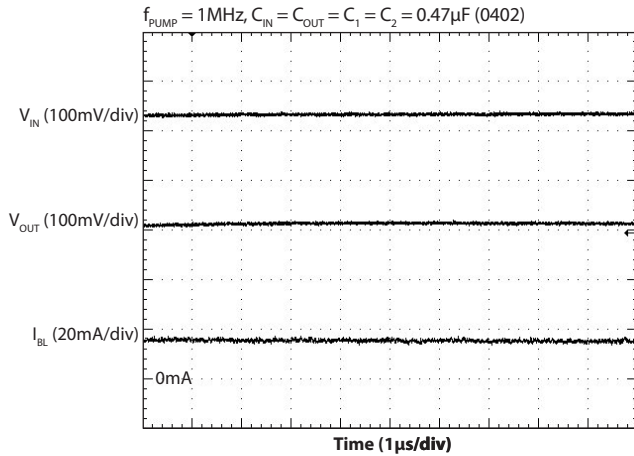


Notes: (1) Efficiency labels “Charge Pump” and “Backlight” are defined on page 13 under the sub-heading Charge Pump Efficiency.
 (2) Plots shown for 5mA data have — $V_{OUT} = 3.27\text{V}$ when in 1.5X and 2X modes, and $V_{OUT} = V_{IN} - 55\text{mV}$ when in 1X mode. V_{OUT} is connected internally to V_{IN} only when the charge pump is in 1X mode and $I_{BL} \leq 5\text{mA}$.

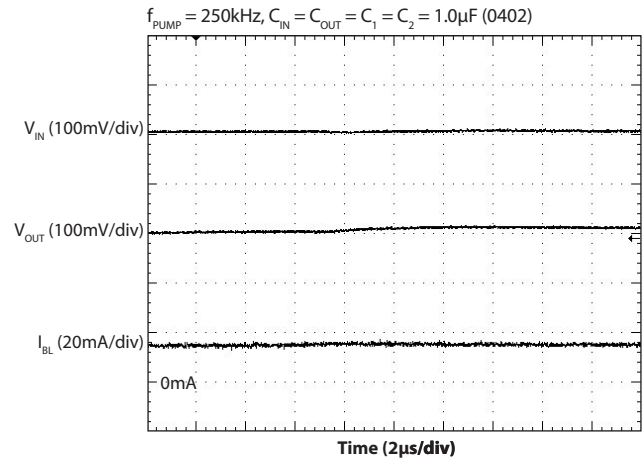
Typical Characteristics (continued)

All data taken with $T_A = 25^\circ\text{C}$, 6 LEDs @ 15mA each unless otherwise noted.

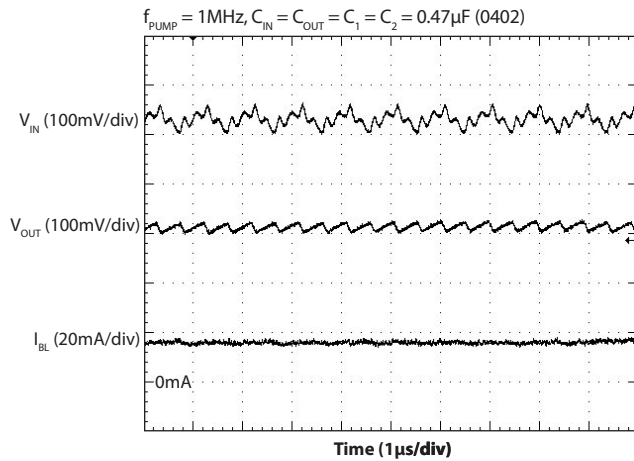
Ripple — 1x Mode



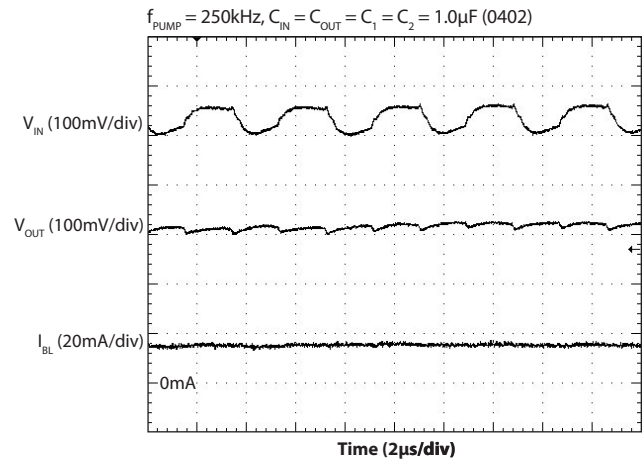
Ripple — 1x Mode



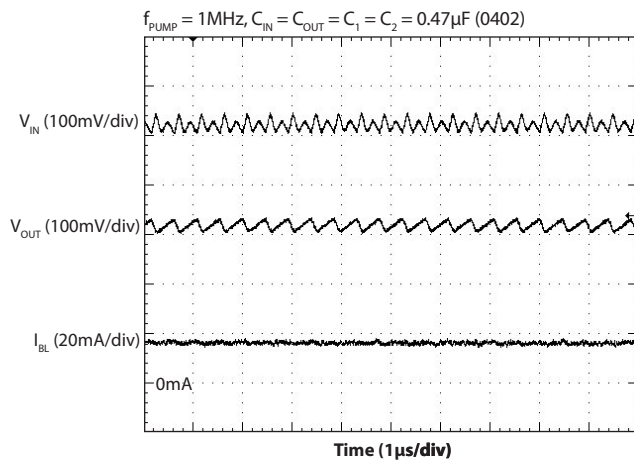
Ripple — 1.5x Mode



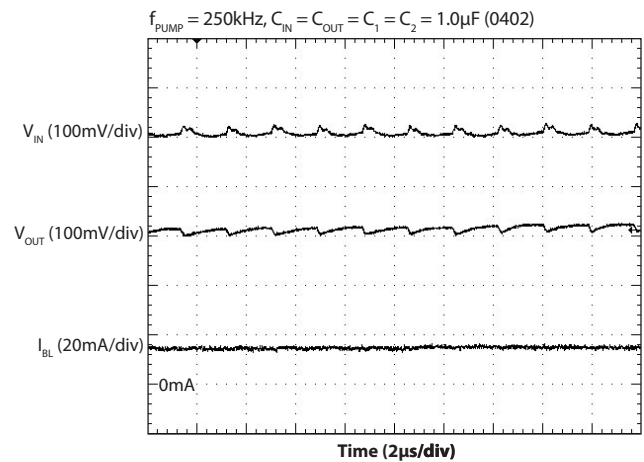
Ripple — 1.5x Mode



Ripple — 2x Mode



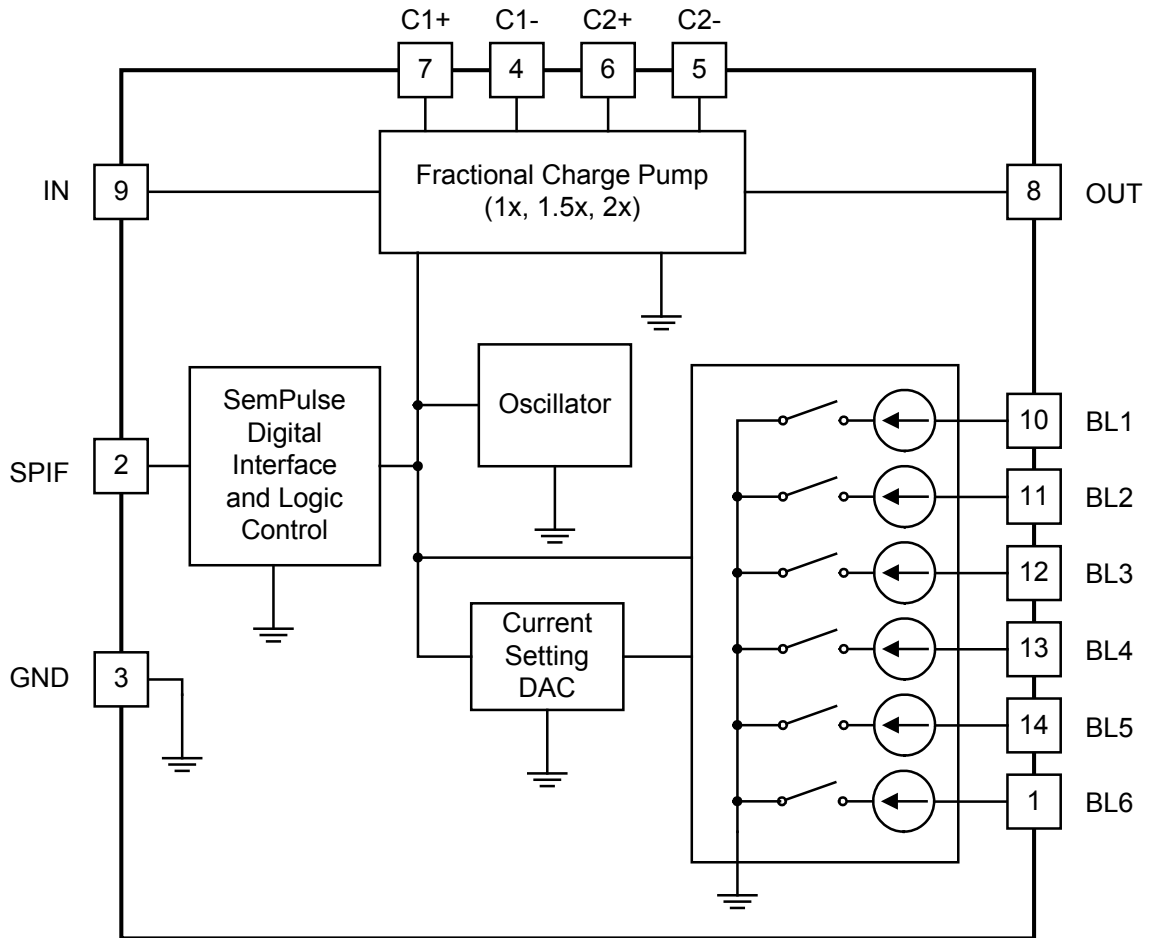
Ripple — 2x Mode



Pin Descriptions

Pin #	Pin Name	Pin Function
1	BL6	Current sink output for backlight LED 6 — leave this pin open if unused
2	SPIF	SemPulse single wire interface pin — used to enable/disable the device and to configure all registers (refer to Register Map and SemPulse Interface sections)
3	GND	Ground pin
4	C1-	Negative connection to bucket capacitor C ₁
5	C2-	Negative connection to bucket capacitor C ₂
6	C2+	Positive connection to bucket capacitor C ₂
7	C1+	Positive connection to bucket capacitor C ₁
8	OUT	Charge pump output — all LED anode pins should be connected to this pin
9	IN	Battery voltage input
10	BL1	Current sink output for backlight LED 1 — leave this pin open if unused
11	BL2	Current sink output for backlight LED 2 — leave this pin open if unused
12	BL3	Current sink output for backlight LED 3 — leave this pin open if unused
13	BL4	Current sink output for backlight LED 4 — leave this pin open if unused
14	BL5	Current sink output for backlight LED 5 — leave this pin open if unused
T	THERMAL PAD	Thermal pad for heatsinking purposes — connect to ground plane using multiple vias — not connected internally

Block Diagram



Applications Information

General Description

This design is optimized for handheld applications supplied from a single Li-ion cell and includes the following key features:

- A high efficiency fractional charge pump that supplies power to all LEDs.
- Six matched current sinks that control LED backlighting current, providing 0mA to 25mA per LED.
- Up to three independently controlled LED banks.
- Selectable charge pump frequency — 250kHz or 1MHz options.

High Current Fractional Charge Pump

The backlight outputs are supported by a high efficiency, high current fractional charge pump output. The charge pump multiplies the input voltage by 1x, 1.5x, or 2x. The output of the charge pump is delivered to the LED anodes. The charge pump switches only in 1.5x and 2x modes and is disabled in 1x mode to save power and improve efficiency.

The charge pump switches at a fixed frequency of either 250kHz or 1MHz. The charge pump switching frequency is set via the SemPulse interface by the FSEL bit. The 250kHz setting is selected by setting FSEL = 0, while the 1MHz setting is selected when FSEL = 1.

The mode selection circuit automatically selects one of the following modes; 1x, 1.5x, or 2x based on circuit conditions such as LED voltage, input voltage, and load current. The 1x mode is the most efficient of the three modes, followed by 1.5x and 2x modes. Circuit conditions such as low input voltage, high output current, or high LED voltage place a higher demand on the charge pump output. A higher numerical mode (1.5x or 2x) may be needed momentarily to maintain regulation at the OUT pin during intervals of high demand. The charge pump responds to momentary high demands, setting the charge pump to the optimum mode to deliver the output voltage and load current while optimizing efficiency. Hysteresis is provided to prevent mode toggling.

The charge pump requires two bucket capacitors. One capacitor must be connected between the C1+ and C1- pins and the other must be connected between the C2+ and C2- pins as shown in the Typical Application Circuit diagram. Bucket capacitors should be equal in value to support current sharing between C_1 and C_2 .

C_{OUT} , C_{IN} , C_1 , and C_2 capacitors with X7R or X5R ceramic dielectric are strongly recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

LED Backlight Current Sinks

The backlight current is set via the SemPulse interface. The current is regulated to one of 32 values between 0mA and 25mA. The step size varies depending upon the current setting. The lowest settings are 0, 50, 100, and 200 μ A. From 0.5mA to 5mA, the step size is 0.5mA. The step size increases to 1mA for settings between 5mA and 21mA. Steps are 2mA between 21mA and 25mA. The variation in step size allows finer adjustment for dimming functions in the low current setting range and coarse adjustment at higher current settings where small current changes are not visibly noticeable in LED brightness. A zero setting is also included to allow the current sink to be disabled by writing to either the enable bit or the current setting register for maximum flexibility.

All backlight current sinks have matched currents. When there is a variation in the forward voltages (ΔV_F) of the LEDs, mis-matched LED voltages do not degrade the accuracy of the backlight currents. The voltages of all BLn pins are compared, and the lowest of these voltages is used as feedback for setting the voltage regulation at the OUT pin. This is done to ensure that sufficient bias exists for all LEDs.

The backlight LEDs default to the off state upon power-up. For backlight applications using less than six LEDs, any unused output must be left open and the unused LED must remain disabled. When writing to the backlight enable register, a zero (0) must be written to the corresponding bit of any unused output. Detailed information about programming of the registers is provided in later sections, beginning at SemPulse Interface on page 21.

Applications Information (continued)

Charge Pump Efficiency

Efficiency of the charge pump is defined as

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

The input current is equal to the output current multiplied by the charge pump mode plus the quiescent current $I_{IN} = I_{OUT} \times \text{Mode} + I_{Q'}$ and the output current is equal to the sum of all backlight currents.

$$I_{OUT} = \sum_{n=1}^6 I_{BLn} \times \text{Mode}$$

V_{OUT} , I_{OUT} , V_{IN} , I_{IN} , $I_{Q'}$ and I_{BLn} are terms from the electrical characteristics section. "Mode" is the active boost ratio of the charge pump, equal to 1, 1.5, or 2. Efficiency plots in the Typical Characteristics section provide charge pump efficiency data labeled with "Charge Pump".

Efficiency of the power conversion to the LEDs is defined as

$$\eta = \frac{\sum_{n=1}^6 (V_{Fn} \times I_{BLn})}{V_{IN} \times I_{IN}}$$

V_{F1} through V_{F6} are the forward voltages of the LEDs. I_{BL1} through I_{BL6} are the regulated backlight sink currents flowing in the LEDs. Efficiency plots in the Typical Characteristics section provide LED backlight efficiency data labeled with "Backlight".

Backlight Quiescent Current

The quiescent current required to operate all backlights is reduced when each backlight current is set to 5.0mA or less. This low-current mode feature results in improved efficiency under light-load conditions, saving approximately 350µA of bias current. Low-current mode disables and bypasses the internal LDO when the charge pump is in 1x mode, connecting the LED anodes to the supply at V_{IN} . Further reduction in quiescent current will result from using fewer than the maximum number of LEDs.

LED Banks

The LEDs can be grouped in up to three independently controlled LED banks. Using the SemPulse interface, the six LED drivers can be grouped as described in the Backlight Grouping Configuration subsection. The banks can be used to provide up to three different current options. This can be useful for controlling keypad, display, and auxiliary backlight operation from one SC662 device.

The LED banks provide versatility by allowing backlights to be controlled independently. For example, applications that have a main and sub display may also need to supply an indicator LED. The three bank option allows the SC662 to control each function with different current settings. Another application involves backlighting two displays and a keypad, each requiring different brightness settings. A third scenario requires supplying different brightness levels to different types of LEDs (such as RGB) to create display effects. In all applications, the brightness level for each LED can be set independently.

Backlight Fade-in / Fade-out Function

The SC662 contains register bits that control the fade state of the main bank. When enabled, the fade function causes the main backlights to change brightness by stepping the current incrementally until the target backlight current is reached. Fade begins immediately after the target backlight current is stored in its register. Fade may be enabled for the main bank only. Sub and third banks do not fade.

In addition to the 32 programmable backlight current values, there are also 75 non-programmable current steps. The non-programmable steps are active only during a fade operation to provide for a very smooth change in backlight brightness. Backlight current steps proceed at a programmable fade rate of 2, 4, or 6ms. The exact length of time used to fade between any two backlight values is determined by multiplying the fade rate by the number of steps between the old and new backlight values. The fade time can be calculated from the data provided in Table 1 on page 15.

Figures 2 through 6 on page 16 provide additional information about the fade process. Each figure represents one linear segment of the overall fade range shown in

Applications Information (continued)

Figure 7. The overall fade range is a piece-wise linear, logarithmic type of function which provides for a very smooth visual fading effect.

The fade rate may be changed dynamically when a fade operation is active by writing new values to the fade register. When a new backlight level is written during an ongoing fade operation, the fade will be redirected to the new value from the present state. An ongoing fade operation may be cancelled by disabling fade, which will result in the backlight current changing immediately to the final value. If fade is disabled, the current level will change immediately without the fade delay.

The terms BLEN and FADE are used for bits which are defined in a later section of the datasheet. The reader may choose to skip ahead to the Register Map and Register and Bit Definitions sections for a better understanding of these terms before continuing with this section’s explanation of the fade function and fade state diagram.

Fade State Diagram

If the main BLEN bits are disabled during an ongoing fade, the main bank will turn off immediately. When the main BLEN bits are re-enabled and FADE = 1, the main backlight currents will begin at 0mA and fade to the target value. If the main BLEN bits are re-enabled and FADE = 0, the main backlights will proceed immediately to the target value.

The state diagram in Figure 1 describes the fade operation. More details can be found in the Register Map section.

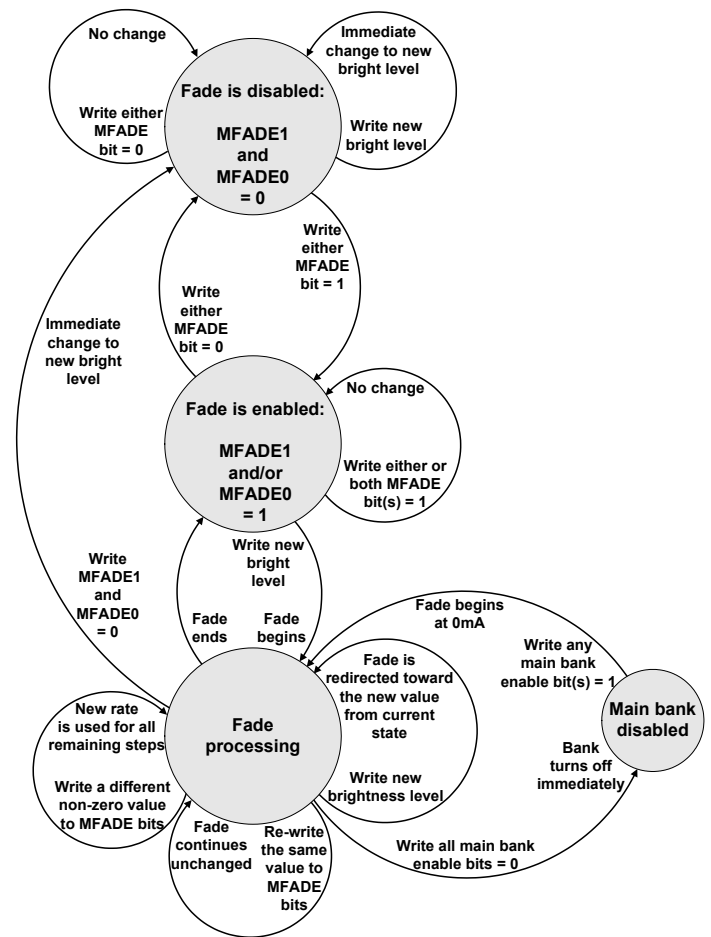


Figure 1 — Fade Function State Diagram

Shutdown Mode

The device is disabled when the SPIF pin is held low for the shutdown time specified in the electrical characteristics section. All registers are reset to default condition at shutdown.



Applications Information (continued)

Table 1 — Number of Backlight Fade Steps between Values (See Note)

Starting Value (mA)	25.0	106	105	104	102	96	90	88	84	80	76	72	68	64	60	52	47	42	38	34	30	26	24	22	20	18	16	14	12	10	8	4	0
	23.0	102	101	100	98	92	86	84	80	76	72	68	64	60	56	48	43	38	34	30	26	22	20	18	16	14	12	10	8	6	4	0	4
	21.0	98	97	96	94	88	82	80	76	72	68	64	60	56	52	44	39	34	30	26	22	18	16	14	12	10	8	6	4	2	0	4	8
	20.0	96	95	94	92	86	80	78	74	70	66	62	58	54	50	42	37	32	28	24	20	16	14	12	10	8	6	4	2	0	2	6	10
	19.0	94	93	92	90	84	78	76	72	68	64	60	56	52	48	40	35	30	26	22	18	14	12	10	8	6	4	2	0	2	4	8	12
	18.0	92	91	90	88	82	76	74	70	66	62	58	54	50	46	38	33	28	24	20	16	12	10	8	6	4	2	0	2	4	6	10	14
	17.0	90	89	88	86	80	74	72	68	64	60	56	52	48	44	36	31	26	22	18	14	10	8	6	4	2	0	2	4	6	8	12	16
	16.0	88	87	86	84	78	72	70	66	62	58	54	50	46	42	34	29	24	20	16	12	8	6	4	2	0	2	4	6	8	10	14	18
	15.0	86	85	84	82	76	70	68	64	60	56	52	48	44	40	32	27	22	18	14	10	6	4	2	0	2	4	6	8	10	12	16	20
	14.0	84	83	82	80	74	68	66	62	58	54	50	46	42	38	30	25	20	16	12	8	4	2	0	2	4	6	8	10	12	14	18	22
	13.0	82	81	80	78	72	66	64	60	56	52	48	44	40	36	28	23	18	14	10	6	2	0	2	4	6	8	10	12	14	16	20	24
	12.0	80	79	78	76	70	64	62	58	54	50	46	42	38	34	26	21	16	12	8	4	0	2	4	6	8	10	12	14	16	18	22	26
	11.0	76	75	74	72	66	62	58	54	50	46	42	38	34	30	22	17	12	8	4	0	4	6	8	10	12	14	16	18	20	22	26	30
	10.0	72	71	70	68	62	58	54	50	46	42	38	34	30	26	18	13	8	4	0	4	8	10	12	14	16	18	20	22	24	26	30	34
	9.0	68	67	66	64	58	54	50	46	42	38	34	30	26	22	14	9	4	0	4	8	12	14	16	18	20	22	24	26	28	30	34	38
	8.0	64	63	62	60	54	50	46	42	38	34	30	26	22	18	10	5	0	4	8	12	16	18	20	22	24	26	28	30	32	34	38	42
	7.0	59	58	57	55	49	45	41	37	33	29	25	21	17	13	5	0	5	9	13	17	21	23	25	27	29	31	33	35	37	39	43	47
	6.0	54	53	52	50	44	40	36	32	28	24	20	16	12	8	0	5	10	14	18	22	26	28	30	32	34	36	38	40	42	44	48	52
	5.0	46	45	44	42	36	32	28	24	20	16	12	8	4	0	8	13	18	22	26	30	34	36	38	40	42	44	46	48	50	52	56	60
	4.5	42	41	40	38	32	28	24	20	16	12	8	4	0	4	12	17	22	26	30	34	38	40	42	44	46	48	50	52	54	56	60	64
	4.0	38	37	36	34	28	24	20	16	12	8	4	0	4	8	16	21	26	30	34	38	42	44	46	48	50	52	54	56	58	60	64	68
	3.5	34	33	32	30	24	20	16	12	8	4	0	4	8	12	20	25	30	34	38	42	46	48	50	52	54	56	58	60	62	64	68	72
	3.0	30	29	28	26	20	16	12	8	4	0	4	8	12	16	24	29	34	38	42	46	50	52	54	56	58	60	62	64	66	68	72	76
	2.5	26	25	24	22	16	12	8	4	0	4	8	12	16	20	28	33	38	42	46	50	54	56	58	60	62	64	66	68	70	72	76	80
	2.0	22	21	20	18	12	8	4	0	4	8	12	16	20	24	32	37	42	46	50	54	58	60	62	64	66	68	70	72	74	76	80	84
1.5	18	17	16	14	8	4	0	4	8	12	16	20	24	28	36	41	46	50	54	58	62	64	66	68	70	72	74	76	78	80	84	88	
1.0	14	13	12	10	4	0	4	8	12	16	20	24	28	32	40	45	50	54	58	62	64	66	68	70	72	74	76	78	80	82	86	90	
0.5	10	9	8	6	0	4	8	12	16	20	24	28	32	36	44	49	54	58	62	66	70	72	74	76	78	80	82	84	86	88	92	96	
0.2	4	3	2	0	6	10	14	18	22	26	30	34	38	42	50	55	60	64	68	72	76	78	80	82	84	86	88	90	92	94	98	102	
0.1	2	1	0	2	8	12	16	20	24	28	32	36	40	44	52	57	62	66	70	74	78	80	82	84	86	88	90	92	94	96	100	104	
0.05	1	0	1	3	9	13	17	21	25	29	33	37	41	45	53	58	63	67	71	75	79	81	83	85	87	89	91	93	95	97	101	105	
0.0	0	1	2	4	10	14	18	22	26	30	34	38	42	46	54	59	64	68	72	76	80	82	84	86	88	90	92	94	96	98	102	106	
	0.0	0.05	0.1	0.2	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	6.0	7.0	8.0	9.0	10.0	11.0	12.0	13.0	14.0	15.0	16.0	17.0	18.0	19.0	20.0	21.0	23.0	25.0	

Ending Value (mA)

NOTE: The fade time is determined by multiplying the number of steps by the fade rate (fade steps × fade rate = fade time).

Applications Information (continued)

NOTES: ● = Programmable backlight steps, ○ = Non-programmable fade steps

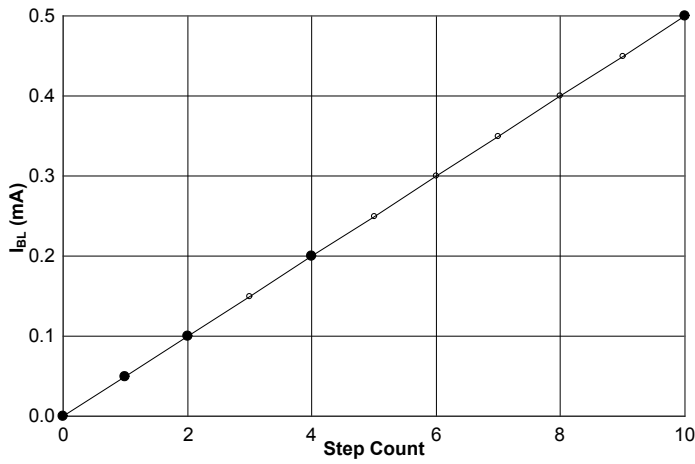


Figure 2 — Backlight Fade Steps (0.0mA to 0.5mA)

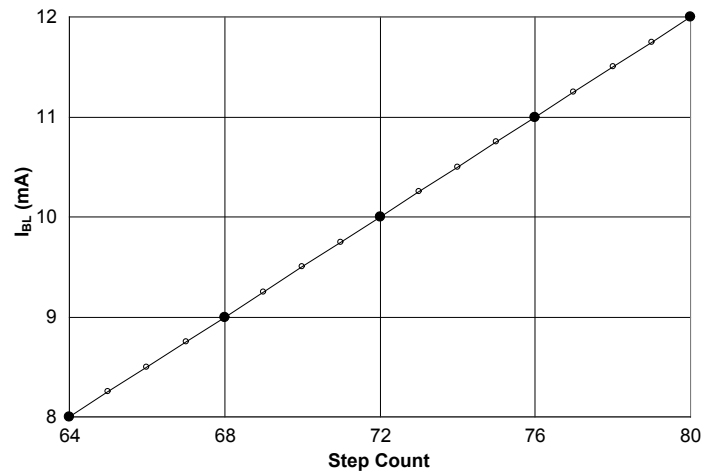


Figure 5 — Backlight Fade Steps (8.0mA to 12.0mA)

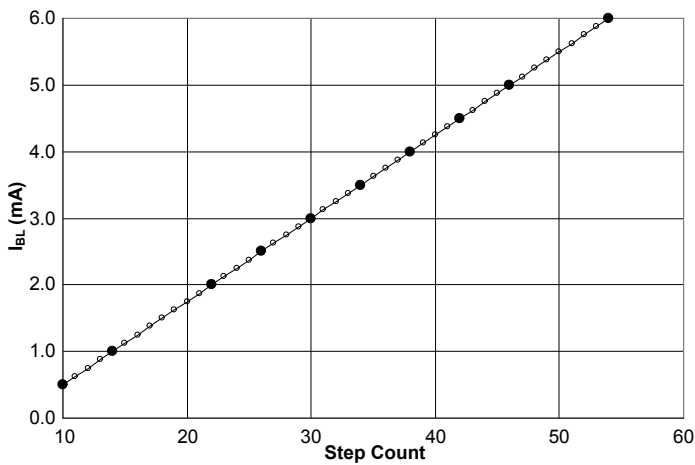


Figure 3 — Backlight Fade Steps (0.5mA to 6.0mA)

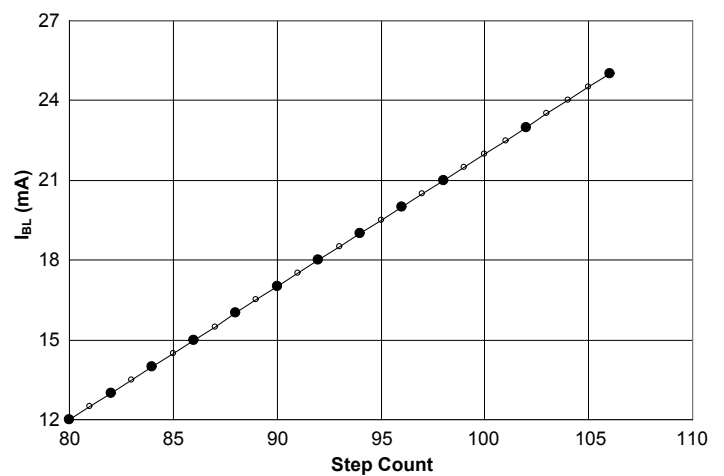


Figure 6 — Backlight Fade Steps (12.0mA to 25.0mA)

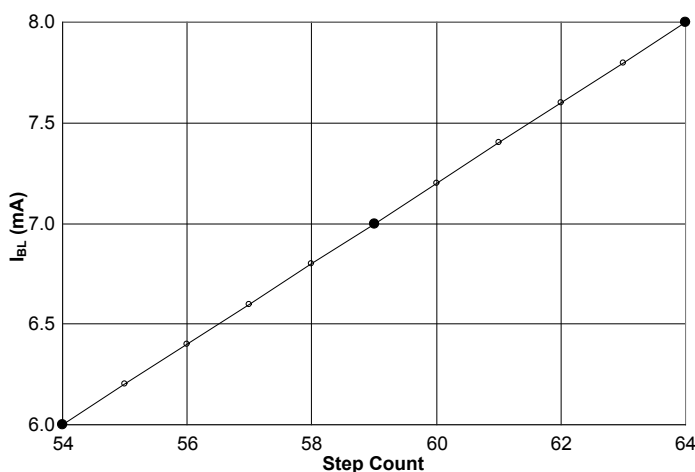


Figure 4 — Backlight Fade Steps (6.0mA to 8.0mA)

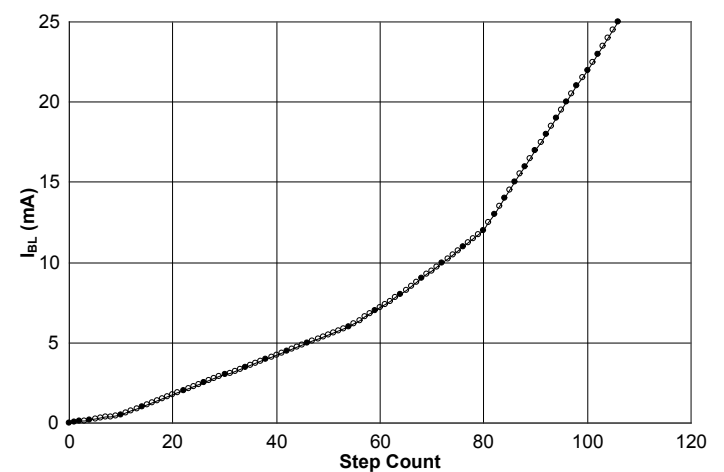


Figure 7 — Backlight Fade Steps (0.0mA to 25.0mA)

Applications Information (continued)

Sleep Mode

When all LEDs are disabled, sleep mode is activated. This is a reduced current mode that helps minimize overall current consumption by disabling the clock and the charge pump while continuing to monitor the serial interface for commands. An additional current savings can be obtained by putting the serial interface in standby mode (see SemPulse Interface, Standby Mode).

Protection Features

The SC662 provides several protection features to safeguard the device from catastrophic failures. These features include:

- Output Open Circuit Protection
- Over-Temperature Protection
- Charge Pump Output Current Limit
- LED Float Detection

Output Open Circuit Protection

Over-Voltage Protection (OVP) at the OUT pin prevents the charge pump from producing an excessively high output voltage. In the event of an open circuit between the OUT pin and all current sinks (no loads connected), the charge pump runs in open loop and the voltage rises up to the OVP limit. OVP operation is hysteretic, meaning the charge pump will momentarily turn off until V_{OUT} is sufficiently reduced. The maximum OVP threshold is 6.0V, allowing the use of a ceramic output capacitor rated at 6.3V.

Over-Temperature Protection

The OT (Over-Temperature) protection circuit prevents the device from overheating and experiencing a catastrophic failure. When the junction temperature exceeds 165°C, the device goes into thermal shutdown with all outputs disabled until the junction temperature is reduced. All register information is retained during thermal shutdown. Hysteresis of 20°C is provided to ensure that the device cools sufficiently before re-enabling.

Charge Pump Output Current Limit

The device limits the charge pump current at the OUT pin. If the OUT pin is shorted to ground, or V_{OUT} is lower than V_{UVLO} , the typical output current limit is 60mA. The output current is limited to 300mA when over loaded resistively with V_{OUT} greater than 2.4V.

LED Float Detection

Float detect is a fault detection feature of the LED backlight outputs. If an output is programmed to be enabled and an open circuit fault occurs at any backlight output, that output will be disabled to prevent a sustained output OVP condition from occurring due to the resulting open loop. Float detect ensures device protection but does not ensure optimum performance. Unused LED outputs must be disabled to prevent an open circuit fault from occurring.

Capacitor Selection

The SC662 is designed to use low-ESR ceramic capacitors for the input and output decoupling capacitors as well as the charge pump bucket capacitors. The required value of input and output capacitors can vary with supply and layout conditions, but typically 1 μ F 0402 (1005 metric) size X5R capacitors are sufficient for both C_{IN} and C_{OUT} when 250kHz is selected for the charge pump clock. Typically 0.47 μ F 0402 size X5R capacitors are sufficient for C_{IN} and C_{OUT} when the charge pump clock is 1MHz.

Table 1 — Recommended Capacitors

Cap	Value μ F	Case Size	f_{PUMP} kHz	Notes
C_{IN}, C_{OUT}	1.0	0402	250	Recommended for FSEL = 0, Typical output $V_{pp} \leq 40$ mV at 250kHz
	0.47	0402	1000	Recommended for FSEL = 1, Typical output $V_{pp} \leq 40$ mV at 1MHz
C_1, C_2	1.0	0402	250	Required to provide full rated output current and maintain a low 1.5x—2x mode transition point for optimum efficiency.
	0.47	0402	1000	Required to provide full rated output current and maintain a low 1.5x—2x mode transition point for optimum efficiency.

NOTE: Use only X5R type capacitors, with a 6.3V rating or higher

Applications Information (continued)

Thermal Management

PCB (Printed Circuit Board) layout directly effects the junction to ambient thermal resistance (θ_{JA}). Layout performance may place limits on the SC662 performance. The SC662 is capable of 150mA of total output current in an ambient temperature of up to 85°C. Both of these parameters, maximum output current ($I_{OUT(MAX)}$), and maximum ambient temperature (T_A), may be reduced if the layout does not provide for adequate heat dissipation. Layout guidelines are recommended in the next section, PCB Layout Considerations.

Applications Information (continued)

PCB Layout Considerations

Following fundamental layout rules is critical for achieving the performance specified in the Electrical Characteristics table. A recommended layout is illustrated in Figures 8, 9, and 10. Figure 8 shows a composite view of the two copper layers plus components, vias, and text descriptors. Figure 9 shows the copper layer on the component side of the board, and Figure 10 is the copper layer for ground and routing.

The following guidelines are recommended when developing a PCB layout:

- Place all capacitors (C1, C2, CIN, and COUT) as close to the device as possible, and on the same side of the board as the SC662.
- CIN, COUT should have their grounds connected at one point as shown in Figure 8, with multiple vias to ground.
- C1 and C2 should be placed so that they do not require vias to connect to the SC662.
- All charge pump current passes through pins IN, OUT, C1-, C1+, C2+, and C2-. Ensure that all connections to these pins use wide traces. Layout should minimize the resistance and inductance of these traces.
- Make all ground connections to a ground plane as shown in the example layout. There should be a short unobstructed path between all ground vias on the ground plane.
- The power trace connecting the battery to the IN pin should be sized for 300mA of battery current. The power trace should be on a layer adjacent to the ground return. If possible, make the power trace equal in width to the ground return trace.
- The output trace connecting the OUT pin to the anode terminals of the LEDs should be sized for 150mA of DC current.
- Up to six LED traces connect between the LED cathodes and the BLn pins. Each LED trace width should be sized for 25mA of DC current. The LED traces route in parallel on one layer and serve as

the return current path from the LEDs to the BLn pins.

- Figure 8 is representative of a two layer design. As shown in this figure, the OUT trace can be placed next to the six LED traces on the same layer. However, if more than two layers are available, the preferred method is to have the OUT trace route underneath the LED traces on a different layer.
- Double vias are preferred for grounding pin 3 of the SC662, and also for grounding the ground leads of CIN and COUT.
- The SPIF trace should be routed away from sources of noise to preserve the signal integrity for the SemPulse interface.
- Multiple vias are recommended for the thermal pad at the center of the device.

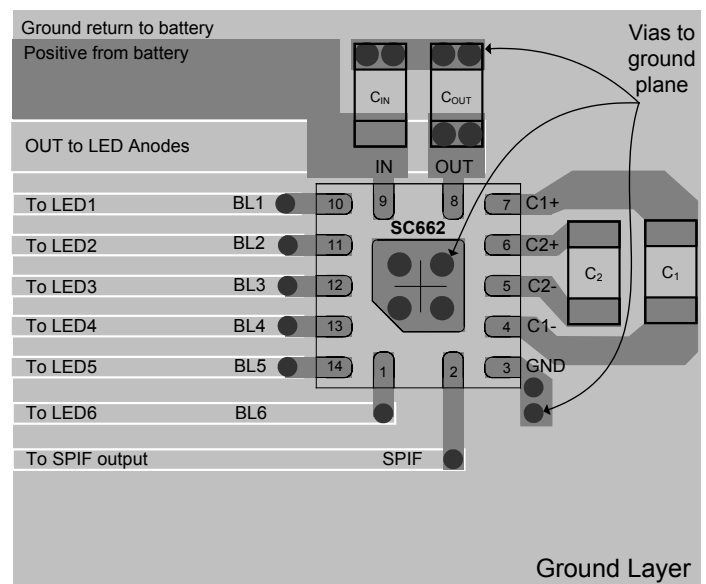


Figure 8 — Recommended PCB Layout

Applications Information (continued)

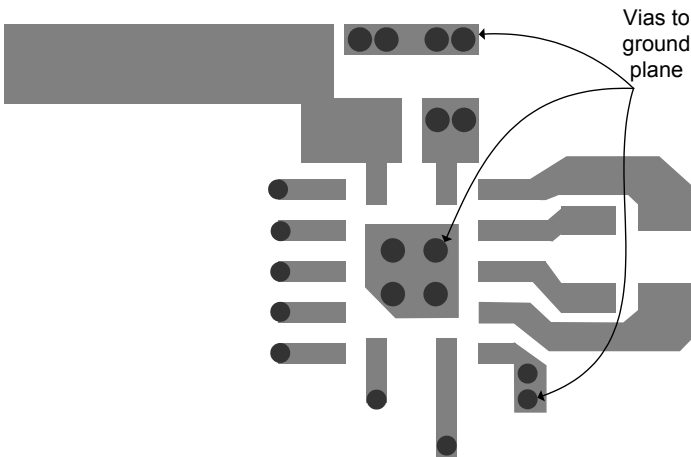


Figure 9 — Component Layer

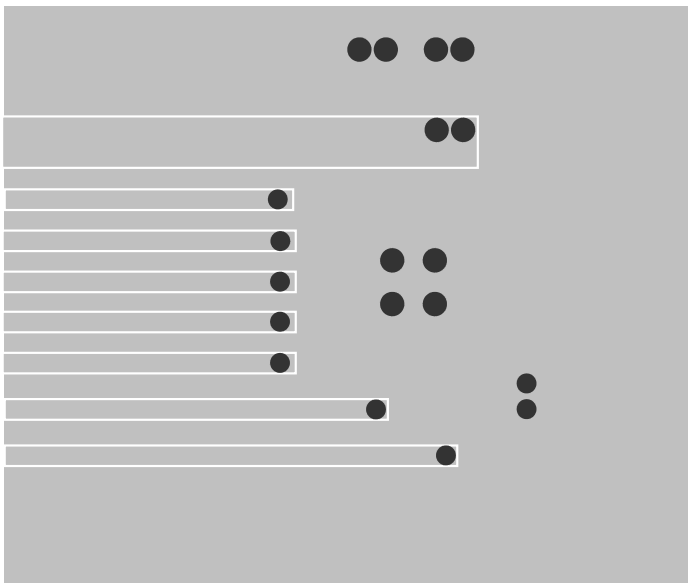


Figure 10 — Ground Layer

SemPulse™ Interface

Introduction

SemPulse is a write-only single wire interface. It provides the capability to access up to 32 registers that control device functionality. Two sets of pulse trains are transmitted via the SPIF pin. The first pulse set is used to set the desired address. After the bus is held high for the address hold period, the next pulse set is used to write the data value. After the data pulses are transmitted, the bus is held high again for the data hold period to signify the data write is complete. At this point the device latches the data into the address that was selected by the first set of pulses. See the SemPulse Timing Diagrams for descriptions of all timing parameters.

Chip Enable/Disable

The device is enabled when the SemPulse interface pin (SPIF) is pulled high for greater than t_{SU} . If the SPIF pin is pulled low again for more than t_{SD} , the device will be disabled.

Address Writes

The first set of pulses can range between 0 and 31 (or 1 to 32 rising edges) to set the desired address. After the pulses are transmitted, the SPIF pin must be held high for t_{HOLDA} to signal to the slave device that the address write is finished. If the pulse count is between 0 and 31 and the line is held high for t_{HOLDA} , the address is latched as the destination for the next data write. If the SPIF pin is not held high for t_{HOLDA} , the slave device will continue to count pulses. Note that if t_{HOLDA} exceeds its maximum specification, the bus will reset. This means that the communication is ignored and the bus resumes monitoring the pin, expecting the next pulse set to be an address. If the total exceeds 31 pulses, SPIF must be held high until the bus reset time t_{BR} is exceeded before commencing communication.

Data Writes

After the bus has been held high for the minimum address hold period, the next set of pulses are used to write the data value. The total number of pulses can range from 0 to 63 (or 1 to 64 rising edges) since there are a total of 6

register bits per register. Just like with the address write, the data write is only accepted if the bus is held high for t_{HOLDD} when the pulse train is completed. If the proper hold time is not received, the interface will keep counting pulses until the hold time is detected. If the total exceeds 63 pulses, the write will be ignored and the bus will reset after the next valid hold time is detected. After the bus has been held high for t_{HOLDD} , the bus will expect the next pulse set to be an address write. Note that this is the same effect as the bus reset that occurs when t_{HOLDA} exceeds its maximum specification. For this reason, there is no maximum limit on t_{HOLDD} — the bus simply waits for the next valid address to be transmitted.

Multiple Writes

It is important to note that this single-wire interface requires the address to be paired with its corresponding data. If it is desired to write multiple times to the same address, the address must always be re-transmitted prior to the corresponding data. If it is only transmitted one time and followed by multiple data transmissions, every other block of data will be treated like a new address. The result will be invalid data writes to incorrect addresses. Note that multiple writes only need to be separated by the minimum t_{HOLDD} for the slave to interpret them correctly. As long as t_{HOLDA} between the address pulse set and the data pulse set is less than its maximum specification but greater than its minimum, multiple pairs of address and data pulse counts can be made with no detrimental effects.

Standby Mode

Once data transfer is completed, the SPIF line must be returned to the high state for at least 10ms to return to the standby mode. In this mode, the SPIF line remains idle while monitoring for the next command. This mode allows the device to minimize current consumption between commands. Once the device has returned to standby mode, the bus is automatically reset to expect the address pulses as the next data block. This safeguard is intended to reset the bus to a known state (waiting for the beginning of a write sequence) if the delay exceeds the reset threshold.

SemPulse™ Interface (continued)

SemPulse Timing Diagrams

The SemPulse single wire interface is used to enable or disable the device and configure all registers (see Figure 11). The timing parameters refer to the digital I/O electrical specifications.

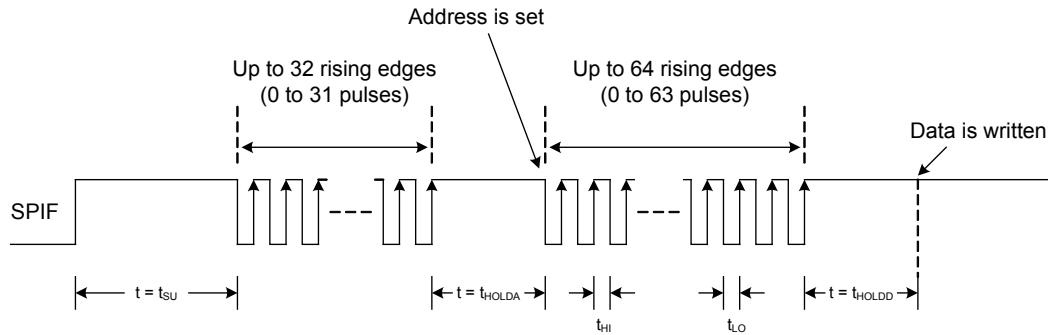


Figure 11 — Uniform Timing Diagram for SemPulse Communication

Timing Example 1

In this example (see Figure 12), the slave chip receives two sets of pulses to set the address and data, and the pulses experience interrupts that cause the pulse width to be nonuniform. Note that as long as the maximum high and low times are satisfied and the hold times are within specification, the data transfer is completed regardless of the number of interrupts that delay the transmission.

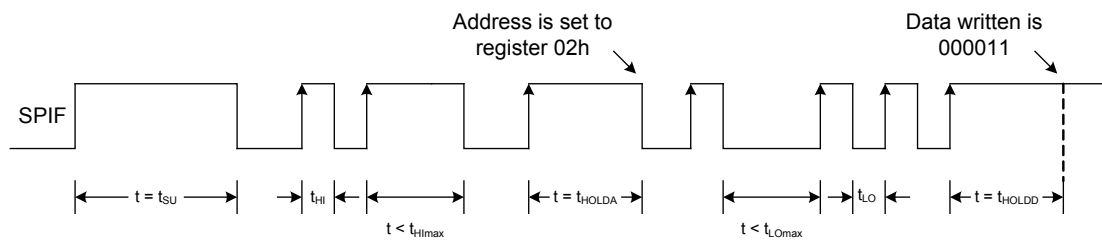


Figure 12 — SemPulse Data Write with Non-Uniform Pulse Widths

Timing Example 2

In this example (see Figure 13), the slave chip receives two sets of pulses to set the address and data, but an interrupt occurs during a pulse that causes it to exceed the minimum address hold time. The write is meant to be the value 03h in register 05h, but instead it is interpreted as the value 02h written to register 02h. The extended pulse that is delayed by the interrupt triggers a false address detection, causing the next pulse set to be interpreted as the data set. To avoid any problems with timing, make sure that all pulse widths comply with their timing requirements as outlined in this datasheet.

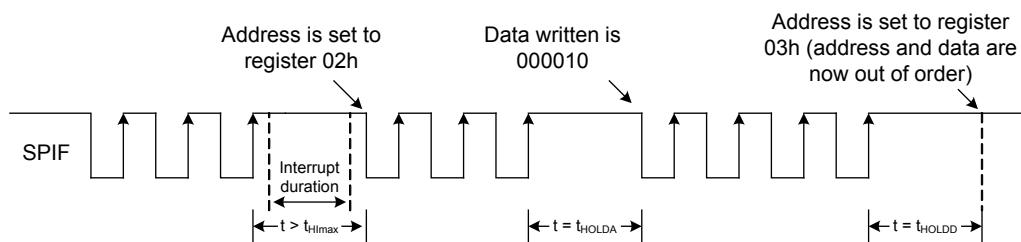


Figure 13 — Faulty SemPulse Data Write Due to Extended Interrupt Duration

Register Map⁽¹⁾

Address	D5	D4	D3	D2	D1	D0	Reset Value	Description
00h	BL EN6	BL EN5	BL EN4	BL EN3	BL EN2	BL EN1	00h	Backlight Enable
01h	0 ⁽²⁾	MBL4	MBL3	MBL2	MBL1	MBL0	00h	Main Backlight Current
02h	0 ⁽²⁾	SBL4	SBL3	SBL2	SBL1	SBL0	00h	Sub Backlight Current
03h	0 ⁽²⁾	TBL4	TBL3	TBL2	TBL1	TBL0	00h	Third Backlight Current
04h	0 ⁽²⁾	0 ⁽²⁾	0 ⁽²⁾	0 ⁽²⁾	MFADE1	MFADE0	00h	Main Fade
05h	0 ⁽²⁾	0 ⁽²⁾	FSEL	MB2	MB1	MB0	00h	Frequency and Banking Configurations

Notes:

(1) All registers are write-only.

(2) 0 = always write a 0 to these bits

Registers and Bit Definitions

BL Enable Control Register (00h)

This register enables each individual LED.

BL EN6 — BL EN1 [D5:D0]

These active high bits enable the six backlight drivers.

Each LED can be controlled independently.

Register and Bit Definitions (continued)

Main Backlight Current Control Register (01h)

This register is used to set the currents for the backlight current sinks assigned to the Main Backlight Group. This group can also be used to control red LEDs for limited RGB control. These current sinks need to be enabled in the Backlight Enable Control register to be active.

Bit D5

This bit is unused and is always a zero, so the maximum pulse count for this register is 31.

MBL4 — MBL0 [D4:D0]

These bits are used to set the current for the main backlight current sinks. All enabled main backlight current sinks will sink the same current, as shown in Table 2.

Table 2 — Main Backlight Current Settings

MBL4	MBL3	MBL2	MBL1	MBL0	Backlight Current (mA)
0	0	0	0	0	0
0	0	0	0	1	0.05
0	0	0	1	0	0.1
0	0	0	1	1	0.2
0	0	1	0	0	0.5
0	0	1	0	1	1.0
0	0	1	1	0	1.5
0	0	1	1	1	2.0
0	1	0	0	0	2.5
0	1	0	0	1	3.0
0	1	0	1	0	3.5
0	1	0	1	1	4.0
0	1	1	0	0	4.5
0	1	1	0	1	5.0
0	1	1	1	0	6.0
0	1	1	1	1	7.0
1	0	0	0	0	8.0
1	0	0	0	1	9.0
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

Register and Bit Definitions (continued)

Sub Backlight Current Control Register (02h)

This register is used to set the currents for the backlight current sinks assigned to the Sub Backlight Group. This group can also be used to control green LEDs for limited RGB control. These current sinks need to be enabled in the Backlight Enable Control register to be active.

Bit D5

This bit is unused and is always a zero, so the maximum pulse count for this register is 31.

SBL4 — SBL0 [D4:D0]

These bits are used to set the current for the sub backlight current sinks. All enabled sub backlight current sinks will sink the same current, as shown in Table 3.

Table 3 — Sub Backlight Current Settings

SBL4	SBL3	SBL2	SBL1	SBL0	Backlight Current (mA)
0	0	0	0	0	0
0	0	0	0	1	0.05
0	0	0	1	0	0.1
0	0	0	1	1	0.2
0	0	1	0	0	0.5
0	0	1	0	1	1.0
0	0	1	1	0	1.5
0	0	1	1	1	2.0
0	1	0	0	0	2.5
0	1	0	0	1	3.0
0	1	0	1	0	3.5
0	1	0	1	1	4.0
0	1	1	0	0	4.5
0	1	1	0	1	5.0
0	1	1	1	0	6.0
0	1	1	1	1	7.0
1	0	0	0	0	8.0
1	0	0	0	1	9.0
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

Register and Bit Definitions (continued)

Third Backlight Current Control Register (03h)

This register is used to set the currents for the backlight current sinks assigned to the Third Backlight Group. This group can also be used to control blue LEDs for limited RGB control. These current sinks need to be enabled in the Backlight Enable Control register to be active.

Bit D5

This bit is unused and is always a zero, so the maximum pulse count for this register is 31.

TBL4 — TBL0 [D4:D0]

These bits are used to set the current for the third backlight current sinks. All enabled third backlight current sinks will sink the same current, as shown in Table 4.

Table 4 — Third Backlight Current Control Bits

TBL4	TBL3	TBL2	TBL1	TBL0	Backlight Current (mA)
0	0	0	0	0	0
0	0	0	0	1	0.05
0	0	0	1	0	0.1
0	0	0	1	1	0.2
0	0	1	0	0	0.5
0	0	1	0	1	1.0
0	0	1	1	0	1.5
0	0	1	1	1	2.0
0	1	0	0	0	2.5
0	1	0	0	1	3.0
0	1	0	1	0	3.5
0	1	0	1	1	4.0
0	1	1	0	0	4.5
0	1	1	0	1	5.0
0	1	1	1	0	6.0
0	1	1	1	1	7.0
1	0	0	0	0	8.0
1	0	0	0	1	9.0
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

Register and Bit Definitions (continued)

Main Fade Control (04h)

This register sets the fade status and rate for the main backlight group.

Bits [D5:D2]

These bits are unused and are always zeros, so the maximum pulse count for this register is 3.

MFADE1, MFADE0[D1:D0]

These bits are used to enable fade and set the fade rate between two backlight currents as shown in Table 5.

Table 5 — Main Display Fade Control Bits

MFADE1	MFADE0	Fade Feature Rise/Fall Rate (ms/step)
0	0	OFF
0	1	2
1	0	4
1	1	6

When the fade rate is set to 2, 4, or 6ms and then a new backlight current is set, the backlight current will change from its current value to the new value in steps, pausing at each step for the duration of the fade rate before proceeding to the next step. The exact length of time used to fade between any two backlight values is determined by multiplying the fade rate by the number of steps between the old and new backlight values. The fade time can be calculated from the data provided in Table 1 on page 15.

Backlight Grouping Configuration (05h)

This register assigns the LEDs to the backlight bank configurations.

Bits [D5:D4]

These bits are unused and are always zeros, so the maximum pulse count for this register is 16.

FSEL [D3]

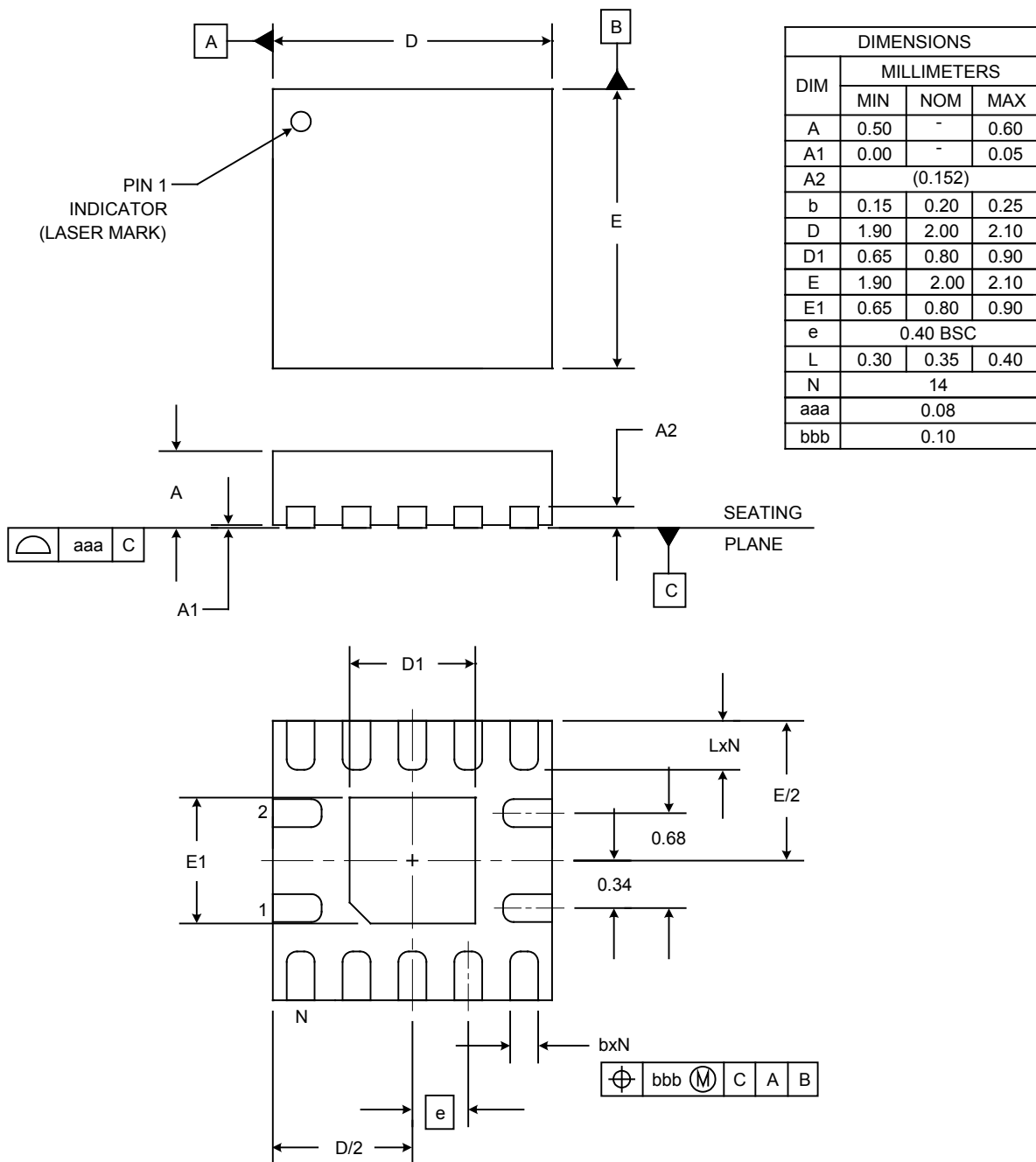
This bit sets the charge pump clock frequency. FSEL = 0 for 250kHz, and FSEL = 1 for 1MHz. The default state for this bit is zero.

MB2 and MB0 [D2:D0]

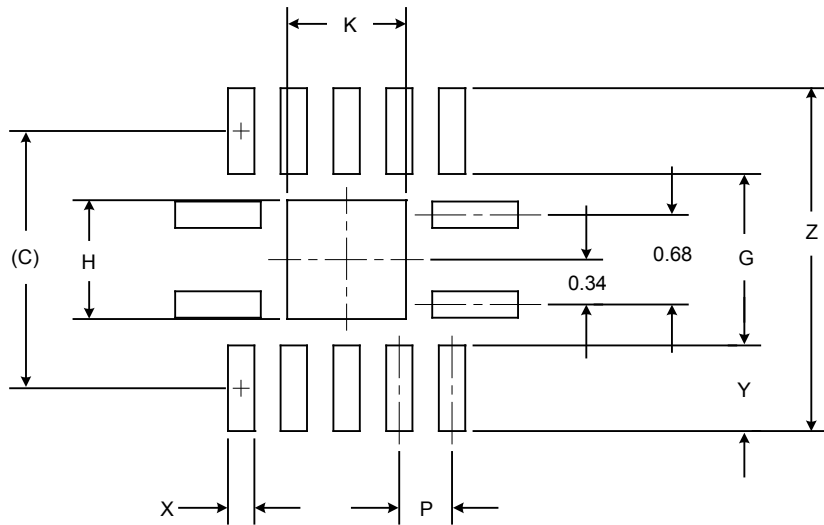
These bits are used to set the number of LED drivers dedicated to each backlight group. This allows the device to drive up to three different sets of LEDs with different current settings. Note that any driver assigned to any LED group can still be disabled independently if not needed. The code set by these bits determines how the LED drivers are assigned among the three LED groups according to the assignments listed in Table 6. Default state for each of these three bits is zero (all LEDs assigned to main display).

Table 6 — Backlight Grouping Configuration

MB2	MB1	MB0	Main Display LED Drivers	Sub Display LED Drivers	Third Display LED Drivers
0	0	0	BL1-BL6		
0	0	1	BL1-BL3	BL4-BL6	
0	1	0	BL1-BL2	BL3-BL4	BL5-BL6
0	1	1	BL1-BL2, BL5-BL6	BL3	BL4
1	0	0	BL1-BL3	BL4-BL5	BL6
1	0	1	BL1-BL4	BL5-BL6	
1	1	X	BL1-BL5	BL6	

Outline Drawing — MLPQ-UT-14 2x2

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern — MLPQ-UT-14 2x2


DIMENSIONS	
DIM	MILLIMETERS
C	(1.95)
G	1.30
H	0.80
K	0.80
P	0.40
X	0.20
Y	0.65
Z	2.60

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH " X " AND " Y " DIRECTIONS.



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Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 Fax: (805) 498-3804

www.semtech.com