

24-Bit, 192kHz Stereo ADC

DESCRIPTION

The WM8785 is a stereo audio ADC with differential inputs designed for high performance recordable media applications. Data is provided as a PCM output.

Stereo 24-bit multi-bit sigma-delta ADCs are used with digital audio output word lengths of 16 to 32 bits, and sampling rates from 8kHz to 192kHz. The device has a selectable high pass filter to remove residual DC offsets. The device also supports a TDM bus for data out.

The device is controlled via a 2 or 3 wire serial interface. The interface provides access to all features including oversampling rate, audio format, powerdown, master/slave control and digital signal manipulation. The device is supplied in a 20-lead SSOP package.

FEATURES

- SNR 111dB ('A' weighted @ 48kHz)
- THD -102dB (at -0.1dB)
- Sampling Frequency: 8 – 192kHz
- 2 or 3 Wire Microprocessor Control Interface
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
 - I²S, Left, Right Justified or DSP
 - 16/20/24/32 bit Word Lengths
- A TDM bus is supported for data out
- Supply Voltages
 - Analogue 4.5 to 5.5V
 - Digital core: 2.7V to 3.6V
- 20-lead SSOP package

APPLICATIONS

- Recordable DVD Players
- Personal Video Recorders
- High End Sound Cards
- Studio Audio Processing Equipment

BLOCK DIAGRAM

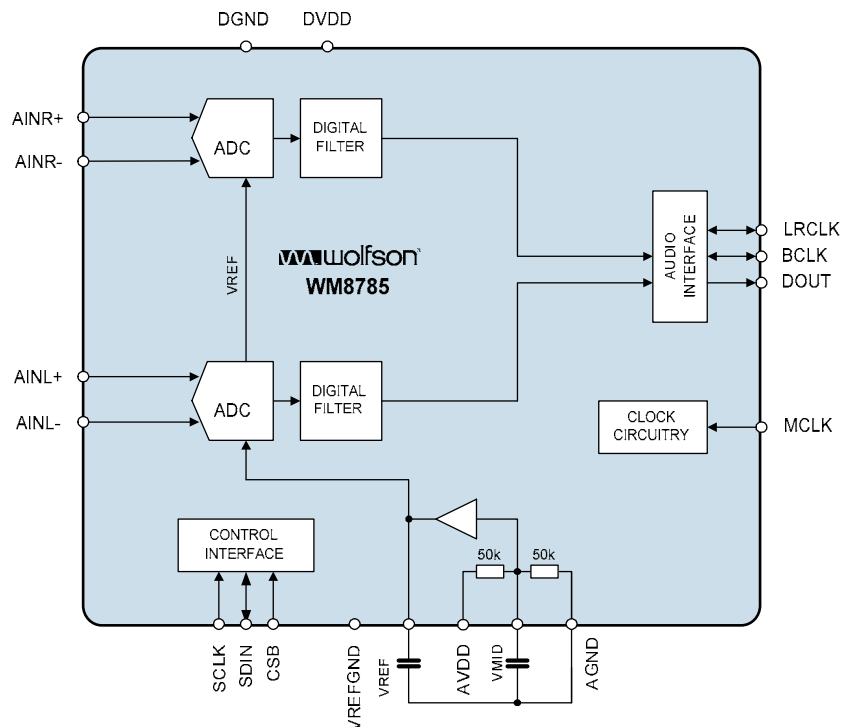
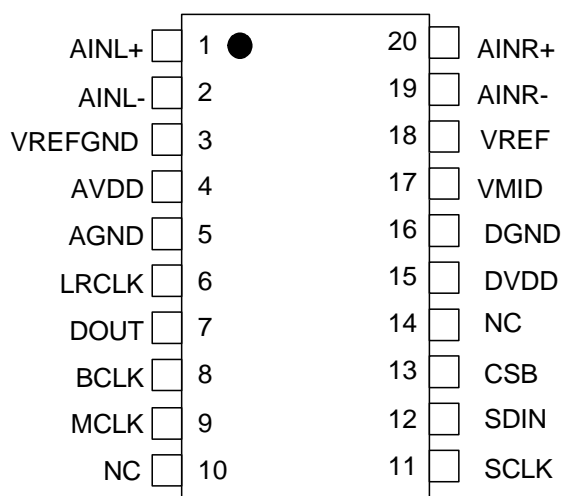


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PIN CONFIGURATION



ORDERING INFORMATION

| ORDER CODE | TEMPERATURE RANGE | PACKAGE | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|---------------|-------------------|--|----------------------------|----------------------------|
| WM8785GEDS/V | -25°C to +85°C | 20-lead SSOP (Pb-free) | MSL3 | 260°C |
| WM8785GEDS/RV | -25°C to +85°C | 20-lead SSOP (Pb-free, tape and reel) | MSL3 | 260°C |

Note:

Reel quantity = 2,000

PIN DESCRIPTION

| PIN | NAME | TYPE | DESCRIPTION |
|------------|-------------|------------------------|--|
| 1 | AINL+ | Analogue Input | Left Channel Positive Input |
| 2 | AINL- | Analogue Input | Left Channel Negative Input |
| 3 | VREFGND | Analogue Reference | Negative Reference Connection |
| 4 | AVDD | Supply | Analogue Supply |
| 5 | AGND | Supply | Analogue Ground (return path for AVDD) |
| 6 | LRCLK | Digital Input / Output | Audio Interface Left / Right Clock |
| 7 | DOUT | Digital Output | ADC Digital Audio Data |
| 8 | BCLK | Digital Input / Output | Audio Interface Bit Clock |
| 9 | MCLK | Digital Input | Master Clock |
| 10 | NC | NC | No Connection |
| 11 | SCLK | Digital Input | Control Interface Clock Input / 2 wire output |
| 12 | SDIN | Digital Input / Output | Control Interface Data Input |
| 13 | CSB | Digital Input | Chip Select / Control Interface Format Selection / 3 wire address select |
| 14 | NC | NC | No connection |
| 15 | DVDD | Supply | Digital Supply |
| 16 | DGND | Supply | Digital Ground (return path for DVDD) |
| 17 | VMID | Analogue Output | Midrail Voltage Decoupling Capacitor |
| 18 | VREF | Analogue Reference | Reference Voltage Decoupling Capacitor |
| 19 | AINR- | Analogue Input | Right Channel Negative Input |
| 20 | AINR+ | Analogue Input | Right Channel Positive Input |

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

| CONDITION | MIN | MAX |
|---|------------|-------------|
| Digital supply voltage | -0.3V | +3.63V |
| Analogue supply voltage | -0.3V | +7V |
| Voltage range digital inputs | DGND -0.3V | DVDD + 0.3V |
| Voltage range analogue inputs | AGND -0.3V | AVDD +0.3V |
| Master Clock Frequency | | 40MHz |
| Operating temperature range, T _A | -25°C | +85°C |
| Storage temperature after soldering | -65°C | +150°C |

Note: Analogue and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|-----------|-----------------|-----|-----|-----|------|
| Digital supply range | DVDD | | 2.7 | | 3.6 | V |
| Analogue supply range | AVDD | | 4.5 | | 5.5 | V |
| Ground | DGND,AGND | | | 0 | | V |

ELECTRICAL CHARACTERISTICS

Test Conditions

DVDD = 3.3V, AVDD = 5.0V, $T_A = +25^\circ\text{C}$, 1kHz signal, A-weighted, $f_s = 48\text{kHz}$, MCLK = 256fs, 24-bit audio data, Slave Mode unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------|--|--------------------------|--------------------------|--------------------------|------------------|
| ADC Performance | | | | | | |
| Full Scale Input Signal Level (for ADC 0dB Input) | | | | 2.0 | | V_{rms} |
| Input resistance | | | | 10 | | $k\Omega$ |
| Input capacitance | | | | 10 | | pF |
| Signal to Noise Ratio (Note 1,2,4) | SNR | A-weighted, @ $f_s = 48\text{kHz}$ | 102 | 111 | | dB |
| | | Unweighted, @ $f_s = 48\text{kHz}$ | | 108 | | dB |
| Signal to Noise Ratio (Note 1,2,4) | SNR | A-weighted, @ $f_s = 96\text{kHz}$ | | 111 | | dB |
| | | Unweighted, @ $f_s = 96\text{kHz}$ | | 108 | | dB |
| Signal to Noise Ratio (Note 1,2,4) | SNR | A-weighted, @ $f_s = 192\text{kHz}$ | | 111 | | dB |
| | | Unweighted, @ $f_s = 192\text{kHz}$ | | 108 | | dB |
| Total Harmonic Distortion | THD | 1kHz, -0.1dB Full Scale @ $f_s = 48\text{kHz}$ | | -102 | -92 | dB |
| | | 1kHz, -0.1dB Full Scale @ $f_s = 96\text{kHz}$ | | -102 | | dB |
| | | 1kHz, -0.1dB Full Scale @ $f_s = 192\text{kHz}$ | | -102 | | dB |
| Total Harmonic Distortion | THD | 1kHz, -0.1dB Full Scale @ $f_s = 48\text{kHz}$ | | 0.0008 | 0.0025 | % |
| | | 1kHz, -0.1dB Full Scale @ $f_s = 96\text{kHz}$ | | 0.0008 | | % |
| | | 1kHz, -0.1dB Full Scale @ $f_s = 192\text{kHz}$ | | 0.0008 | | % |
| Dynamic Range | DNR | -60dBFS | 102 | 111 | | dB |
| Channel Level Matching | | 20kHz signal | | 0.1 | | dB |
| Power Supply Rejection Ratio | PSRR | 1kHz 100mVpp, applied to AVDD, DVDD | | 50 | | dB |
| | | 20Hz to 20kHz 100mVpp | | 45 | | dB |
| Digital Logic Levels (CMOS Levels) | | | | | | |
| Input LOW level | V_{IL} | | | | $0.3 \times \text{DVDD}$ | V |
| Input HIGH level | V_{IH} | | $0.7 \times \text{DVDD}$ | | | V |
| Input leakage current | | | -1 | ± 0.2 | +1 | μA |
| Input capacitance | | | | 5 | | pF |
| Output LOW | V_{OL} | $I_{\text{OL}}=1\text{mA}$ | | | $0.1 \times \text{DVDD}$ | V |
| Output HIGH | V_{OH} | $I_{\text{OH}}=-1\text{mA}$ | $0.9 \times \text{DVDD}$ | | | V |
| Analogue Reference Levels | | | | | | |
| Midrail Reference Voltage | VMID | AVDD to VMID and VMID to VREFGND | -3% | AVDD/2 | +3% | V |
| Potential Divider Resistance | R_{VMID} | AVDD to VMID and VMID to GND | | 50 | | $k\Omega$ |
| Buffered Reference Voltage | VREF | | -3% | $0.8 \times \text{AVDD}$ | +3% | V |

Test Conditions

DVDD = 3.3V, AVDD = 5.0V, T_A = +25°C, 1kHz signal, A-weighted, fs = 48kHz, MCLK = 256fs, 24-bit audio data, Slave Mode unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--------|-----------------|-----|-----|-----|------|
| Supply Current | | | | | | |
| Analogue supply current | | | | 27 | | mA |
| Digital supply current | | | | 5 | | mA |
| Power Down | | | | 22 | | uA |

Note:

1. VMID is decoupled with 10uF and 0.1uF capacitors close to the device package. Smaller capacitors may reduce performance.

TERMINOLOGY

1. Signal-to-noise ratio (dB) – Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, over a 20Hz to 20kHz bandwidth. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
5. All performance measurements are done with a 20kHz low pass filter, and where noted an A-weight filter, except where noted. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although this is not audible, it may affect dynamic specification values

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

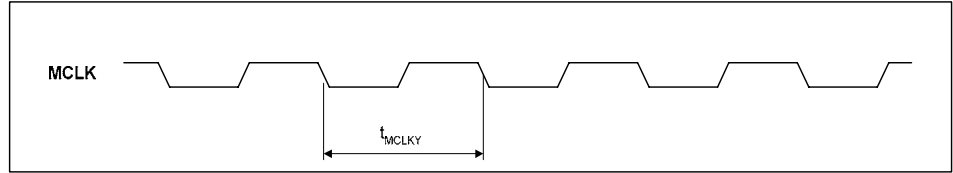


Figure 1 System Clock Timing Requirements

Test Conditions

DVDD = 3.3V, DGND = 0V, $T_A = +25^\circ\text{C}$, Slave Mode, $f_s = 48\text{kHz}$, MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|--|--------------|-------|-----|-------|------|
| System Clock Timing Information | | | | | |
| MCLK System clock cycle time | T_{MCLKY} | 25 | | | ns |
| MCLK duty cycle | T_{MCLKDS} | 60:40 | | 40:60 | |

AUDIO INTERFACE TIMING – MASTER MODE, PCM DATA

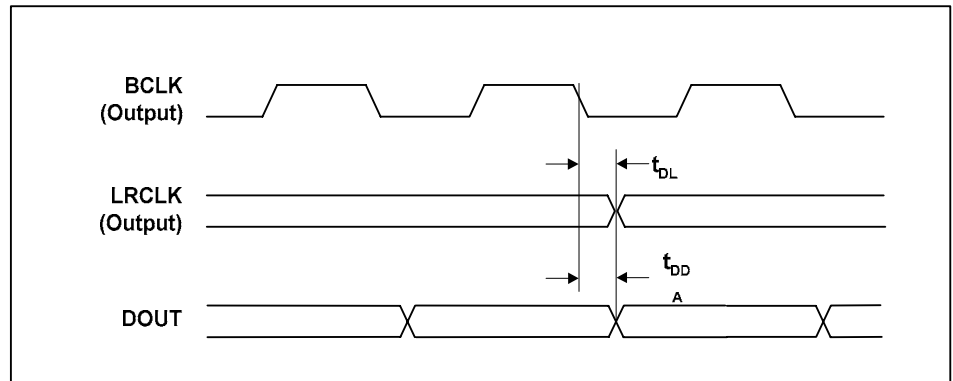


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DVDD = 3.3V, DGND = 0V, $T_A = +25^\circ\text{C}$, Master Mode, $f_s = 48\text{kHz}$, MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|--|-----------|-----|-----|-----|------|
| Audio Data Input Timing Information | | | | | |
| LRCLK propagation delay from BCLK falling edge | t_{DL} | 0 | | 10 | ns |
| DOUT propagation delay from BCLK falling edge | t_{DDA} | 0 | | 11 | ns |

AUDIO INTERFACE TIMING – SLAVE MODE, PCM DATA

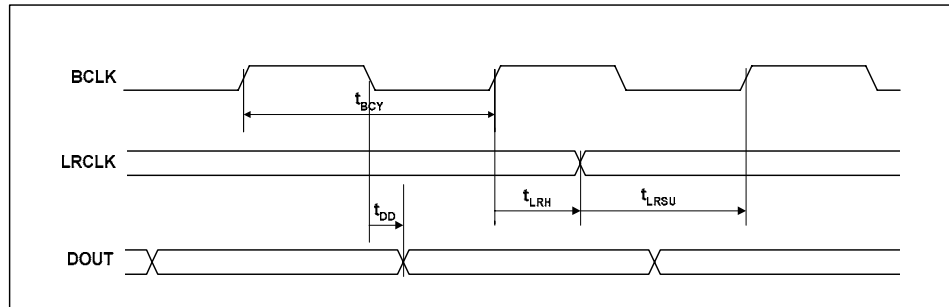


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DVDD = 3.3V, DGND = 0V, TA = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|-------------------|-----|-----|-----|------|
| Audio Data Input Timing Information | | | | | |
| BCLK cycle time | t _{BCY} | 25 | | | ns |
| LRCLK set-up time to BCLK rising edge | t _{LRSU} | 10 | | | ns |
| LRCLK hold time from BCLK rising edge | t _{LRH} | 10 | | | ns |
| DOUT propagation delay from BCLK falling edge | t _{DD} | 0 | | 11 | ns |

CONTROL INTERFACE TIMING – 3-WIRE MODE

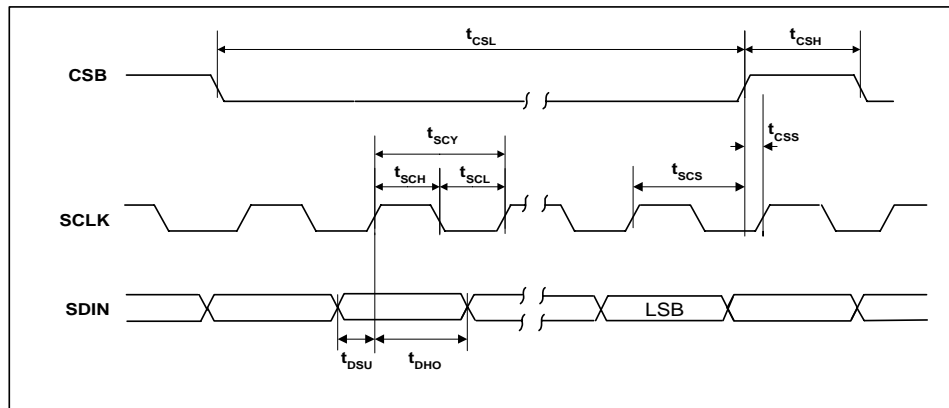


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DVDD = 3.3V, DVDD = 3.3V, DGND = 0V, TA = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|------------------|-----|-----|-----|------|
| Program Register Input Information | | | | | |
| SCLK rising edge to CSB rising edge | t _{SSC} | 80 | | | ns |
| SCLK pulse cycle time | t _{SCY} | 200 | | | ns |
| SCLK pulse width low | t _{SCL} | 80 | | | ns |
| SCLK pulse width high | t _{SCH} | 80 | | | ns |
| SDIN to SCLK set-up time | t _{DSU} | 40 | | | ns |
| SCLK to SDIN hold time | t _{DHO} | 40 | | | ns |
| CSB pulse width low | t _{CSL} | 40 | | | ns |
| CSB pulse width high | t _{CSH} | 40 | | | ns |
| CSB rising to SCLK rising | t _{CSS} | 40 | | | ns |
| Pulse width of spikes that will be suppressed | t _{ps} | 4 | | 6 | ns |

CONTROL INTERFACE TIMING – 2-WIRE MODE

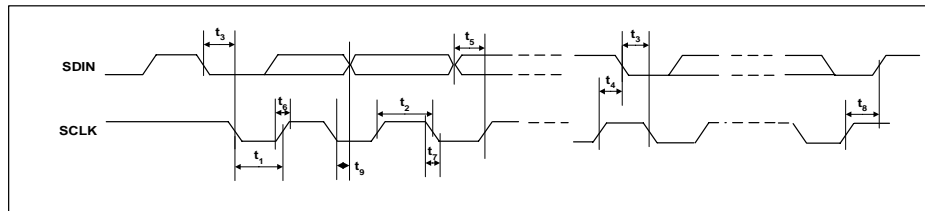


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DVDD = 3.3V, DVDD = 3.3V, DGND = 0V, $T_A = +25^\circ\text{C}$, Slave Mode, $f_s = 48\text{kHz}$, MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|----------|-----|-----|-----|------|
| Program Register Input Information | | | | | |
| SCLK Frequency | | 0 | | 5 | MHz |
| SCLK Low Pulse-Width | t_1 | 80 | | | ns |
| SCLK High Pulse-Width | t_2 | 80 | | | us |
| Hold Time (Start Condition) | t_3 | 600 | | | ns |
| Setup Time (Start Condition) | t_4 | 600 | | | ns |
| Data Setup Time | t_5 | 100 | | | ns |
| SDIN, SCLK Rise Time | t_6 | | | 300 | ns |
| SDIN, SCLK Fall Time | t_7 | | | 300 | ns |
| Setup Time (Stop Condition) | t_8 | 600 | | | ns |
| Data Hold Time | t_9 | | | 900 | ns |
| Pulse width of spikes that will be suppressed | t_{ps} | 4 | | 6 | ns |

POWER-ON RESET

The WM8785 has an internal power-on reset circuit. The reset sequence is entered at power-on or power-up (DVDD). Until the internal reset is removed, DOUT is forced to zero. DOUT remains zero for a count equal to 32 sample clocks, after power up. (This count is driven by MCLK and is independent of any external LRCLK).

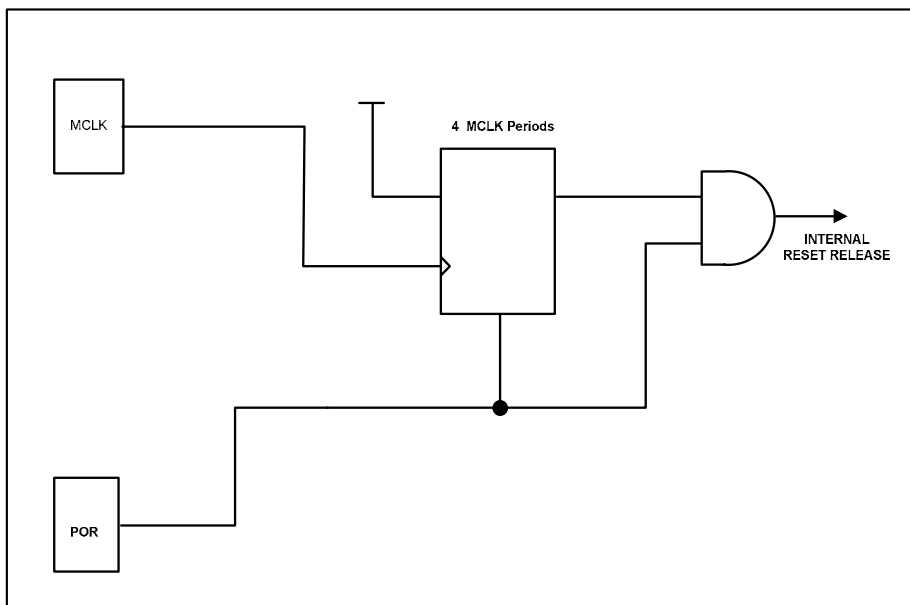


Figure 6 POR Circuit

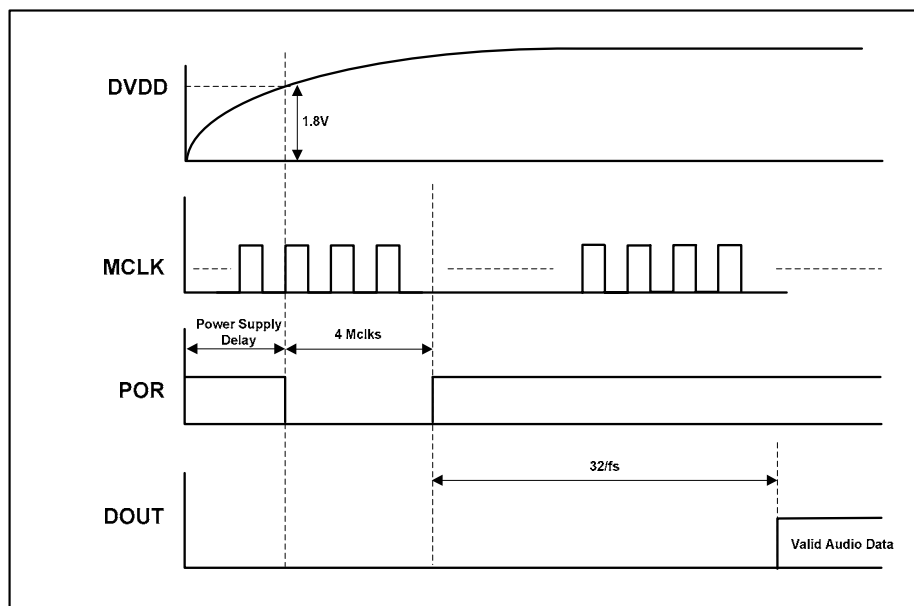


Figure 7 POR Timing

DIGITAL FILTER CHARACTERISTICS

The WM8785 digital filter characteristics scale with sample rate.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|---------|--------|-----------|------|
| ADC Sample Rate (Single Rate – 48KHz typically) | | | | | |
| Passband | +/- 0.005dB | 0 | | 0.454fs | |
| | -6dB | | 0.5fs | | |
| Passband Ripple | | | | +/- 0.005 | dB |
| Stopband | | 0.546fs | | | |
| Stopband Attenuation | f > 0.546fs | -85 | | | dB |
| Group Delay | | | 32/fs | | s |
| ADC Sample Rate (Dual Rate - 96kHz typically) | | | | | |
| Passband | +/- 0.005dB | 0 | | 0.454fs | |
| | -6dB | | 0.5fs | | |
| Passband Ripple | | | | +/- 0.005 | dB |
| Stopband | | 0.546fs | | | |
| Stopband Attenuation | f > 0.546fs | -85 | | | dB |
| Group Delay | | | 32/fs | | s |
| ADC Sample Rate (Quad Rate - 192kHz typically) | | | | | |
| Passband | +/- 0.005dB | 0 | | 0.25fs | |
| | -3dB | | 0.45fs | | |
| | -6dB | | 0.5fs | | |
| Passband Ripple | | | | +/- 0.005 | dB |
| Stopband | | 0.75fs | | | |
| Stopband Attenuation | f > 0.75fs | -85 | | | dB |
| Group Delay | | | 10/fs | | s |
| High Pass Filter Corner Frequency | -3dB | | 3.7 | | Hz |
| | -0.5dB | | 10.4 | | |
| | -0.1dB | | 21.6 | | |

TERMINOLOGY

1. Stop Band Attenuation (dB) - the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

FILTER RESPONSES

SINGLE RATE 48k

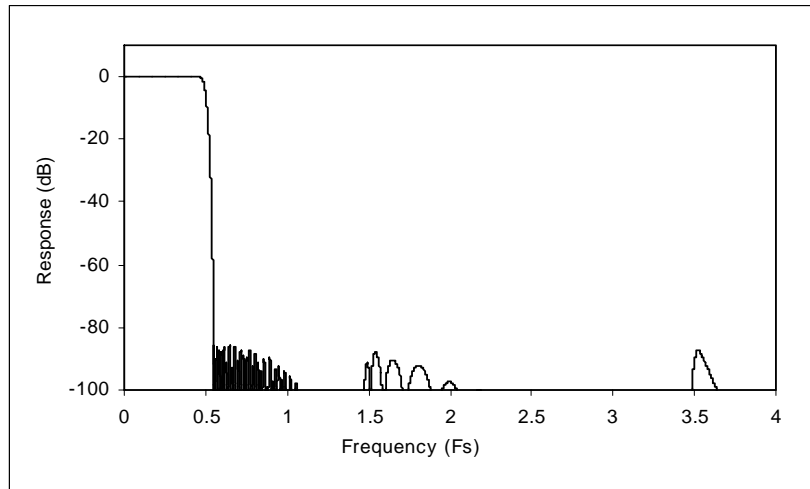


Figure 8 Single Rate 48k Filter Response

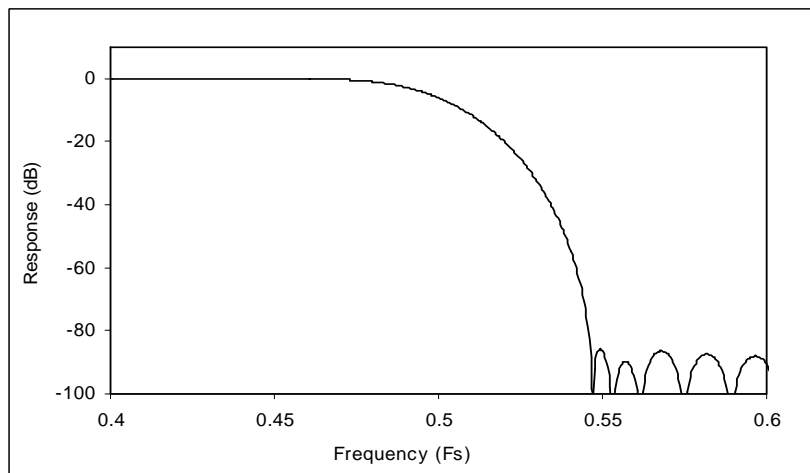


Figure 9 Single Rate 48k Filter Response

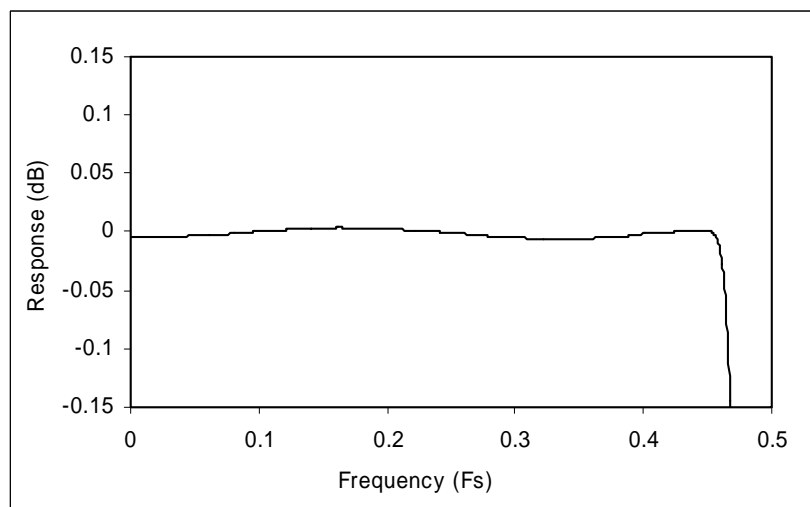


Figure 10 Single Rate 48k Filter Response

DUAL RATE 96k

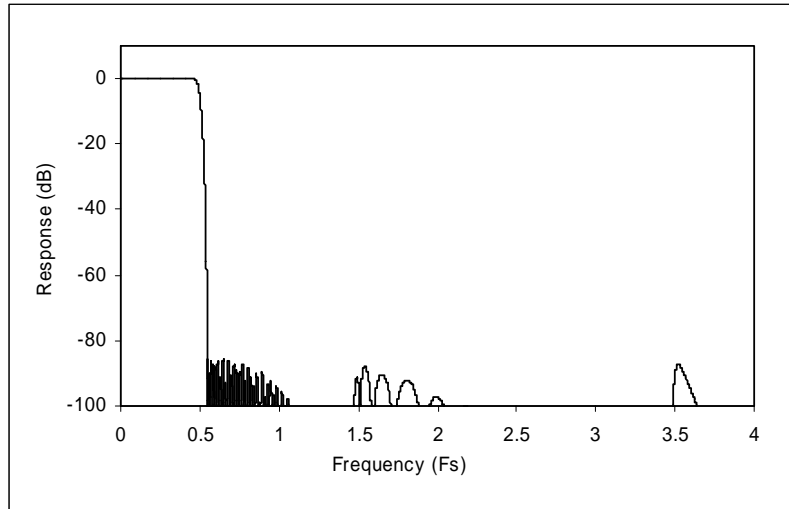


Figure 11 Dual Rate 96k Filter Response

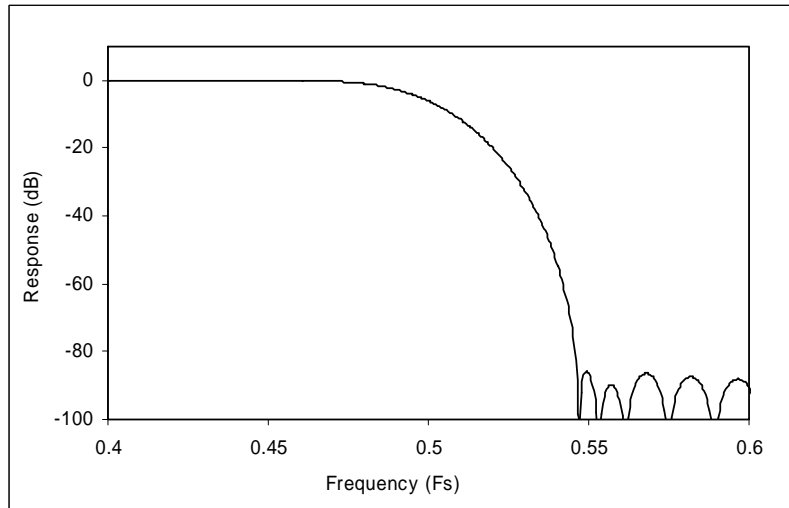


Figure 12 Dual Rate 96k Filter Response

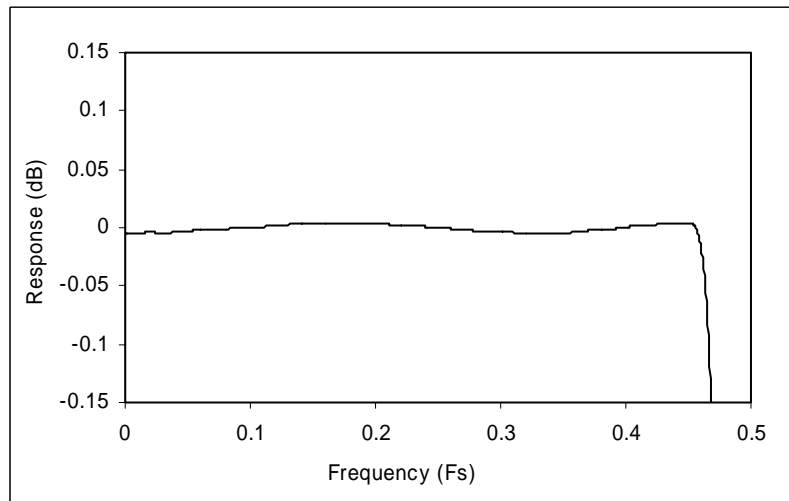


Figure 13 Dual Rate 96k Filter Response

QUAD RATE 192k

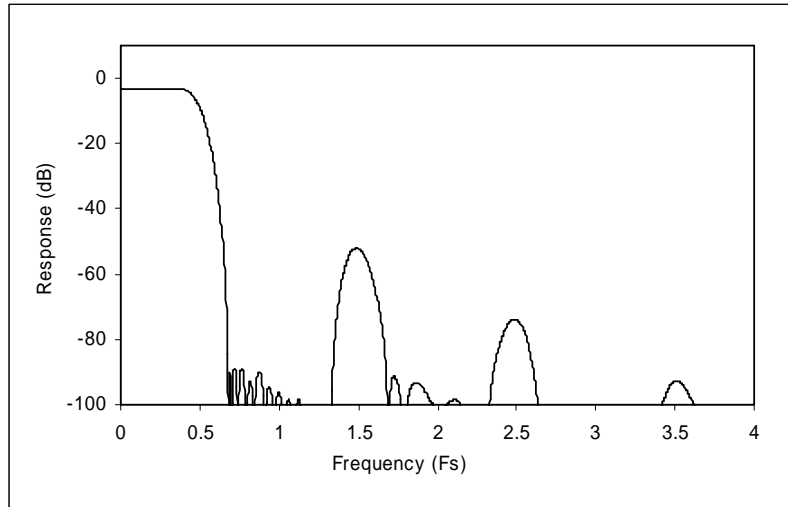


Figure 14 Quad Rate 192k Filter Response

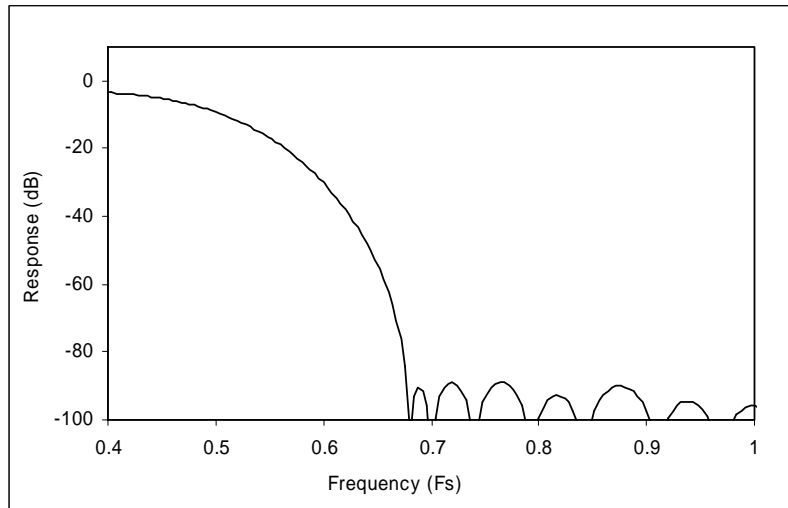


Figure 15 Quad Rate 192k Filter Response

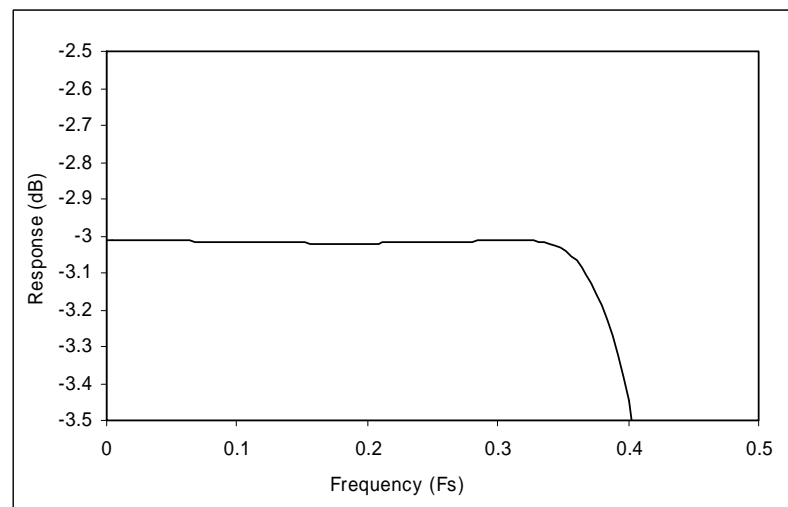


Figure 16 Quad Rate 192k Filter Response

DEVICE DESCRIPTION

INTRODUCTION

The WM8785 is a high performance stereo audio ADC designed for demanding recording applications such as DVD recorders, studio mixers, PVRs, and AV amplifiers. The WM8785 consists of stereo line level inputs, followed by a sigma-delta modulator and digital filtering.

The WM8785 uses a multi-bit high-order oversampling architecture delivering high SNR operating at oversampling ratios from 128fs to 32fs according to the sample rate. Sample rates from 8kHz to 192kHz are supported. The WM8785 supports master clock rates from 128fs to 768fs.

The digital filter is a high performance linear phase FIR filter. The digital filters are optimised for each sample rate. Also included is a selectable high pass filter to remove residual DC offsets from the input signal.

The output from the ADC is available on a configurable digital audio interface. It supports a number of audio data formats including I²S, Left justified and Right justified or DSP, and can operate in master or slave modes.

The WM8785 can be controlled through a 2 wire or 3 wire MPU control interface. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs. A TDM bus is supported for multiplexing data output.

The WM8785 can be powered down under software control to reduce system power consumption.

DIGITAL AUDIO INTERFACE

The digital audio interface uses three pins:

- DOUT: ADC data output
- LRCLK: ADC data alignment clock
- BCLK: Bit clock, for synchronisation

The digital audio interface takes the data from the internal ADC digital filters and places it on DOUT and LRCLK. DOUT is the formatted digital audio data stream output from the ADC digital filters with left and right channels multiplexed together. LRCLK is an alignment clock that controls whether Left or Right channel data is present on the DOUT line. DOUT and LRCLK are synchronous with the BCLK signal with each data bit transition signified by a BCLK high to low transition. DOUT is always an output. BCLK and LRCLK maybe inputs or outputs depending whether the device is in Master or Slave mode, (see Master and Slave Mode Operation, below).

Four different audio data formats are supported:

- Left justified
- Right justified
- I²S
- DSP

They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

MASTER AND SLAVE MODE OPERATION

The WM8785 can be configured as either a master or slave mode device. As a master device the WM8785 generates BCLK and LRCLK and thus controls sequencing of the data transfer on DOUT. In slave mode, the WM8785 responds with data to clocks it receives over the digital audio interface. The mode can be selected by setting MCR=000 (see Table below). Master and slave modes are illustrated below.

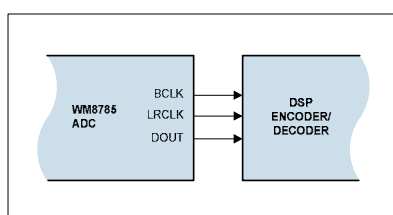


Figure 17a Master Mode

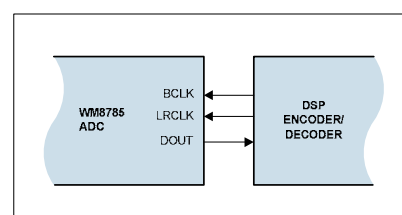


Figure 17b Slave Mode

AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

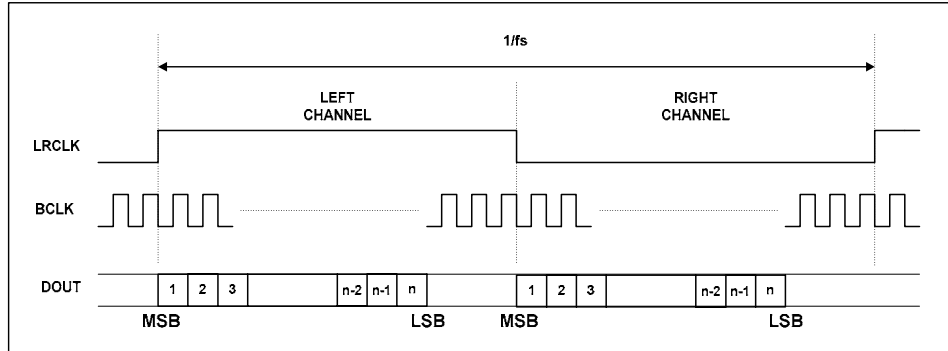


Figure 18 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.

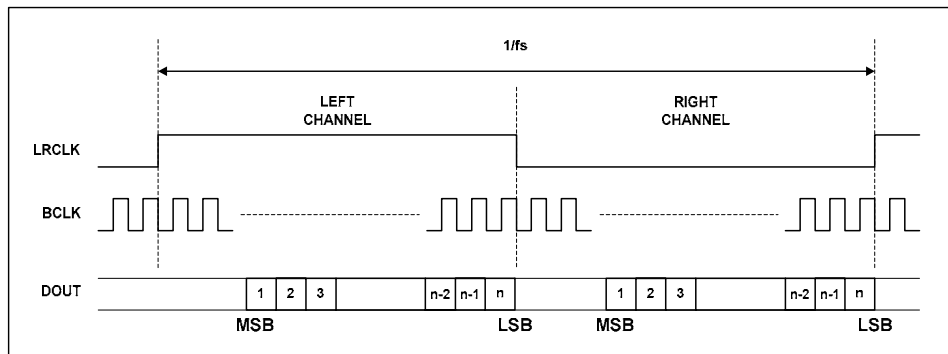


Figure 19 Right Justified Audio Interface (assuming n-bit word length)

In I²S mode, the MSB is available on the second rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

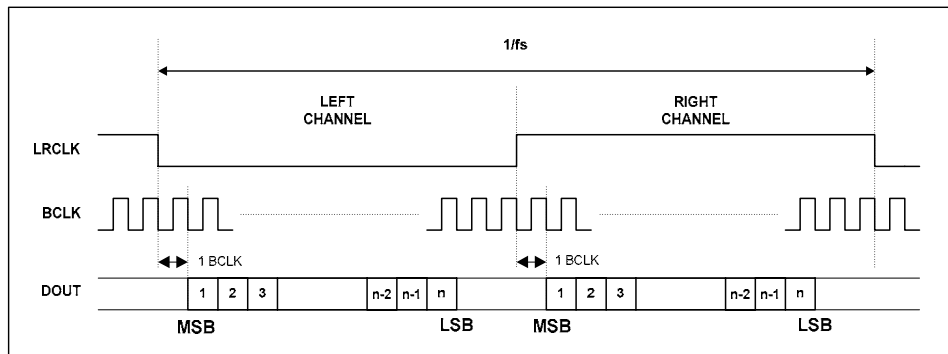


Figure 20 I²S Justified Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 21 and Figure 22. In device slave mode, Figure 23 and Figure 24, it is possible to use any length of frame pulse less than $1/f_s$, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

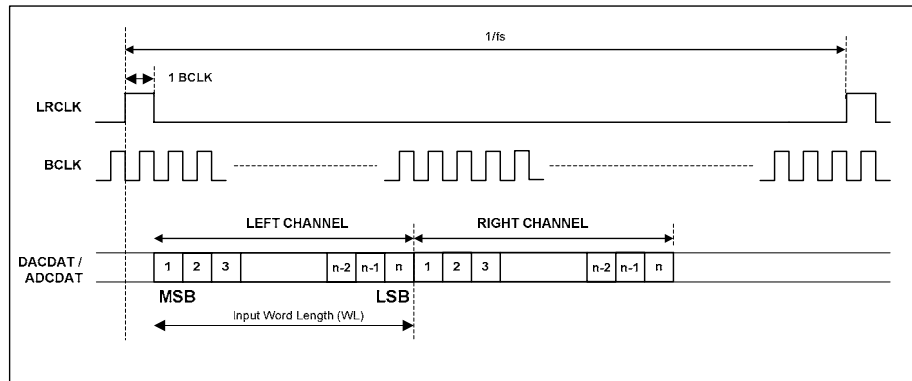


Figure 21 DSP/PCM Mode Audio Interface (mode A, LRP=0, Master)

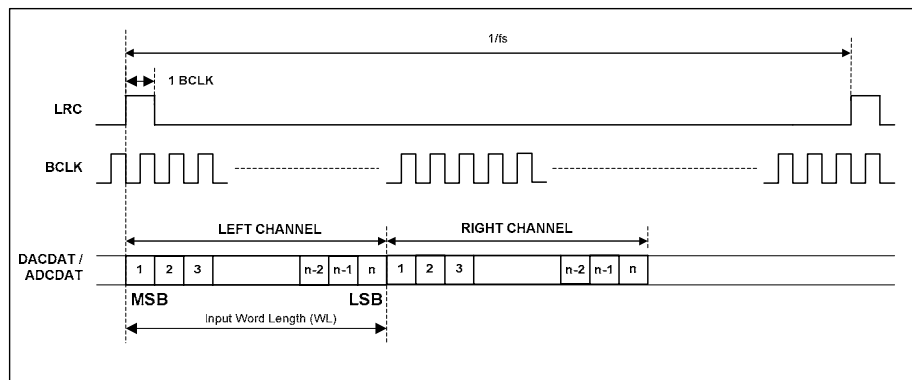


Figure 22 DSP/PCM Mode Audio Interface (mode B, LRP=1, Master)

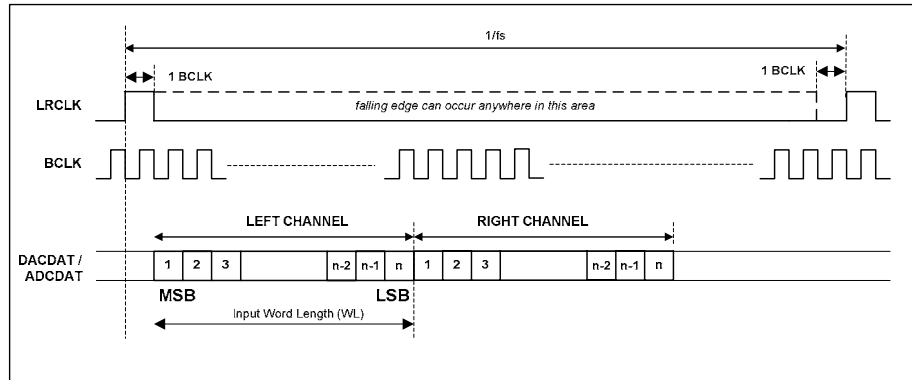


Figure 23 DSP/PCM Mode Audio Interface (mode A, LRP=0, Slave)

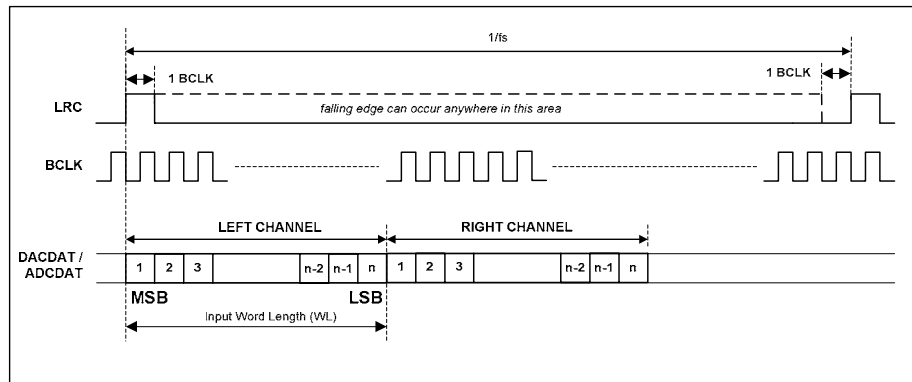


Figure 24 DSP/PCM Mode Audio Interface (mode B, LRP=1, Slave)

AUDIO INTERFACE CONTROL

The register bits controlling the audio interface are summarised below. Note that dynamically changing the software format may cause erroneous operation of the interfaces and is therefore not recommended.

All ADC data is 2's complement. The length of the digital audio data is programmable at 16/20/24 or 32 bits, as shown below. The ADC digital filters process data using 24 bits. If the WM8785 is programmed to output 16 or 20 bit data then it strips the LSBs from the 24 bit data. If the device is programmed to output 32 bits then it packs the LSBs with zeros.

In master mode LRCLK and BCLK are generated on chip. In slave mode they are received from an external source.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--|-----|---------|---------|--|
| R0 (00h) Sample Rate and Digital Audio Interface Format | 6:5 | FORMAT | 10 | Audio Data Format Select 11: DSP Format 10: I ² S Format 01: Left justified 00: Right justified |
| R1 (01h) Digital Audio Interface Format and TDM | 1:0 | WL | 10 | Audio Data Word Length 11: 32 bits (see Note) 10: 24 bits 01: 20 bits 00: 16 bits |
| | 2 | LRP | 0 | right, left and I ² S modes – LRCLK polarity 1 = invert LRCLK polarity 0 = normal LRCLK polarity DSP Mode – A/B select 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B) 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) |
| | 3 | BCLKINV | 0 | BCLK invert bit (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted |
| | 4 | LRSWAP | 0 | Left/Right channel swap 1 = swap left and right DAC data in audio interface 0 = output left and right data as normal |

Table 1 Audio Data Format Control

Note: Right Justified mode does not support 32-bit data. If WL=11 in Right justified mode, the actual word length is 24 bits.

DIGITAL HIGH PASS

The high pass filter can be enabled using the HPFL and HPFR bits (see digital filter characteristics)

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--|-----|-------|---------|--|
| R2(02h) HPfilter , Output disable, Power down, Mono mode | 0 | HPFR | 1 | Digital High Pass Filter, Right Channel 0 = HPF Off 1 = HPF On |
| | 1 | HPFL | 1 | Digital High Pass Filter, Left Channel 0 = HPF Off 1 = HPF On |

Table 2 Oversampling Ratio Selection

The high pass filter should only be disabled for procedures such as DC offset calibration. It should be noted that the output range of the ADC with a DC level applied and HPF disabled is as follows:

Maximum code: 7FDFB0

Minimum code: 802033

DATA OUT PIN DISABLE

To prevent any communication problems on the Audio Interface, the interface can be disabled (DOUT tristated and floating) using the SDODIS bit.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--|-----|--------|---------|---|
| R2(02h) HP Filter , Output disable, Power down, Mono mode | 2 | SDODIS | 0 | DOUT serial data pin disable 0 = DOUT pin enabled 1 = DOUT pin off (high impedance) |

Table 3 Oversampling Ratio Selection

CONTROL INTERFACE

SELECTION OF CONTROL MODE

The WM8785 is controlled by writing to registers through a serial control interface. A control word consists of 16 bits. The first 7 bits (B15 to B9) are address bits that select which control register is accessed. The remaining 9 bits (B8 to B0) are register bits, corresponding to the 9 bits in each control register. The control interface can operate as either a 3-wire or 2-wire MPU interface. The CSB pin is sampled at power-up and selects the interface format. After power-up the pin is available to latch in control data in 3-wire interface mode.

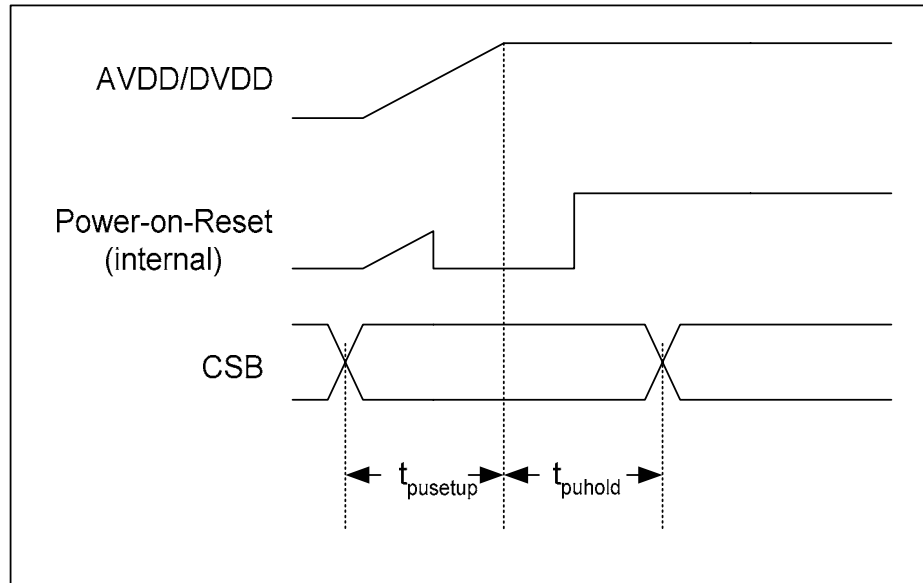


Figure 25 Control Interface Mode Selection

| CSB PIN STATUS | INTERFACE FORMAT |
|----------------|------------------|
| Low | 2 wire |
| High | 3 wire |

Table 4 Control Interface Mode Selection

| SETUP/HOLD | TIME |
|----------------------|-------|
| t _{pusetup} | 250us |
| t _{puhold} | 250us |

Table 5 Control Interface Mode Selection

3-WIRE SERIAL CONTROL MODE

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on CSB latches in a complete control word consisting of the last 16 bits.

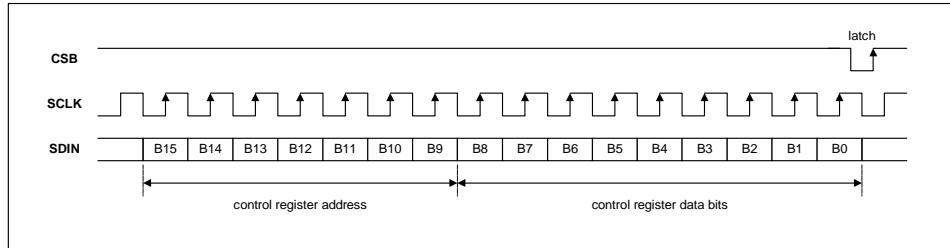


Figure 26 3-Wire Serial Control Interface

2-WIRE SERIAL CONTROL MODE

The WM8785 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the WM8785).

The WM8785 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8785 and the R/W bit is '0', indicating a write, then the WM8785 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1', the WM8785 returns to the idle condition and wait for a new start condition and valid address.

Once the WM8785 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8785 register address plus the first bit of register data). The WM8785 then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8785 acknowledges again by pulling SDIN low.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8785 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

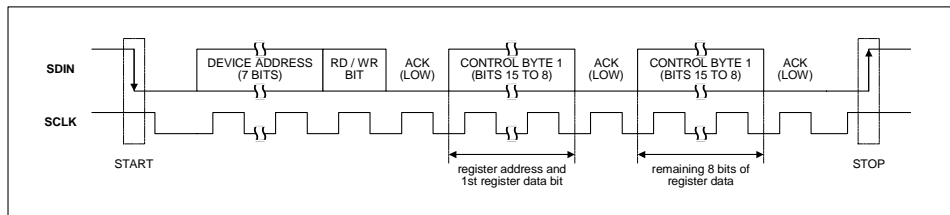


Figure 27 2-Wire Serial Control Interface

The WM8785 device address is 0011010.

TIME DIVISION MULTIPLEXED DATA OUT

The WM8785 can be used to time division multiplex several data channels at once. For example, the diagram below illustrates 4 devices connected to the same TDM bus. While one DOUT pin is driving data, the others will be tri-stated.

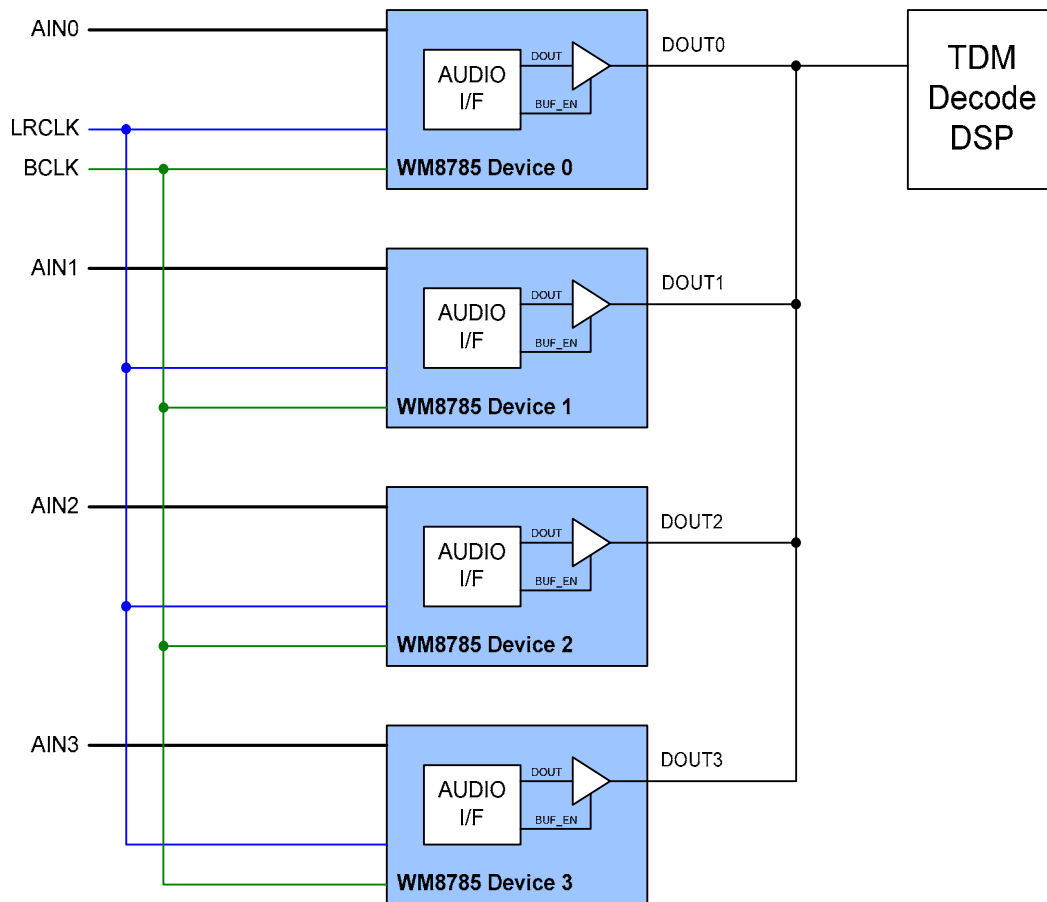


Figure 28 WM8785 in Time Division Multiplexing Setup

Note:

1. TDM is only available in slave mode.
2. Right justified mode is not supported

TDM SELECTION

The figure below indicates how data is multiplexed onto the TDM bus, in left justified mode. This assumes we have 4 devices, and each device has 2 data channels:

- LCHAN = left channel
- RCHAN = right channel

Each channel is allocated 32 BCLKs

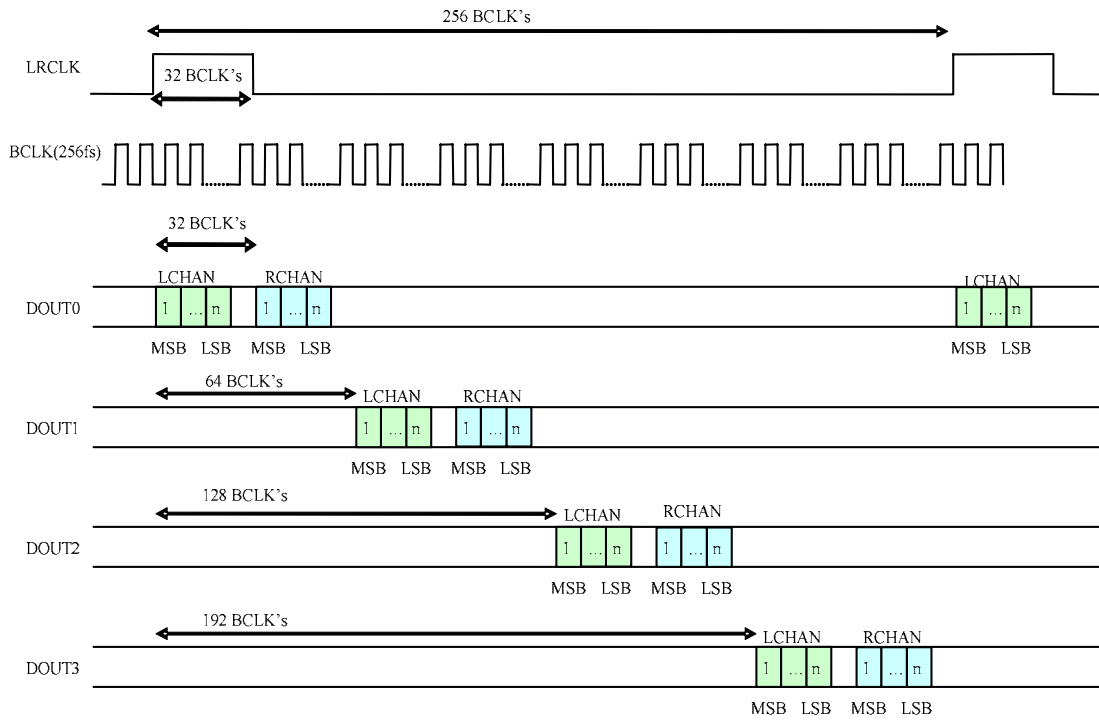


Figure 29 WM8785 in Time Division Multiplexing Left Justified Mode

Up to 4 devices (8 channels) can be supported, which would require 256 BCLKs per sample. (whereas 128 BCLKs will allow only 2 devices, or 4 channels). The table below shows the range of BCLK frequencies required.

| BCLK RATE | DEVICES THAT CAN BE SUPPORTED | OVER-SAMPLE RATIOS SUPPORTED (SET BY OSR) |
|---------------------------|-------------------------------|---|
| 64 fs 128 fs 192 fs | 1 1, 2 1, 2 | Single/dual/quad rates all supported |
| 256 fs | 1, 2, 3, 4 | Single rate only supported |

Table 6 Range of BCLK Frequencies Required

Note: MCLK frequency must always be greater or equal to BCLK frequency

To avoid bus contention all chips on the TDM should be programmed before DOUT is released after power up (DOUT is held at vss for 32 samples after power-up). Alternatively SDODIS should be set while devices are programmed (to tri-state DOUT).

Two registers must be set to enter TDM mode:

- DEVNO[2:0] sets the number of devices which are on the bus
- TDM[2:0] allocates a TDM slot to the device

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--|-----|------------|---------|--|
| R1(h01) Clocking, Sample Rates, Oversampling and Signal Control | 7:5 | DEVNO[2:0] | 000 | Number of TDM Devices 000 = 1 Device 001 = 2 Devices 010 = 3 Devices 011 = 4 Devices |

Table 7 DEVNO

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--|-----|----------|---------|---|
| R2(h02) Clocking, Sample Rates, Oversampling and Signal Control | 8:6 | TDM[2:0] | 000 | Time Division Multiplexing Device Select 000 = Device 0 (no delay) 001 = Device 1 (64 BCLK delay) 010 = Device 2 (128 BCLK delay) 011 = Device 3 (192 BCLK delay) |

Table 8 TDM

Note: When TDM is not required, the register will default to 000 (normal operation)

The figures below indicate TDM mode for I2S and DSP mode A.

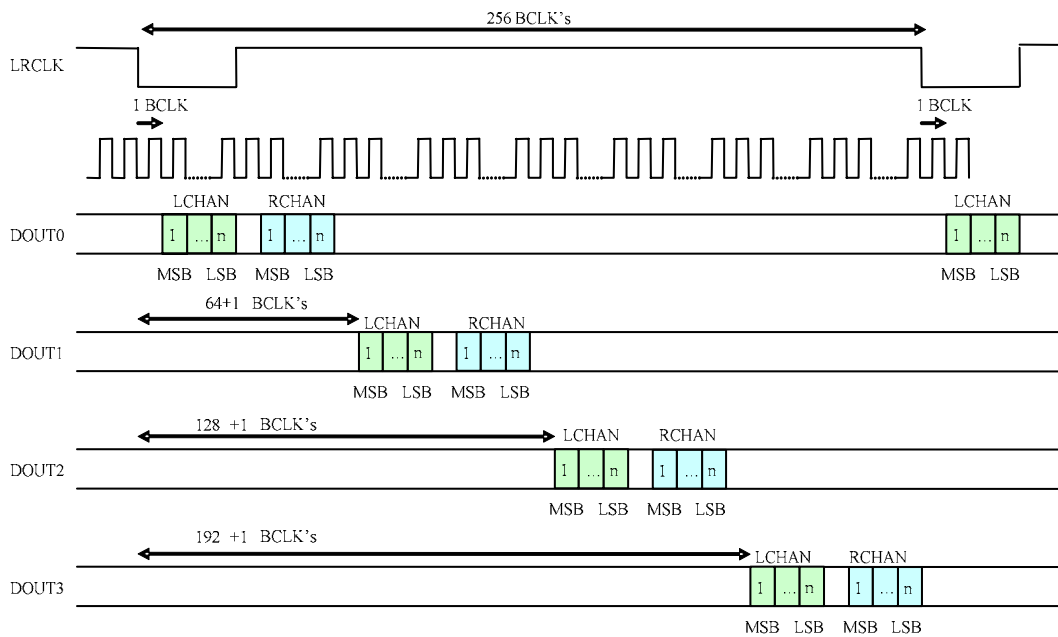


Figure 30 TDM Bus I2S Mode

OVERSAMPLING RATIOS AND SIGMA-DELTA MODULATOR FREQUENCY

For correct operation of the device and optimal performance, the user must select the appropriate ADC modulator oversampling ratio. The oversampling ratio is selected using the OSR[1:0] bits.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------|-----|----------|---------|--|
| R0(h00) Signal Control | 4:3 | OSR[1:0] | 00 | Oversampling Ratio Control 00: Single Rate (128fs) 01: Dual Rate (64fs) 10: Quad Rate (32fs) 11: Not Valid |

Table 9 Oversampling Ratio Selection

The WM8785 can operate at sample rates from 8kHz to 192kHz. The WM8785 uses a sigma-delta modulator that operates at frequencies between 1.024MHz and 6.144MHz

| SAMPLING RATE (LRCLK) | OVERSAMPLING RATIO | SIGMA-DELTA MODULATOR FREQUENCY (MHZ) |
|-----------------------|---------------------|---------------------------------------|
| 8kHz | Single Rate (128fs) | 1.024 |
| 32kHz | Single Rate (128fs) | 4.096 |
| 44.1kHz | Single Rate (128fs) | 5.6448 |
| 48kHz | Single Rate (128fs) | 6.144 |
| 96kHz | Dual Rate (64fs) | 6.144 |
| 192kHz | Quad Rate (32fs) | 6.144 |

Table 10 Sigma-delta Modulator Frequency

MASTER CLOCK AND AUDIO SAMPLE RATES

Master clock frequencies of 128f_s, 192f_s, 256f_s, 384f_s, 512f_s and 768f_s are supported. In slave mode the WM8785 automatically detects the audio sample rate. In Master mode the master clock frequency is selected using MCR[2:0] bits. This is described in table below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------------------------|-----|----------|---------|---|
| R0(h00) Clocking, Sample Rates, | 2:0 | MCR[2:0] | 000 | Master/Slave Selection 000: Slave Mode 001: Master Mode, 128fs 010: Master Mode, 192fs 011: Master Mode, 256fs 100: Master Mode, 384fs 101: Master Mode, 512fs 110: Master Mode, 768fs |

Table 11 Master Clock Frequency

The master clock (MCLK) is used to operate the digital filters and the noise shaping circuits. The WM8785 supports a wide range of master clock frequencies, and can generate many commonly used audio sample rates directly from the master clock. Table 1 shows the recommended master clock frequencies for different sample rates

| SAMPLING RATE (LRCLK) | OVERSAMPLING RATIO | MASTER CLOCK FREQUENCY (MHZ) | | | | | |
|--------------------------|-----------------------|------------------------------|--------|---------|---------|---------|---------|
| | | 128fs | 192fs | 256fs | 384fs | 512fs | 768fs |
| 32kHz | Single Rate | - | - | 8.192 | 12.288 | 16.384 | 24.576 |
| 44.1kHz | Single Rate | - | - | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 48kHz | Single Rate | - | - | 12.288 | 18.432 | 24.576 | 36.864 |
| 96kHz | Dual Rate | - | - | 24.576 | 36.864 | - | - |
| 192kHz | Quad Rate | 24.576 | 36.864 | - | - | - | - |

Table 12 Slave Mode: Recommended Master Clock Frequency Selection

MLCK AND LRCLK PHASE RELATIONSHIP

The WM8785 does not require a specific phase relationship between MLCK and LRCLK. If the relationship between MCLK and LRCLK changes by more than +/-8 BCLKs in a 64 BCLK frame, the WM8785 will attempt to re-synchronise. During re-synchronisation, data samples may be dropped or duplicated.

POWER DOWN CONTROL

The WM8785 can be powered down by setting the PWRDNL and PWRDNR bits. This is described in the table below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------|-----|--------|---------|---|
| R2(02h) Signal control | 3 | PWRDNR | 0 | Power Down Right Channel 0 = Power On 1 = Power Off |
| | 4 | PWRDNL | 0 | Power Down Left Channel 0 = Power On 1 = Power Off |

Table 13 Power Down Control

REGISTER MAP

| REGISTER | ADDRESS | REMARK | BIT8 | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | DEFAULT |
|----------|---------|--|--|-------|--------|--------|---------|-------|------|------|------|-------------|
| R0(00h) | 00_0000 | Sample Rate And Audio IF Format | 0 | 0 | FORMAT | | OSR | | MCR | | | 0_0000_0011 |
| R1(01h) | 00_0001 | Audio IF Format And TDM | 0 | DEVNO | | LRSWP | BCLKINV | LRP | WL | | | 0_0000_1010 |
| R2(02h) | 00_0010 | Signal Control | TDM | | 0 | PWRDNL | PWRDNR | SDDIS | HPFL | HPFR | | 0_0000_0011 |
| R7(07h) | 00_0111 | Reset | Writing to reg 7 will cause software reset | | | | | | | | | 0_0000_0000 |

Table 14 Register Map for Control Interface

Notes:

1. All unused register bits should be set to zero
2. The interface will initiate SWRB whenever R7 is addressed, regardless of the data input.
3. SWRB is released on the next register write or after 4 MCLK cycles (which ever occurs first).
4. Until the SWRB is released, DOUT is forced to zero.
5. DOUT remains zero for a count of 32 sample clocks SWRB is released, this count is driven by MCLK and is independent of any external LRCLK.

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

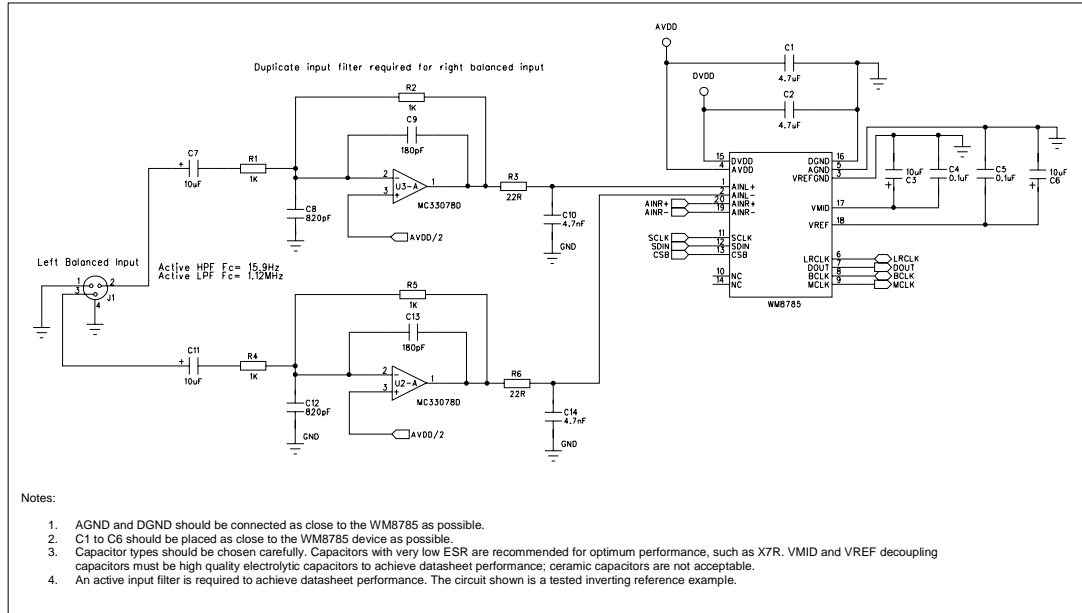
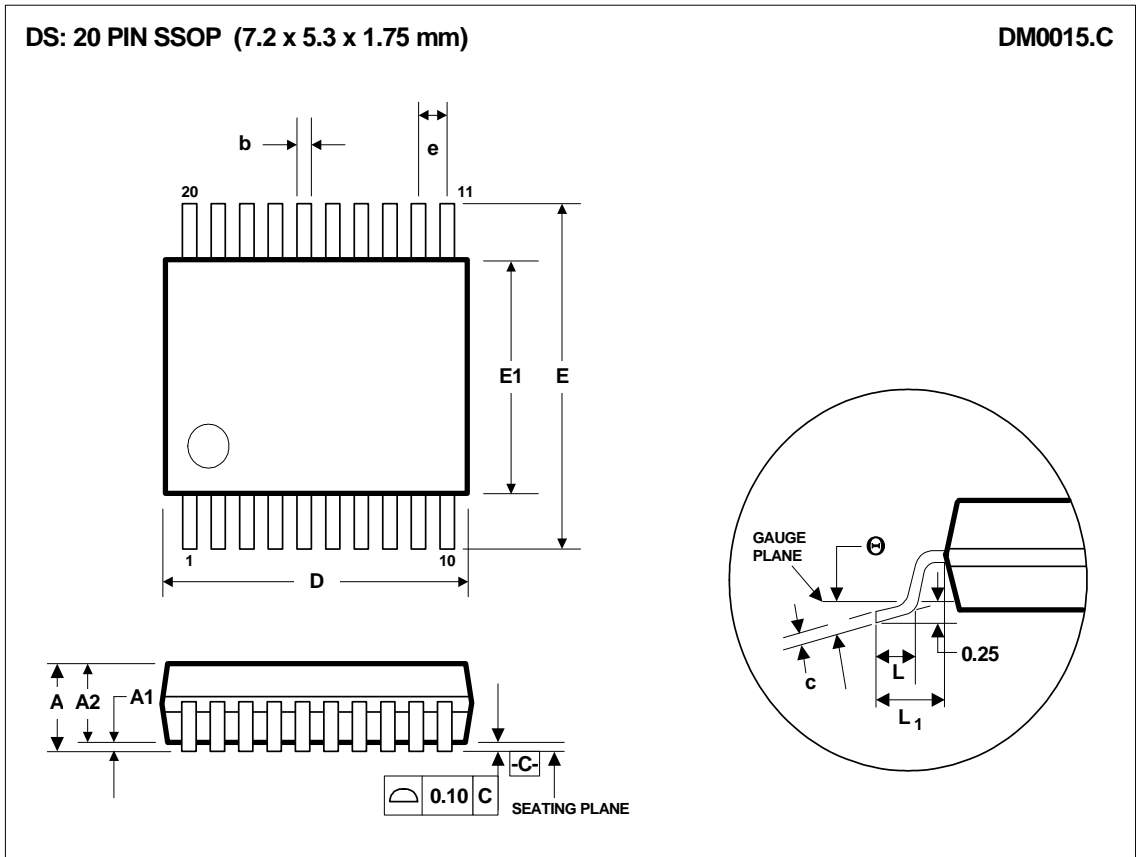


Figure 31 External Component Diagram

PACKAGE DIMENSIONS



| Symbols | Dimensions (mm) | | |
|----------------------|------------------|-------|-------|
| | MIN | NOM | MAX |
| A | ----- | ----- | 2.0 |
| A₁ | 0.05 | ----- | ----- |
| A₂ | 1.65 | 1.75 | 1.85 |
| b | 0.22 | 0.30 | 0.38 |
| c | 0.09 | ----- | 0.25 |
| D | 6.90 | 7.20 | 7.50 |
| e | 0.65 BSC | | |
| E | 7.40 | 7.80 | 8.20 |
| E₁ | 5.00 | 5.30 | 5.60 |
| L | 0.55 | 0.75 | 0.95 |
| L₁ | 1.25 REF | | |
| θ | 0° | 4° | 8° |
| REF: | JEDEC.95, MO-150 | | |

- NOTES:
 A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
 D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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