

REVISIONS																		
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED															
A	Add vendor CAGE number 75569 to the drawing. Add vendor CAGE number 6Y440 to device types 03LX, 03XX, 04LX, and 04XX. Removed vendor CAGE number OBK02 from drawing as approved source of supply. Editorial changes throughout.	1989 OCT 16	<i>M. A. Fyfe</i>															

REV																			
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REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A		A	A	A	A	A	A	A	A	A	
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

PMIC N/A	PREPARED BY <i>James E. Jorgensen</i>	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY <i>Deborah Rensing</i>	MICROCIRCUITS, DIGITAL, MEMORY, CMOS 256K X 1 SRAM, MONOLITHIC SILICON		
	APPROVED BY <i>M. A. Fyfe</i>	SIZE	CAGE CODE	
	DRAWING APPROVAL DATE 22 OCTOBER 1988	A	67268	5962-88725
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5962-E1468

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-M-38510, Inspection lot - class B paragraph) shall be subjected to and pass the internal water vapor test (method 1018 of MIL-STD-883), the frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{CC} = 4.5 V to 5.5 V V _{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Operating supply current <u>1/</u>	I _{CC1}	t _{AVAV} = t _{AVAV} (minimum), V _{CC} = 5.5 V, CE = V _{IL} , all other inputs at V _{IL}	1, 2, 3	01-04		120	mA
				05		135	
Standby power supply current TTL <u>1/</u>	I _{CC2}	CE ≥ V _{IH} , all other inputs < V _{IL} or ≥ V _{IH} , V _{CC} = 5.5 V, f = 0 MHz	1, 2, 3	A11		25	mA
Standby power supply current CMOS <u>1/</u>	I _{CC3}	CE ≥ (V _{CC} - 0.2 V), f = 0 MHz, V _{CC} = 5.5 V, all other inputs < 0.2 V or > (V _{CC} - 0.2 V)	1, 2, 3	A11		20	mA
Input leakage current, any input	I _{ILK}	V _{CC} = 5.5 V, V _{IN} = 0 V to 5.5 V	1, 2, 3	A11		±10	μA
Off-state output leakage current	I _{OLK}	V _{CC} = 5.5 V, V _{IN} = 0 V to 5.5 V	1, 2, 3	A11		±10	μA
Output high voltage	V _{OH}	I _{OUT} = -4.0 mA, V _{CC} = 4.5 V, V _{IL} = 0.8 V, V _{IH} = 2.2 V	1, 2, 3	A11	2.4		V
Output low voltage	V _{OL}	I _{OUT} = 8.0 mA, V _{CC} = 4.5 V, V _{IL} = 0.8 V, V _{IH} = 2.2 V	1, 2, 3	A11		0.4	V
Input capacitance	C _{IN}	V _{IN} = 0 V, f = 1.0 MHz, T _A = +25°C, see 4.3.1c	4	A11		10.0	pF
Output capacitance	C _{OUT}	V _{OUT} = 0 V, f = 1.0 MHz, T _A = +25°C, see 4.3.1c	4	A11		12.0	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{CC} = 4.5 V to 5.5 V V _{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip enable access time	t _{ELQV}	See figure 3 <u>2/</u>	9,10,11	01		35	ns
				02		45	
				03		55	
				04		70	
				05		25	
Read cycle time	t _{AVAV}	See figure 3 <u>2/ 3/</u>	9,10,11	01	35		ns
				02	45		
				03	55		
				04	70		
				05	25		
Address access time	t _{AVQV}	See figure 3 <u>2/ 4/</u>	9,10,11	01		35	ns
				02		45	
				03		55	
				04		70	
				05		25	
Output hold after address change	t _{AVQX}	See figure 3 <u>2/</u>	9,10,11	A11	3.0		ns
Chip enable to output active	t _{ELQX}	See figure 3 <u>2/ 5/ 6/</u>	9,10,11	A11	3.0		ns
Chip disable to output inactive	t _{EHQZ}	See figure 3 <u>2/ 5/ 6/</u>	9,10,11	01,02, 05	0	20	ns
				03	0	25	
				04	0	30	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{CC} = 4.5 V to 5.5 V V _{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip enable to power up	t _{ELPU}	See figure 3 <u>2/ 5/</u>	9,10,11	A11	0		ns
Chip enable to power down	t _{EHPD}	See figure 3 <u>2/ 5/</u>	9,10,11	01		35	ns
				02		45	
				03		55	
				04		70	
				05		25	
Write cycle time	t _{AVAV}	See figure 4 <u>2/</u>	9,10,11	01	35		ns
				02	45		
				03	55		
				04	70		
				05	25		
Write pulse width	t _{WLWH}	See figure 4 <u>2/</u>	9,10,11	01	30		ns
				02	40		
				03	50		
				04	55		
				05	20		
Chip enable to end of write	t _{ELEH}	See figure 4 <u>2/</u>	9,10,11	01	30		ns
				02	40		
				03	50		
				04	55		
				05	20		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{CC} = 4.5 V to 5.5 V V _{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit	
					Min	Max		
Data setup to end of write	t _{DVWH}	See figure 4	2/	9,10,11	01, 02	20	ns	
					03, 04	25		
					05	16		
Data hold after end of write	t _{WHDX}	See figure 4	2/	9,10,11	A11	2.0	ns	
Address setup to end of write	t _{AVWH}	See figure 4	2/	9,10,11	01	30	ns	
					02	40		
					03	50		
					04	55		
					05	20		
Address setup to beginning of write	t _{AVWL}	See figure 4	2/	9,10,11	A11	0	ns	
	t _{AVEL}	See figure 4	2/	9,10,11	A11	2.0	ns	
Address hold after end of write	t _{WHAV}	See figure 4	2/	9,10,11	A11	5.0	ns	
Write enable to output disable	t _{WLQZ}	See figure 4	2/ 5/ 6/	9,10,11	01, 05	0	15	ns
					02	0	20	
					03	0	25	
					04	0	30	
Output active after end of write	t _{WHQX}	See figure 4	2/ 5/ 6/ 7/	9,10,11	A11	0	ns	

- 1/ I_{CC} is dependent upon output loading and cycle rate. The specified values apply with output(s) unloaded.
- 2/ AC measurements assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading of 30 pF load capacitance. Output timing reference is 1.5 V. See figure 5.
- 3/ For read cycles 1 and 2, WE is high for entire cycle.
- 4/ Device is continuously selected, CE low.
- 5/ Parameter if not tested, shall be guaranteed to the limits specified in table I.
- 6/ Measured ±500 mV from steady-state output voltage. Load capacitance is 5.0 pF.
- 7/ If WE is low when CE goes low, the output remains in the high impedance state.

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Device types	01 through 05	
Case outlines	L	X
Terminal number	Terminal symbol	
1	A	A
2	A	A
3	A	A
4	A	NC
5	A	A
6	A	A
7	A	A
8	A	A
9	A	A
10	Q	A
11	WE	Q
12	V _{SS}	NC
13	CE	WE
14	D	V _{SS}
15	A	CE
16	A	D
17	A	A
18	A	NC
19	A	A
20	A	A
21	A	A
22	A	A
23	A	A
24	V _{CC}	A
25	---	A
26	---	NC
27	---	A
28	---	V _{CC}

NC = No connection

FIGURE 1. Terminal connections.

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Device types 01 through 05

\overline{CE}	\overline{WE}	Mode	I/O	Power
H	X	Not selected	High Z	Standby
L	L	Write	DIN	Active
L	H	Read	DOUT	Active

H = Logic "1" state
L = Logic "0" state
X = Don't care

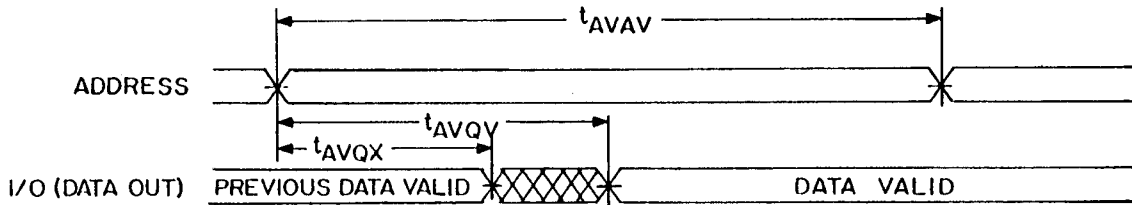
FIGURE 2. Truth table.

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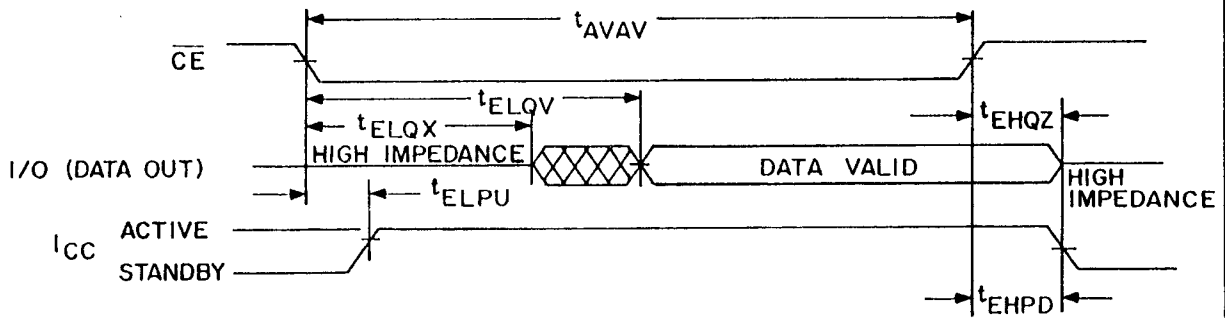
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READ CYCLE NO. 1 (\overline{WE} HIGH, \overline{CE} LOW) (See notes 1, 2, and 3)



READ CYCLE NO. 2 (\overline{WE} HIGH) (See notes 1 and 2)



NOTES:

1. \overline{WE} is high for entire cycle.
2. \overline{CE} and \overline{WE} must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in monotonic fashion.
3. Device is continuously selected, \overline{CE} low.

FIGURE 3. Read cycle timing diagrams.

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WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED) (See notes 1 and 2)

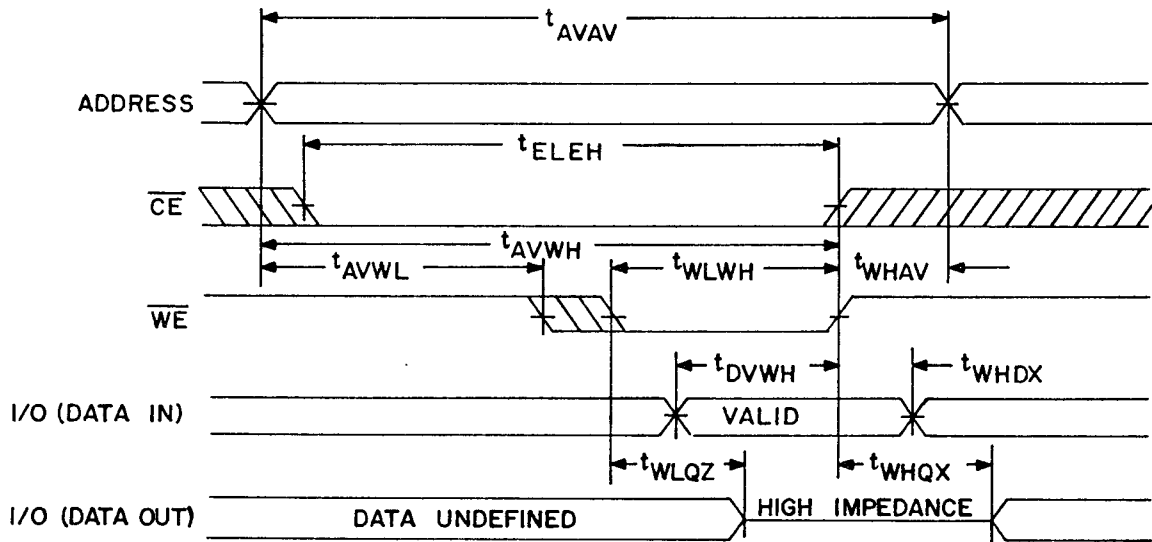


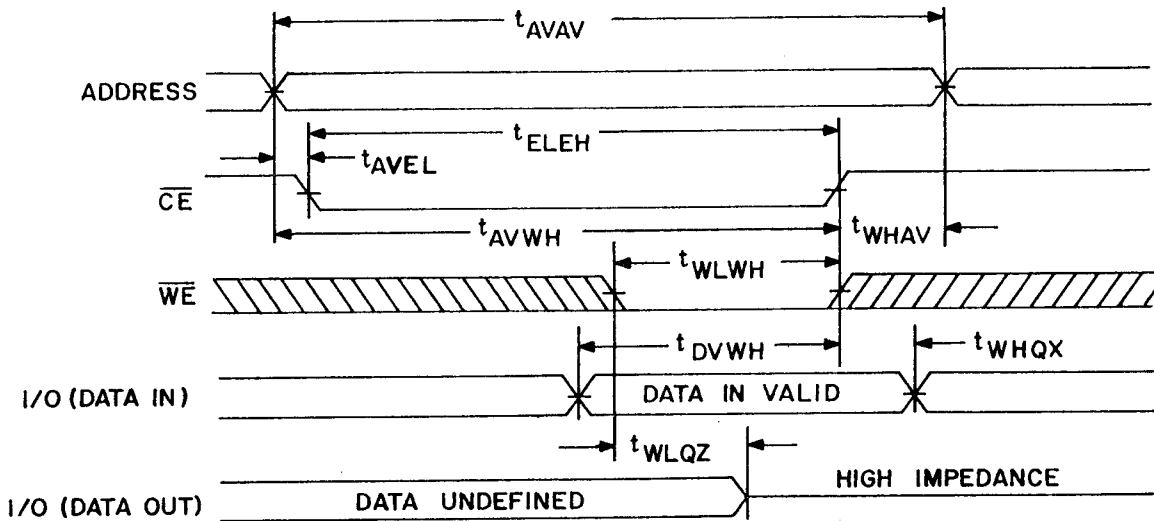
FIGURE 4. Write cycle timing diagrams.

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WRITE CYCLE NO. 2 (\overline{CE} CONTROLLED) (See notes 1 and 2)



NOTES:

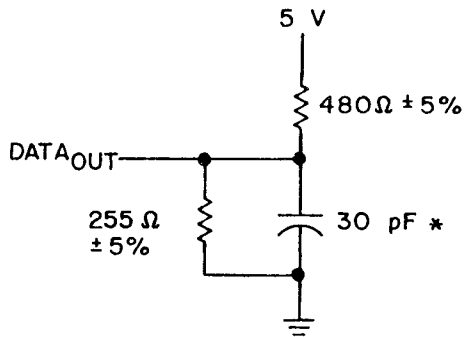
1. \overline{CE} and \overline{WE} must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in monotonic fashion.
2. \overline{CE} and \overline{WE} must be $\geq V_{IH}$ during address transitions.

FIGURE 4. Write cycle timing diagrams - Continued.

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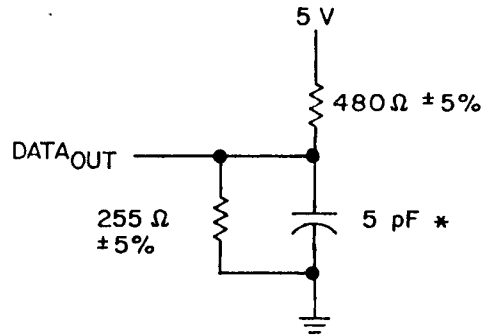
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CIRCUIT A

Output load

*Including scope and jig
(minimum values)



CIRCUIT B

(for t_{ELOQ} , t_{WLQZ}
 t_{EHQX} , t_{WHQX})

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 5. Output load circuits.

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3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance.
- d. Subgroups 7 and 8 tests shall include verification of the truth table.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8

* PDA applies to subgroups 1 and 7.
 ** See 4.3.1c.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

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6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>
5962-8872501LX	61772 66301 6Y440 75569	IDT71257535CB EDI81256C35QB MT5C2561C-35 P4C1257-35CMB
5962-8872501XX	66301 6Y440 75569	EDI81256C35LB MT5C2561EC-35 P4C1257-35LMB
5962-8872502LX	61772 66301 6Y440 75569	IDT71257545CB EDI81256C45QB MT5C2561C-45 P4C1257-45CMB
5962-8872502XX	66301 6Y440 75569	EDI81256C45LB MT5C2561EC-45 P4C1257-45LMB

See footnote on next page.

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Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>
5962-8872503LX	61772 66301 6Y440 75569	IDT71257555CB EDI81256C55QB MT5C2561C-55 P4C1257-55CMB
5962-8872503XX	66301 6Y440 75569	EDI81256C55LB MT5C2561EC-55 P4C1257-55LMB
5962-8872504LX	61772 66301 6Y440 75569	IDT71257570CB EDI81256C70QB MT5C2561C-70 P4C1257-55CMB
5962-8872504XX	66301 6Y440 75569	EDI81256C70LB MT5C2561EC-70 P4C1257-55LMB
5962-8872505LX	6Y440 61772 75569	MT5C2561C-25 IDT71257S25CB P4C1257-25CMB
5962-8872505XX	6Y440 75569	MT5C2561EC-25 P4C1257-25LMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

Vendor name and address

61772

Integrated Device Technology Incorporated
3236 Scott Boulevard
Santa Clara, CA 95052

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Vendor CAGE
number

Vendor name
and address

66301

Electronic Designs Incorporated
42 South Street
Hopkinton, MA 01748

6Y440

Micron Technology Incorporated
2805 East Columbia Road
Boise, ID 83706

75569

Performance Semiconductor Corporation
610 East Weddell Drive
Sunnyvale, CA 94089

**STANDARDIZED
MILITARY DRAWING**

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

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