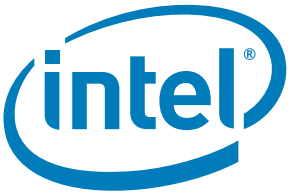

82573 Family of GbE Controllers

Datasheet

Product Features

- **PCIe***
  - — x1 PCIe* interface on ICH7 or MCH devices
  - — Peak bandwidth: 2 Gb/s per direction
  - — Power management
  - — High bandwidth density per pin
- **MAC**
  - — Optimized transmit and receive queues
  - — IEEE 802.3x compliant flow control with software controlled pause times and threshold values
  - — Caches up to 64 packet descriptors per queue
  - — Programmable host memory receive buffers (256 bytes to 16 KB) and cache line size (16 bytes to 256 bytes)
  - — 32 KB configurable transmit and receive FIFO buffer
  - — Mechanism available for reducing interrupts generated by transmit and receive operation
  - — Descriptor ring management hardware for transmit and receive
  - — Optimized descriptor fetching and write-back mechanisms
  - — Wide, pipelined internal data path architecture
- **PHY**
  - — Integrated PHY for 10/100/1000 Mb/s full and half duplex operation
  - — IEEE 802.3ab auto negotiation support
  - — IEEE 802.3ab PHY compliance and compatibility
  - — DSP architecture implements digital adaptive equalization, echo cancellation, and cross-talk cancellation
- **Host Offloading**
  - — Transmit and receive IP, TCP and UDP checksum off-loading capabilities
  - — Transmit TCP segmentation, IPv6 offloading, and advanced packet filtering
  - — IEEE 802.1q VLAN support with VLAN tag insertion, stripping and packet filtering for up to 4096 VLAN tags
  - — Descriptor ring management hardware for transmit and receive
- **Manageability**
  - — Intel® Active Management Technology (Intel® AMT) support (82573E only)
  - — Alerting Standards Format 2.0 and advanced pass through support (82573E/V only)
  - — Boot ROM Preboot eXecution Environment (PXE) Flash interface support
  - — Compliance with PCI Power Management 1.1 and Advanced Configuration and Power Interface (ACPI) 2.0 register set compliant
  - — Wake on LAN support
- **Additional**
  - — Three activity and link indication outputs that directly drive LEDs
  - — Programmable LEDs
  - — Internal PLL for clock generation that can use a 25 MHz crystal
  - — Power saving feature for the 82573L. During the L1 and L2 link states, the 82573L asserts the Clock Request signal (CLKREQ#) to indicate that its PCIe* reference clock can be gated
  - — On-chip power control circuitry
  - — Loopback capabilities
  - — JTAG (IEEE 1149.1) Test Access Port (TAP) built in silicon
- **Technology**
  - — Lead-free 196-pin Thin and Fine Pitch Ball Grid Array (TF-BGA) package
  - — Operating temperature: 0° C to 70° C (with external regulators)
  - — Operating temperature: 0° to 55° C (with on-die 2.5V regulator)
  - — Storage temperature -40° C to 125° C

Order Number: 315514-002
Revision 2.5

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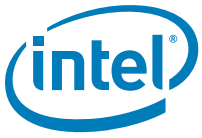
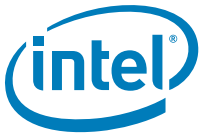


Tables

Revision History

Date	Revision	Description
Jan 2007	2.5	Updated the PHY_REF signal description in Section 2.6.
Oct 2006	2.4	Added document order number. Corrected the AUX_PWR pin (C6) description for the 82573E/V. Updated Table 18 “Crystal Specifications”. Updated the visual pin assignments for the 82573L. Major edit all sections.
August 2006	2.3	Chapter 1, Introduction, corrected note. 3.5.1, Removed line item 3.5.2, Corrected title Heading
June 2006	2.2	Revised Section 3.3, 'PCIe Miscellaneous Signals", updated Intel logo.
Feb 2006	2.1	Added Section 5.2, 'Thermal Specifications".”
Sept 2005	2.0	Integrated 82573L information into this document.
June 2005	1.5	Initial public release.



1.0 Introduction

Note: Unless specifically noted, 82573 refers to the Intel® 82573E, 82573V and 82573L GbE controllers.

82573 GbE controllers are single, compact components with integrated Gigabit Ethernet Media Access Control (MAC) and Physical Layer (PHY) functions. These devices use PCIe* architecture (Revision 1.0a). For desktop, workstation, and value server network designs with critical space constraints, the 82573 enables a GbE implementation in a very small area.

The 82573 provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab, respectively). In addition to managing MAC and PHY Ethernet layer functions, the 82573 manages PCIe* packet traffic across its transaction, link, and physical and logical layers.

The 82573E contains a dedicated microcontroller for manageability with an on-board Intel® Active Management Technology (Intel® AMT) enabling network. This enables manageability implementations required by information technology personnel for out-of-band management, remote troubleshooting and recovery, asset management, and non-volatile storage. Intel® AMT is the first step towards a complete Intel® Cross-Platform Manageability Program (Intel® CPMP), which is a business and technology initiative to deliver consistent management capabilities, protocols, and interfaces across all Intel platforms.

The 82573E and 82573V GbE controllers have an integrated System Management Bus (SMBus) port enabling industry standards, such as the Alert Standard Forum (ASF) 2.0. With SMBus, management packets can be routed to or from a management processor. In addition, integrated ASF 2.0 circuitry provides alerting and capabilities with standardized interfaces.

The 82573 with PCIe* architecture is designed for high performance and low memory latency. The device is optimized to connect to a system I/O Control Hub (ICH7) using one PCIe* lane. Alternatively, the 82573 is able to connect to a Memory Control Hub (MCH) device with a PCIe* interface.

Wide internal data paths eliminate performance bottlenecks by efficiently handling large address and data words. The 82573 efficiently handles packets with minimum latency by combining a parallel and pipelined logic architecture optimized for GbE and independent transmit and receive queues. The 82573 also includes advanced interrupt handling features and uses efficient ring buffer descriptor data structures, with up to 64 packet descriptors per queue cached on chip. A 32-KB on-chip packet buffer maintains superior performance. In addition, using hardware acceleration, the 82573 offloads tasks from the host (for example, TCP/UDP/IP checksum calculations and TCP segmentation).

The 82573L features low power management. During the L1 and L2 link states, the 82573L asserts the Clock Request signal (CLKREQ#) to indicate that its PCIe* reference clock can be gated.

The 82573 is packaged in a 15 mm X 15 mm, 196-Ball Grid Array (BGA).

1.1 Document Scope

This document contains targeted datasheet specifications for the 82573 GbE controller, including signal descriptions, DC and AC parameters, packaging data, and pinout information.

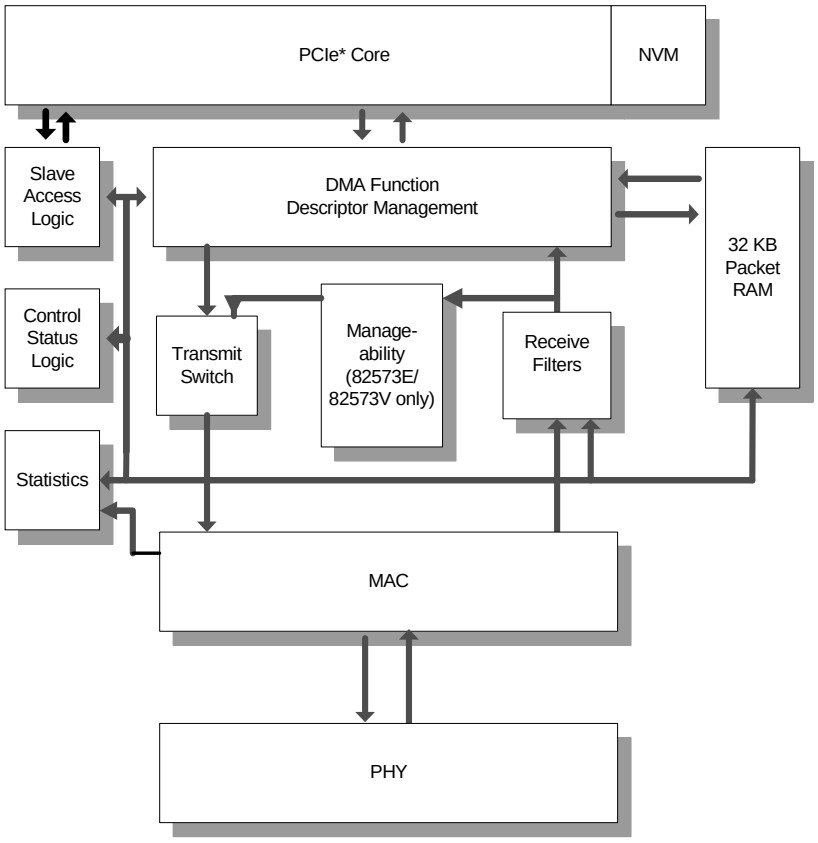
1.2 Reference Documents

This application assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- IEEE Standard 802.3, 2000 Edition. Institute of Electrical and Electronics Engineers (IEEE).
- PCI Express Base Specification, Revision 1.0a. PCI Special Interest Group.
- PCI Express Card Electromechanical Specification, Revision 1.0a. PCI Special Interest Group.
- PCI Bus Power Management Interface Specification, Revision 1.1. PCI Special Interest Group.
- Intel Ethernet Controller Timing Device Selection Guide. Intel Corporation.
- 82573 NVM Map and Programming Information Guide. Intel Corporation.
- 82573/82562 Dual Footprint Design Guide. Intel Corporation.
- PCIe* Family of Gigabit Ethernet Controllers Software Developer's Manual. Intel Corporation.
- 82573 Family GbE Controllers Specification Update. Intel Corporation.

1.3 82573 Architecture

Figure 1. 82573 Block Diagram



Note: The 82573L does not support manageability.

1.4 Product Codes for the 82573

Device	Top Marking	Leaded/ Unleaded	Product Features
82573E	RC82573E	Leaded	82573E with Intel® AMT includes: • Intel® AMT • ASF 2.0 • Advanced Pass Through (APT)
82573E	PC82573E	Lead Free	82573E with Intel® AMT includes: • Intel® AMT • ASF 2.0 • APT
82573V	RC82573V	Leaded	82573V Baseline includes: • ASF 2.0 • APT
82573V	PC82573V	Lead Free	82573V Baseline includes: • ASF 2.0 • APT
82573L	RC82573L	Leaded	82573L: • Low-power • No management
82573L	PC82573L	Lead Free	82573L: • Low-power • No management

2.0 Signal Descriptions

2.1 Signal Type Definitions

The signals of the 82573 are electrically defined as follows:

Name	Definition
I	Input Standard input only digital signal.
O	Output Standard output only digital signal.
I/O	I/O Standard I/O digital signal.
TS	Tri-state Bi-directional three-state digital input/output signal.
OD	Open Drain Wired-OR with other agents. The signaling agent asserts the open drain signal, but the signal is returned to the inactive state by a weak pull-up resistor. The pull-up resistor might require two or three clock periods to fully restore the signal to the de-asserted state.
A	Analog PCIe, SerDes, or PHY analog signal.
P	Power Power connection, voltage reference, or other reference connection.

Name	Definition
B	Input Bias
PU	Pull Up This signal requires a pull-up resistor.
PD	Pull Down This signal requires a pull-down resistor.

2.2 PCIe* Data Signals

Signal	Type	Name and Function
PE_CLKn PE_CLKp	A(In)	PCIe Differential Reference Clock The reference clock is furnished by the system and has a 300 ppm frequency tolerance. It is used as reference clock for PCIe transmit and receive circuitry and is used by the PCIe core PLL to generate 125 MHz and 250 MHz clocks for the PCIe* core logic.
PE_T0n PE_T0p	A(0ut)	PCIe* Serial Data Output These signals connect to corresponding PERn and PERp signals on a system motherboard or a PCIe* connector. Series AC coupling capacitors are required at the 82573 device end. The PCIe* differential outputs are clocked at 2.5 Gb/s.
PE_R0n PE_R0p	A(In)	PCIe Serial Data Input These signals connect to corresponding PETn and PETp signals on a system motherboard or a PCIe* connector. The PCIe* differential inputs are clocked at 2.5 Gb/s.

2.3 PCIe* Miscellaneous Signals

Signal	Type	Name and Function
PE_RST#	I	Reset This signal indicates whether or not the PCIe* power and clock are available.
PE_WAKE#	OD	Wake This signal is driven to zero when it receives a wake-up packet and either the PME enable bit of the Power Management Control/Status Register is set to 1b or the Advanced Power Management enabled bit of the Wake Up Control Register equals 1b.
AUX_ PRESENT (AUX_PWR)[1]	I	Auxiliary Power Present AUX_PRESENT must be pulled up to 3.3V standby power if the 82573 is powered from standby supplies. This signal must be pulled down if auxiliary power is not used.
CLKREQ# (82573L only)	OD	Clock Request. The Clock Request (CLKREQ#) signal is located at ball P9 of the 82573L. When it is sampled high, this open-drain signal alerts the system that the 82573L does not need the PCIe* differential reference clock. During normal operation, the 82573L keeps CLKREQ# asserted (low), and the system supplies this clock to the device on the PE_CLKp and PE_CLKn signals. The 82573L deasserts CLKREQ# (high) when it is in an electrical idle state (L1 and L2), and the system might choose to continue supplying the reference clock or gate it conserving platform power. The CLKREQ# signal should be connected to the clock driver that supplies the 82573L PCIe* clock. If other devices use the same CLKREQ# signal, a pull-up resistor should be used to ensure that no device pulls this signal low when it is powered off.

1. This signal is used in all three devices and has the same functionality but is denoted as AUX_PRESENT in the 82573E/V and AUX_PWR in the 82573L.

2.4 Non-Volatile Memory Interface Signals

Signal	Type	Name and Function
NVM_SI	I/O	NVM Serial Data Output The data output pin is used for input to the non-volatile memory device. This pin is occasionally used as input during arbitration. This signal has an internal pull-up resistor.
NVM_SO	I	NVM Serial Data Input The data input pin is used for output from the non-volatile memory device to the 82573. This signal has an internal pull-up resistor.
NVM_SK	O TS	NVM Serial Clock The serial clock provides the clock rate for the memory interface.
NVM_CS#	I/O	NVM Chip Enable This signal is used to enable the device. This signal has an internal pull-up resistor.
NVM_REQ	O	NVM Arbitration Request. This signal is used to request use of the NVM interface.
NVM_PROT	I/PU	NVM Protection Enable. This pin should be connected to ground to disable NVM protection; otherwise, NVM protection is enabled. This signal has an internal pull-up resistor.
NVM_TYPE	I/PU	NVM Device Type If the device uses a Flash, this pin should be connected to a pull-down resistor. If the 82573 is connected to an EEPROM, this pin can be connected to an external pull-up resistor. This signal has an internal pull-up resistor of 30 KΩ ±50%.
NVM_SHARED#	I/PU	NVM Shared Enable This pin should be connected to a pull-down resistor to enable sharing of SPI Flash with ICH. This signal has an internal pull-up resistor.

2.5 Miscellaneous Signals

2.5.1 Reset and Power-down Signals

Signal	Type	Name and Function
LAN_PWR_GOOD	I	LAN Power Good This signal indicates that stable power is available to the 82573. When the signal is low, LAN_PWR_GOOD acts as a master reset of the entire device. LAN_PWR_GOOD should be connected to a power supervisor driven from auxiliary power. The signal should go active approximately 80 ms after all power rails are within their operating ranges. A PCIe* reset must only occur after LAN Power Good is active.
DEVICE_OFF#	I	Device Off This asynchronously disables the 82573, including voltage regulator control outputs if selected in external control.

2.5.2 System Management Bus (SMBus) Signals[1]

Note: The signals listed in the following table should not be connected when using an 82573L. Refer to the *82573/82562 Dual Footprint Design Guide* reference schematics for more information.

Signal	Type	Name and Function
SMB_CLK	I/O	SMBus Clock The SMBus Clock signal is an open drain signal for the serial SMBus interface.
SMB_DAT	I/O	SMBus Data The SMB Data signal is an open drain signal for the serial SMBus interface.
SMB_ALRT#/ ASF_PWR_ GOOD	I/O	SMBus Alert/PCI Power Good The SMBus Alert signal is an open drain signal for serial SMBus interface. In ASF mode, this signal acts as the PCI Power Good input signal.

2.5.3 LED Signals

Signal	Type	Name and Function
LED0#	O	LED0 This pin provides a signal for programmable LED indication.
LED1#	O	LED1 This pin provides a signal for programmable LED indication.
LED2#	O	LED2 This pin provides a signal for programmable LED indication.

2.5.4 Other Signals

Signal	Type	Name and Function
THERMn THERMp	O	Thermal Test Pins These pins are used for thermal testing. They can be connected to test points.
FUSEV	P	Fuse Supply This should be connected to 2.5V for normal operation.

1. The 82573L does not support the System Management Bus (SMBus).

2.6 PHY Analog and Crystal Signals

Signal	Type	Name and Function
MDI0n MDI0p	A	Media Dependent Interface [0] 1000BASE-T: In MDI configuration, MDIp0/MDIn0 corresponds to BI_DA+/-, and in MDI-X configuration, MDIp0/MDIn0 corresponds to BI_DB+/-. 100BASE-TX: In MDI configuration, MDIp0/MDIn0 is used for the transmit pair, and in MDI-X configuration, MDIp0/MDIn0 is used for the receive pair. 10BASE-T: In MDI configuration, MDIp0/MDIn0 is used for the transmit pair, and in MDI-X configuration, MDIp0/MDIn0 is used for the receive pair.
MDI1n MDI1p	A	Media Dependent Interface [1] 1000BASE-T: In MDI configuration, MDIp1/MDIn1 corresponds to BI_DB+/-, and in MDI-X configuration, MDIp1/MDIn1 corresponds to BI_DA+/-. 100BASE-TX: In MDI configuration, MDIp1/MDIn1 is used for the receive pair, and in MDI-X configuration, MDIp1/MDIn1 is used for the transmit pair. 10BASE-T: In MDI configuration, MDIp1/MDIn1 is used for the receive pair, and in MDI-X configuration, MDIp1/MDIn1 is used for the transmit pair.
MDI2n MDI2p	A	Media Dependent Interface [2] 1000BASE-T: In MDI configuration, MDIp2/MDIn2 corresponds to BI_DC+/-, and in MDI-X configuration, MDIp2/MDIn2 corresponds to BI_DD+/-. 100BASE-TX: Unused. 10BASE-T: Unused.
MDI3n MDI3p	A	Media Dependent Interface [3] 1000BASE-T: In MDI configuration, MDIp3/MDIn3 corresponds to BI_DD+/-, and in MDI-X configuration, MDIp3/MDIn3 corresponds to BI_DC+/-. 100BASE-TX: Unused. 10BASE-T: Unused.
PHY_REF	A	Reference Input This signal is used as the analog reference input for the PHY. It should be connected to a pull-down, 4.99 K Ω, 1% resistor.
XTAL1	I	Crystal One The Crystal One pin is a 25 MHz input signal. It should be connected to a parallel resonant crystal with a frequency tolerance of 30 ppm. The other end of the crystal should be connected to XTAL2.
XTAL2	O	Crystal Two Crystal Two is the output of an internal oscillator circuit used to drive a crystal into oscillation.

2.7 Test Signals

2.7.1 MAC Test Signals

Signal	Type	Name and Function
TEST_EN	I	Factory Test Pin A 1 KΩ pull-down resistor should be attached to ground from this pin for normal operation.
ALT_CLK125	NC	Alternate 125 MHz Clock This signal should not be connected. This signal has an internal pull-up resistor.
JTAG_TCK	I	JTAG Test Access Port Clock This signal has an internal pull-down resistor.
JTAG_TDI	I	JTAG Test Access Port Test Data In This signal has an internal pull-up resistor.
JTAG_TDO	O/OD	JTAG Test Access Port Test Data Out
JTAG_TMS	I	JTAG Test Access Port Mode Select This signal has an internal pull-up resistor.
CLK_VIEW	NC	Clock View The Clock View signal is an output for the clock signals required for IEEE testing. This signal has an internal pull-up resistor.
TEST[16:0] for the 82573E/V TEST[10:0] for the 82573L	Rsvd	Test Pin[16:0] These test pins are for the 82573E/V only. These signals have internal pull-up resistor. For normal operation, these pins should be left unconnected. Test Pin[10:0] These test pins are for the 82573L only. These signals have internal pull-up resistor. For normal operation, these pins should be left unconnected.

2.7.2 PHY Test Signals

Signal	Type	Name and Function
PHY_HSDACn PHY_HSDACp (82573E/V) PHY_TESTn PHY_TESTp (82573L only)[1]	A(Out)	PHY Differential Test Port These signals are used for factory test purposes only.
PHY_TSTPT		PHY Test Port This signal is used for factory test purposes only. This pin must be left unconnected for normal operation.

1. These signals are used in all three devices and have the same functionality but are denoted as PHY_HSDACn and PHY_HSDACp in the 82573E/V and PHY_TESTn and PHY_TESTp in the 82573L.

2.7.3 Other Test Signals

Signal	Type	Name and Function
SDP[3:0]	NC	These signals are used for factory test purposes only and have internal pull-up resistors.

2.8 Power Signals

2.8.1 Power Support Signals

Signal	Type	Name and Function
CTRL_25	P	2.5V Control This is the voltage control signal for external 2.5V. It is only active when the EN25REG signal is low (disabled). When external 2.5V and 1.2V supplies are used, CTRL_25 can be left floating or can be connected to ground through a 3.3 KΩ resistor.
CTRL_12	P	1.2V Control This is the voltage control signal for external 1.2V. When external 2.5V and 1.2V supplies are used, CTRL_12 can be left floating or can be connected to ground through a 3.3 KΩ resistor.
EN25REG	I/PU	Enable 2.5V Regulator When this signal is high, the internal 2.5V regulator is enabled. When it is low, the internal 2.5V regulator is disables and the CTRL_25 signal is active. This signal should be pulled up to the 3.3V power rail.

2.8.2 Digital and Analog Power Supply Signals

Signal	Type	Name and Function
VCC33	P	3.3V Power Supply This signal is used for I/O circuits.
VCC25	P	2.5V Analog Power Supply These signals are used for PHY analog, PHY I/O, PCIe* analog and phase lock loop circuits. All 2.5V pins should be connected to a single power supply.
VCC12	P	1.2V Digital Power Supply These signals are used for core digital, PHY digital, PCIe* digital and clock circuits. All 1.2V pins should be connected to a single power supply.
IREG25_IN (82573E/V) VCC3.3_REG25 (82573L only)[1]	P	IREG25_IN 3.3V power supply for internal 2.5V regulator. When external 2.5V and 1.2V supplies are used, IREG25_IN should be connected to 3.3V.
VCC25_OUT	P	VCC25_OUT 2.5V output supply from internal power supply. When external 2.5V and 1.2V supplies are used, VCC25_OUT can be left floating.

1. This signal is used in all three devices and has the same functionality but is denoted as IREG25_IN for the 82573E/V and VCC3.3_REG25 for the 82573L.

2.9 Grounds and No Connects

Signal	Type	Name and Function
VSS	P	Ground These signals connect to ground. VSS is also referred to as GND.
NC		No Connect These pins are reserved by Intel and might have factory test functions. For normal operation, do not connect any circuitry to these pins. Do not connect pull-up or pull-down resistors.

3.0 Voltage, Temperature, and Timing Specifications

3.1 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Symbol	Parameter	Min	Max	Unit
Tstg	Storage temperature	-40	125	°C
VCC (3.3)	DC supply voltage on 3.3V pins with respect to VSS	-0.3	6.6	V
VCC (2.5)	DC supply voltage on 2.5V pins with respect to VSS[2]	-0.3	5.0	V
VCC (1.2)	DC supply voltage on 1.2V pins with respect to VSS[b]	-0.3	2.4	V
Vin	Input voltage (digital inputs)	-1.0	VCC (3.3) + 0.3 (less than 6.6 V)	V
AVin	Analog input voltage (digital inputs)	-1.0	VCC (2.5) + 0.3 (less than 5.0 V)	V
R_{PUD}	Pull-up/pull-down Resistor Value	15	50	KΩ

1. Maximum ratings are referenced to ground (VSS). Permanent device damage is likely to occur if the ratings in this table are exceeded for an indefinite duration. These values should not be used as the limits for normal device operations. This specification is not guaranteed by design or simulations.
2. During normal device power up and power down, the 2.5V and 1.2V supplies must not ramp before the 3.3V.

3.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typical	Max	Units
T_{OP}	Operating Temperature with external regulators		0		70	°C
	Operating temperature with on-die 2.5V regulator		0		55	°C
V_{PERIF}	Periphery Voltage Range	3.3 V ± 3%	3.0	3.3	3.6	V
V_D	Core Digital Voltage Range	1.2 V ± 5%	1.14	1.2	1.26	V
V_A	Analog VDD Range	2.5 V ± 5%	2.375	2.5	2.625	V

3.3 Power Supply Connections

There are three options in providing power to the 82573:

- Connecting the 82573 to three external power supplies with nominal voltages of 3.3V, 2.5V, and 1.2V. This is covered in Section 3.3.1.
- Powering the 82573 with only an external 3.3V supply and using internal power regulators from the 82573 combined with external PNP transistors to supply the 2.5V and 1.2V levels. This is covered in Section 3.3.3.
- Using the 2.5V internal (on-die) regulator combined with an external PNP transistor to supply the 1.2V level. This is covered in Section 3.3.3.

3.3.1 External LVR Power Delivery

The following power supply requirements apply to designs where the 82573 is supplied by external voltage regulators. These systems do not use the internal regulator logic built into the 82573 as described in Section 3.3.3.

Table 3. 3.3V External Supply Voltage Ramp and Sequencing Recommendations

Parameter	Description	Min	Max	Unit
Rise Time	Rise time from 10% to 90%	5	100[1]	ms
Monotonicity	Voltage dip allowed in ramp		300	mV
Slope	Ramp rate at any time between 10% to 90% Minimum = (0.8 * Vmin) / (Maximum Rise Time) Maximum = (0.8 * Vmax) / (Minimum Rise Time)		1500	mV/ms
Operational Range	Voltage range for normal operating conditions	3	3.6	V
Ripple	Maximum voltage ripple at a bandwidth of 50 MHz		100	mV_{pk-pk}
Overshoot	Maximum voltage allowed[2]		660	mV
Capacitance	Minimum capacitance	25		µF

1. Good design practices achieve voltage ramps to within the regulation bands in approximately 20 ms or less.
2. Excessive overshoot can affect long term reliability.

Table 4. 2.5V External Supply Voltage Ramp and Sequencing Recommendations

Parameter	Description	Min	Max	Unit
Rise Time	Rise time from 10% to 90%	2.5	100[1]	ms
Monotonicity	Voltage dip allowed in ramp		200	mV
Slope	Ramp rate at any time between 10% to 90% Minimum = (0.8 * Vmin) / (Maximum Rise Time) Maximum = (0.8 * Vmax) / (Minimum Rise Time)		1500	mV/ms
Operational Range	Voltage range for normal operating conditions	2.375	2.625	V
Operational Range	Voltage range for normal operating conditions	-5	+5	%
Ripple	Maximum voltage ripple at a bandwidth of 50 MHz		60	mV_{pk-pk}
Undershoot	Maximum voltage allowed will not exceed 10% of nominal supply			
Overshoot	Maximum voltage allowed[2]		480	mV
Output Capacitance	Capacitance range when using a PNP circuit	4.7	25	µF
Input Capacitance	Capacitance range when using a PNP circuit	4.7		µF
Capacitance ESR	Equivalent series resistance of output capacitance[3]		10	mΩ
I_{CTRL}	Maximum output current rating with respect to CTRL_25		20	mA

1. Good design practices achieve voltage ramps to within the regulation bands in approximately 20 ms or less.
2. Excessive overshoot can affect long term reliability.
3. Tantalum capacitors must not be used.

Table 5. 1.2V External Supply Voltage Ramp and Sequencing Recommendations

Parameter	Description	Min	Max	Unit
Rise Time	Rise time from 10% to 90%	1.5[1]		ms
Monotonicity	Voltage dip allowed in ramp		120	mV
Slope	Ramp rate at any time between 10% to 90% Minimum = (0.8 * Vmin) / (Maximum Rise Time) Maximum = (0.8 * Vmax) / (Minimum Rise Time)		1500	mV/ms
Operational Range	Voltage range for normal operating conditions	1.14	1.26	V
Operational Range	Voltage range for normal operating conditions	-5	+5	%
Ripple	Maximum voltage ripple at a bandwidth of 50 MHz		60	mV_{pk-pk}
Undershoot	Maximum voltage allowed will not exceed 10% of nominal supply			
Overshoot	Maximum voltage allowed[2]		500	mV
Output Capacitance	Capacitance range when using a PNP circuit	4.7	25	µF
Input Capacitance	Capacitance range when using a PNP circuit	4.7		µF
Capacitance ESR	Equivalent series resistance of output capacitance[3]		10	mΩ
I_{CTRL}	Maximum output current rating with respect to CTRL_12		20	mA

1. Good design practices achieve voltage ramps to within the regulation bands in approximately 20 ms or less.
2. Excessive overshoot can affect long term reliability.
3. Tantalum capacitors must not be used.

3.3.2 Power Sequencing with External Regulators

The following power-on and power-off sequence should be applied when external power supplies are in use. Designs must comply with the required power sequence to avoid risk of either latch-up or forward biased internal diodes.

Generally, the 82573 power sequencing should power up the three power rails in the following order: 3.3V → 2.5V → 1.2V. However, if this general guideline is not followed, there are specific requirements that must be adhered to. These requirements are listed in the following two subsections.

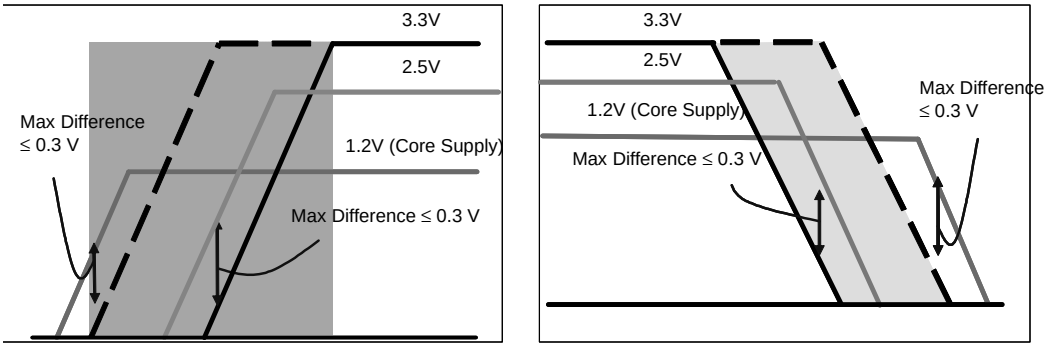
3.3.2.1 External LVR Power Up Sequencing and Tracking

Sequencing of the external supplies during power up might be necessary to ensure that the 82573 is not electrically overstressed and does not latch-up. These requirements are shown in Figure 2.

The 82573 core voltage (1.2V) cannot exceed the 3.3V supply by more than 0.5 V at any time during the power up. The 82573 core voltage (1.2V) cannot exceed the 2.5V supply by more than 0.5 V at any time during the power up. The core voltage is not required to begin ramping before the 3.3V or the 2.5V supply.

The 82573 analog voltage (2.5V) can not exceed the 3.3V supply by more than 0.5 V at any time during the power up. The analog voltage is not required to begin ramping before the 3.3V supply.

Figure 2. Minimum Requirements for Power Supply Sequencing



- If the 1.2V and 2.5V rails power up before 3.3V, they should never exceed the 3.3V supply by more than 0.3 V.
- At power down, all three supplies should be turned off simultaneously. If the 3.3V supply powers down first, the 1.2V and 2.5V supplies must never exceed the 3.3V supply by more than 0.3 V.

3.3.2.2 External LVR Power Down Sequencing

There are no specific power down sequencing and tracking requirements for the 82573 silicon. The risk of latch-up or electrical overstress is small since the only charge storing in decoupling capacitors is left in the system.

3.3.3 Internally Generated Power Delivery

The 82573 has two internal linear voltage regulator controllers. The controllers use external transistors to generate 2 of the 3 required voltages: 2.5V (nominal) and 1.2V (nominal). These two voltages are stepped down from a 3.3V source.

Table 6. 3.3V Internal Power Supply Parameters

Parameter	Description	Min	Max	Units
Rise Time	Time from 10% to 90% mark	5		ms
Monotonicity	Voltage dip allowed in ramp	-	300	mV
Slope	Ramp rate at any given time between 10% and 90% Min: 0.8*V(min)/Rise time (max) Max: 0.8*V(max)/Rise time (min)	-	1500	mV/ms
Operational Range	Voltage range for normal operating conditions	3.0	3.6	V
Ripple[1]	Maximum voltage ripple (peak to peak)	-	100	mV
Overshoot	Maximum overshoot allowed	-	660	mV
Overshoot Settling Time	Maximum overshoot allowed duration. (At that time delta voltage should be lower than 5 mV from steady state voltage)	-	3	ms

1. The peak to peak output rippled is measured at 20 MHz bandwidth within the operational range.

3.3.4 Internal LVR Power Sequencing

All supplies should rise monotonically. Sequencing of the supplies is controlled by the 82573.

3.3.4.1 Power Up Sequencing and Tracking

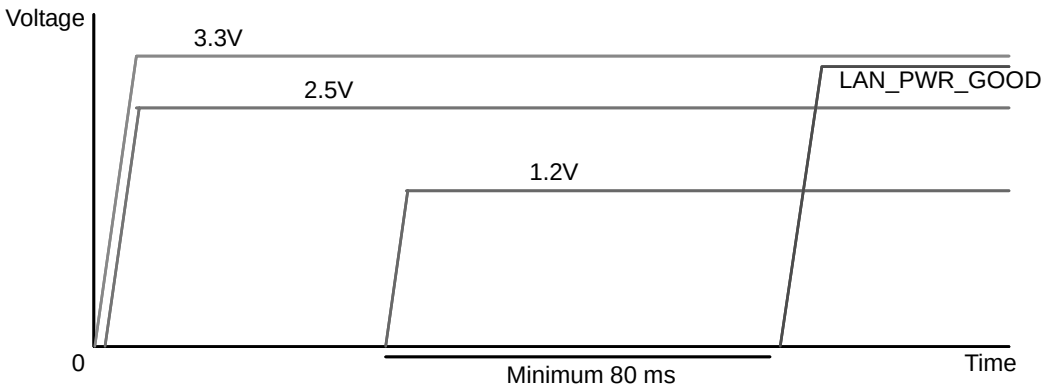
During power up, the sequencing and tracking of the internally controlled supplies (2.5V and 1.2V) are controlled by the 82573. No specific motherboard requirements are necessary to prevent electrical overstress or latch-up.

The 82573 analog voltage (2.5V) never exceeds the 3.3V supply at any time during the power up. This is because the 2.5V supply is generated from the 3.3V supply when the internal voltage regulator control logic is being used. Figure 3 shows the internal LVR circuit. The 2.5V supply tracks the 3.3V ramp.

The 82573 core voltage (1.2V) never exceeds the 3.3V at any time during the power up. This is because the 2.5V supply is generated from the 3.3V supply when the internal voltage regulator control logic is being used. Figure 3 shows the internal LVR circuit. The 1.2V ramp is delayed internally to prevent it from exceeding the 2.5V and 3.3V supply at any time. The delay is proportional to the slope of the 3.3V ramp.

The delay is approximated by $T_{ramp}(3.3V)*0.25 < T_{delay}(1.2V) < T_{ramp}(3.3V)*0.75$. T_{ramp} is defined to the ramp rate of the 3.3V input to the internal voltage regulator circuit.

Figure 3. Power Supply Sequencing



- It is recommended that the voltage on a lower voltage rail never exceed the voltage on a higher voltage rail during power on.
- There are no minimum time requirements between the voltage rails as long as they power up in sequence: 3.3V → 2.5V → 1.2V.
- All 3 supplies must be stable for at least 80 ms before LAN_PWR_GOOD is asserted. 100 ms is preferable if possible.
- A PCIe* reset must occur after LAN Power Good is active.

3.3.4.2 Internal LVR Power Down Sequencing

There are no specific power down sequencing and tracking requirements for the 82573 device. The risk of latch-up or electrical overstress is small because the only charge storing in decoupling capacitors is left in the system.

3.3.4.3 Internal Voltage Regulators Components for the 82573

Table 7. 82573 Bill of Materials (BOM) of Components for Internal Regulator

Description	Quantity	Recommended Component		
		Manufacturer	Part Number	Package
PNP Transistor For 1.2V LVR	1	Philips	BCP-69-16	SOT-223
PNP Transistor For 2.5V LVR	1	Philips	BCP-69-16	SOT-223

3.3.4.4 2.5V Internal LVR Specification

Table 8. 2.5V Internal LVR Specification[1]

Parameter	Value		Units	Comments
	Minimum	Maximum		
Input Voltage	3.0	3.6	V	
Input Voltage Slew Rate	5		ms	
Input Capacitance	4.7		µF	
Input Capacitance ESR		10	mΩ	
Load Current	1	-	A	V_{OUT} = 2.500 V
Output Voltage Tolerance	-5	+5	%	
Output Capacitance	4.7		µF	
Output Capacitance ESR		10	mΩ	
Current Consumption During Power Up		0.5	mA	
Current Consumption During Power Down		0.5	mA	
Maximum Undershoot		< 10	%	of nominal supply
Peak to Peak Output Ripple		120	mV	±60 mV at 20 MHz bandwidth
PSRR		20	dB	
External PNP h_{FE}	100			

1. The use of tantalum capacitors is not recommended.

3.3.4.5 1.2V Internal LVR Specification

Table 9. 1.2V Internal LVR Specification[1]

Parameter	Value		Units	Comments
	Minimum	Maximum		
Input Voltage	3.0	3.6	V	
Input Voltage Slew Rate	5		ms	
Input Capacitance	4.7		µF	
Input Capacitance ESR		10	mΩ	
Load Current	1	-	A	V_{OUT} = 1.200 V
Output Voltage Tolerance	-5	+5	%	
Output Capacitance	4.7		µF	
Output Capacitance ESR		10	mΩ	
Current Consumption During Power Up		0.5	mA	
Current Consumption During Power Down		0.5	mA	
Maximum Undershoot		< 10	%	of nominal supply
Peak to Peak Output Ripple		120	mV	±60 mV at 20 MHz bandwidth
PSRR		20	dB	
External PNP h_{FE}	100			

1. The use of tantalum capacitors is not recommended.

3.3.4.6 PNP Transistor Specification for Internal LVR

Table 10. PNP Specification (Sheet 1 of 2)

Symbol	Description	Min	Max	Units
$V_{ce,sat}$	Collector-Emitter Saturation Voltage	-	0.5	V
I_c(max)	Collector Current, Maximum Sustained	-	1000	mA
I_b	Base Current, Maximum Sustained	-	10	mA
V_{be}	Base-Emitter on Voltage	-	1	V
T_{jmax}	Maximum Junction Temperature	-	125	°C

Table 10. PNP Specification (Sheet 2 of 2)

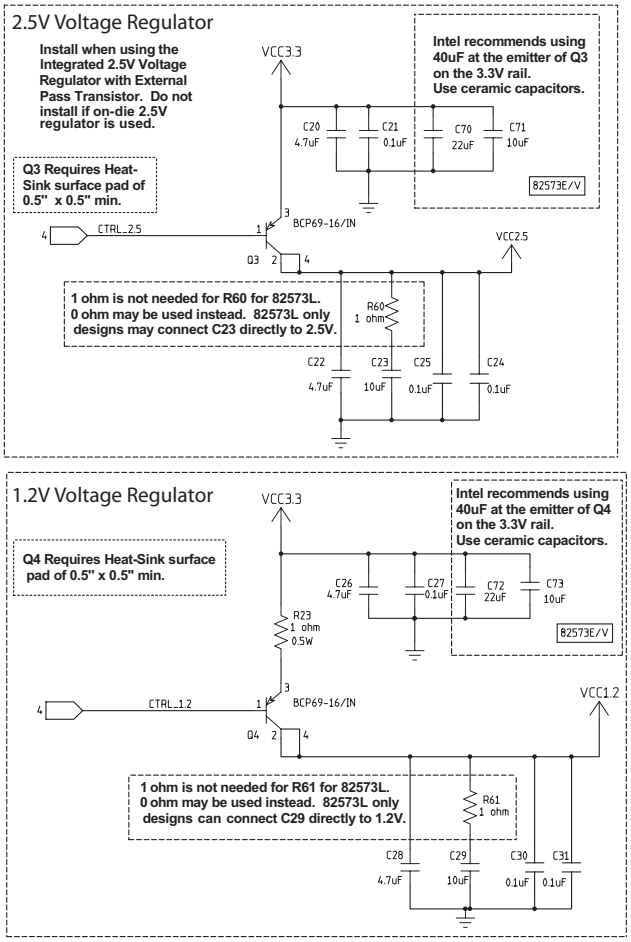
Symbol	Description	Min	Max	Units
Power Dissipation	Maximum Total Power Dissipation	-	1.35	W
h_{FE}	DC Current Gain	100	-	-
f_T	Current Gain Product Bandwidth	10	-	MHz

3.3.4.7 Internal LVR Board Schematic

When using the internal voltage regulator controllers built into the 82573, resistors might need to be placed in series with the emitter in order to prevent the PNP transistors from overheating. These series resistors dissipate a portion of the power that would otherwise be dissipated by the PNP devices. The value and power rating of the resistors must be carefully chosen to balance thermal limits against the PNP characteristics against total current draw. The regulator must never drop below the minimum V_{ce} and out of the linear region.

The effective resistance of the pass resistors should equal approximately 1 Ω and have a combined power dissipation rating of 0.5 Watts for the 82573. Figure 4 shows the recommended implementation.

Figure 4. 82573 2.5V and 1.2V LVR Schematic



3.4 DC and AC Specifications

Table 11. 82573E and 82573V Maximum Measured External Power Characteristics[1]

System State	Link State	82573E Power (mW) with Intel® AMT	82573V Power (mW) without Intel® AMT
S0	1000 Mbps Active (Maximum Power)	1548	1426

1. Maximum conditions refer to fast silicon, high temperature and nominal VCC.

Table 12. 82573E and 82573V Typical Measured External Power Characteristics[1]

System State	Link State	3.3V Current (mA)	2.5V Current (mA)	1.2V Current (mA)	82573E/V Power (mW)[2 3]
S0	1000 Mb/s: Intel® AMT (82573E only)	12	297	551	1443.3
	1000 Mb/s Active	12	297	490	1370.1
	1000 Mb/s Idle	12	276	380	1185.6
	100 Mb/s Active	11	130	144.5	534.7
	100 Mb/s Idle	11	107	101	425
	10 Mb/s Active	7	167	125.5	591.2
	10 Mb/s Idle	7	76	82	311.5
	No Link (SPD)	3	40	73	197.5
Sx	100 Mb/s Idle (wake)	11	104	93.5	408.5
	10 Mb/s Idle (wake)	7	72	74.5	292.5
	No Link (no wake)	3	36[4]	64.5	177.3
	Device Off	3	42[d]	48.5	173.1

1. Maximum conditions refer to fast silicon, high temperature and nominal VCC.
2. For 10/100 Mb/s non-stress mode with Intel® AMT, add 12 mW to this number (for example, using IDE-R functionality).
3. For 10/100 Mb/s stress mode active Intel® AMT, add 120 mW to this number (for example, using IDE-R functionality).
4. The current use is slightly higher in the device off state than in the no link state. This occurs since a PHY reset is required in the device off state, which overrides the PHY power down.

Table 13. 82573E and 82573V 2.5V Internal Power Regulator Numbers

System State	Link State	3.3V Current (mA)	2.5V Current (mA) (on-die 2.5V regulator)	1.2V Current (mA)	82573E/V Power (mW)
S0	1000 Mb/s: Active with Full Management	313	Internal	607	1760
	1000 Mb/s Active	313	Internal	506	1638
	1000 Mb/s Idle	294	Internal	404	1453
	100 Mb/s Active	142	Internal	145	642
	100 Mb/s Idle	119	Internal	101	513
	10 Mb/s Active	173	Internal	126	722
	10 Mb/s Idle	84	Internal	83	376
	D0 No Link (SPD)	44	Internal	73	233
Sx	D3 100 Mb/s Idle (wake)	116	Internal	94	493
	D3 10 Mb/s Idle (wake)	80	Internal	75	354
	D3 No Link (no wake)	40	Internal	64	209
	Device Off	45	Internal	49	207

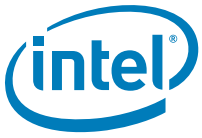


Table 14. 82573L Maximum Measured Power Characteristics[1]

System State	Link State	82573L (mW)
S0	1000 Mb/s Active (Maximum Power)	1296

1. Maximum conditions refer to fast silicon, high temperature and nominal VCC.

Table 15. 82573L Measured Power Characteristics

System State	Link State	3.3V Current (mA)	2.5V Current (mA)	1.2V Current (mA)	82573L Power (mW)
S0	1000 Mb/s Active	14.8	288.5	372.5	1217
	1000 Mb/s Idle	14.8	243.2	294.0	1010
	100 Mb/s Active	14.0	121.3	111.5	483
	100 Mb/s Idle	14.2	78.8	58.5	314
	10 Mb/s Active	10.5	169	118	504
	10 Mb/s Idle	10.3	143.5	91.8	194
	D0 No Link (SPD)	6.2	7.0	12.3	53
Sx	D3 100 Mb/s Idle (wake)	14.2	78.8	49.3	303
	D3 10 Mb/s Idle (wake)	10.5	45.7	31.0	186
	D3 No Link (no wake)	6.2	7.3	12.2	53

Table 16. DC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
Vih	Input High Voltage		2.0		V
Vil	Input Low Voltage			0.8	V
Vhy	Input Hysteresis		100		mV
Voh	Output High Voltage		2.4		V
Vol	Output Low Voltage			0.4	V
Ilkg	Input Leakage Current	0 < Vin < VCCP		±50	µA
Rpup/ Rpdn	Internal Pull Up and Pull Down Resistor		15	50	KΩ
Cin/out	Pin Capacitance	Input and bi-directional buffer		2.5	pF
Cout	Output Pin Capacitance	Output only buffer		2.0	pF

Table 17. LED DC Specifications

Symbol	Parameter[1]	Condition	Min	Max	Unit
Voh	Output High Voltage	at 12 mA	2.4		V
Vol	Output Low Voltage	at 12 mA		0.4	V
Ioz	3-state Output Leakage Current	Voh = VDD or VSS		±10	mV
Ios	Output Short Current	VDD = 3.6 V, Vo = VDD, VDD = 3.6 V, Vo = VSS			µA
Cin/out	Pin Capacitance[2]	Input and bi-directional buffer		2.5	pF

1. Outputs are inputs/outputs in test mode.
2. This parameter is characterized but not tested.

3.5 External Interfaces

3.5.1 Crystal

The quartz crystal is strongly recommended as a low cost and high performance choice with the 82573 device. Quartz crystals are the mainstay of frequency control components and are available from numerous vendors in many package types with various specification options.

Table 18. Crystal Specifications

Parameter Name	Symbol	Recommended Value	Max/Min Range	Conditions
Frequency	f_o	25.000 MHz	-	at 25 °C
Vibration mode	-	Fundamental	-	-
Frequency Tolerance	$\Delta f/f_o$ at 25 °C	±30 ppm		at 25 °C
Temperature Tolerance	$\Delta f/f_o$	±30 ppm		-
Operating Temperature	T_{opr}	0 °C to +70 °C		-
Equivalent Series Resistance (ESR)	R_s	40 Ω	50 Ω (max)	at 25 MHz
Load Capacitance	C_{load}	20 pF		-
Shunt Capacitance	C_o	6 pF		-
Max Drive Level	DL	500 µW	1 mW	-
Nominal Drive Level	DL	200 µW	500 µW	-
Aging	f/f_o	±5 ppm per year	±5 ppm per year	-
Board Capacitance	C_s	4 pF	[1]	-
External Capacitors	C1, C2	22 pF		-
Board Resistance	R_s	0.1 Ω	1 Ω	-

1. This value can change up to 10%.

3.5.2 External Clock Oscillator

If an external oscillator is used to provide a clock to the 82573, the connection shown in the figure below must be used. The XTAL2 output signal of the 82573 must not be connected. The XTAL1 input signal receives the output of the oscillator directly. AC coupling is not recommended.

Figure 5. External Clock Oscillator Connectivity to the 82573

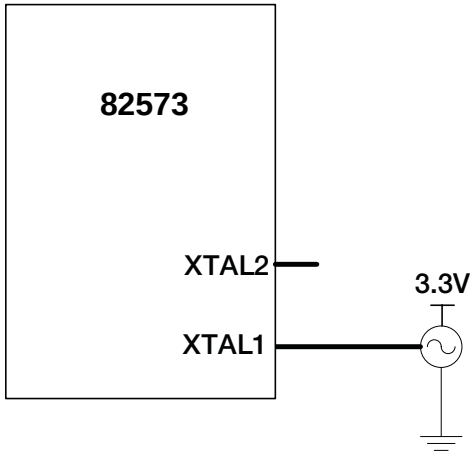


Table 19. Specification for External Clock Oscillator

Parameter Name	Symbol	Value	Conditions
Frequency	f_o	25.0 MHz	at 25 °C
Swing	V_{p-p}	3.3 ± 0.3 V	-
Frequency Tolerance	$\Delta f/f_o$	±30 ppm	0 °C to +70 °C
Operating Temperature	T_{opr}	-20 °C to +70 °C	0 °C to +70 °C
Aging	$\Delta f/f_o$	±5 ppm per year	-

3.5.3 Non-Volatile Memory (NVM) Interface: EEPROM

Table 20. NVM Interface Timing Specifications for EEPROM (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Units
t_{SCK}	SCK clock frequency	0	2	2.1	MHz
t_{RU}	Input rise time		2.5	2	µs
t_{FI}	Input fall time		2.5	2	µs
t_{WH}	SCK high time[1]	200	250		ns
t_{WH}	SCK low time[a]	200	250		ns
t_{CS}	CS high time	250			ns
t_{CSS}	CS setup time	250			ns
t_{CSH}	CS hold time	250			ns
t_{SU}	Data-in setup time	50			ns
t_H	Data-in hold time	50			ns
t_V	Output Valid	0		200	ns

Table 20. NVM Interface Timing Specifications for EEPROM (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Units
t_{HO}	Output hold time	0			ns
t_{DIS}	Output disable time			250	ns
t_{WC}	Write cycle time			10	ms

1. 50% duty cycle.

4.0 Package and Pinout Information

This section describes the 82573 physical characteristics and pin-to-signal mapping.

4.1 Package Information

The 82573 device is a lead-free 196-pin thin and Fine Pitch Ball Grid Array (TF-BGA) measuring 15 mm by 15 mm. The nominal ball pitch is 1.0 mm.

Figure 6. 82573 Controller TF-BGA Package Ball Pad Dimensions

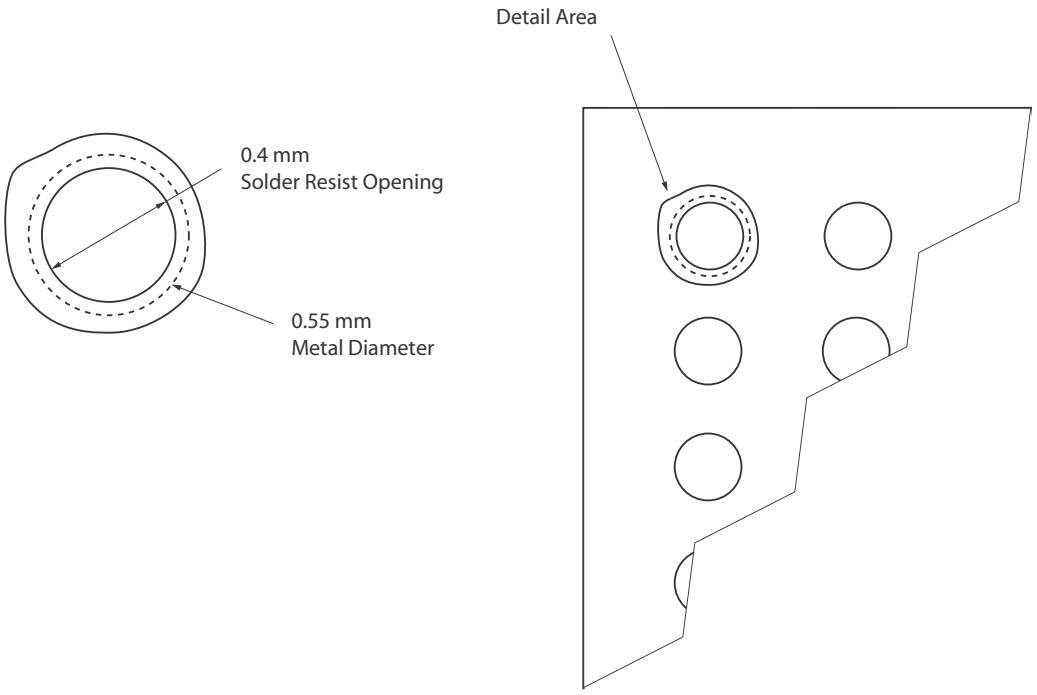
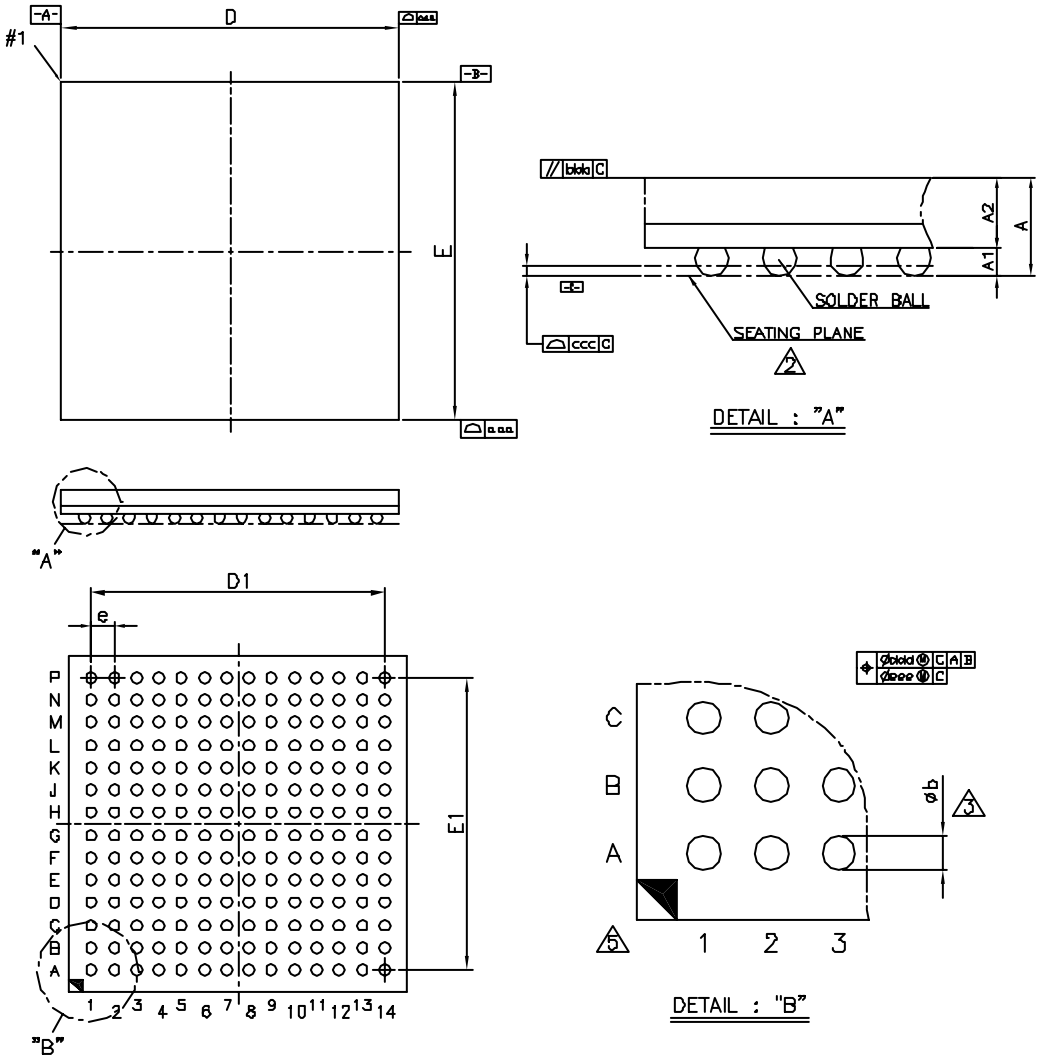


Figure 7. 82573 Mechanical Specifications



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.60	---	---	0.063
A1	0.35	0.40	0.45	0.014	0.016	0.018
A2	1.01	1.06	1.11	0.040	0.042	0.044
D	14.90	15.00	15.10	0.587	0.591	0.594
E	14.90	15.00	15.10	0.587	0.591	0.594
D1	---	13.00	---	---	0.512	---
E1	---	13.00	---	---	0.512	---
e	---	1.00	---	---	0.039	---
b	0.45	0.50	0.55	0.018	0.020	0.022
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.15			0.006		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	14/14			14/14		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

4.2 Thermal Specifications

The case temperature (T_C) is calculated using the equation:

$T_C = T_A + P (\psi_{JA} - \psi_{JC})$

Junction temperature (T_J) is calculated using the equation:

$T_J = T_A + P \psi_{JA}$

The power consumption (P) is calculated by using the typical ICC and nominal VCC where T_A represents the ambient temperature. The thermal resistances are listed in Table 21.

Table 21. Thermal Resistance Values

Symbol	Parameter	Value at Specified Airflow (m/s)				Units
		0	1	2	3	
TJ	Maximum junction temperature	127.1	122.1	119.3	117.5	C
Ψ_{JA}	Thermal resistance, junction-to-ambient	26.0	23.7	22.4	21.6	C/Watt
Ψ_{JC}	Thermal resistance, junction-to-case	6.1	6.1	6.1	6.1	C/Watt

Thermal resistances are determined empirically with test devices mounted on standard thermal test boards. Real system designs may have different characteristics due to board thickness, arrangement of ground planes, and proximity of other components. The case temperature measurements should be used to assure that the 82573 is operating under recommended conditions. The use of a heat sink device is not required.

4.3 Pinout Information

4.3.1 PCIe Bus Interface Signals

Table 22. PCIe Data Signals

Signal	Pin	Signal	Pin	Signal	Pin
PE_CLKn	G2	PE_T0n	C1	PE_R0n	F1
PE_CLKp	G1	PE_T0p	D1	PE_R0p	F2

Table 23. PCI Express Miscellaneous Signals

Signal	Pin	Signal	Pin	Signal	Pin
PE_RST#	P7	PE_WAKE#	P10	AUX_PRESENT (82573E/V) / AUX_PWR (82573L)[1]	C6
CLKREQ# (82573L only)	P9				

1. This signal is used in all three devices and has the same functionality but is denoted as AUX_PRESENT in the 82573E/V or AUX_PWR in the 82573L.

4.3.2 Non-Volatile Memory Interface Signals

Table 24. Non-Volatile Memory Interface Signals

Signal	Pin	Signal	Pin	Signal	Pin
NVM_SI	A9	NVM_CS#	B10	NVM_TYPE	A6
NVM_SO	B9	NVM_REQ	B4	NVM_SHARED#	D3
NVM_SK	C9	NVM_PROT	A5		

4.3.3 Miscellaneous Signals

Table 25. Reset and Power-down Signals

Signal	Pin	Signal	Pin	Signal	Pin
LAN_PWR_GOOD	P5	DEVICE_OFF#	L7		

Table 26. SMBus Signals

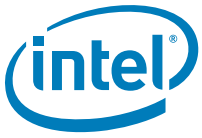
Signal	Pin	Signal	Pin	Signal	Pin
SMB_CLK	P11	SMB_DAT	M11	SMB_ALRT# / ASF_PWR_GOOD	N11

Table 27. LED Signals

Signal	Pin	Signal	Pin	Signal	Pin
LED0#	B11	LED1#	C11	LED2#	A12

Table 28. Other Signals

Signal	Pin	Signal	Pin	Signal	Pin
THERMn	L2	THERMp	L3		



4.3.4 PHY Signals

Table 29. Analog and Crystal Signals

Signal	Pin	Signal	Pin	Signal	Pin
MDI0n	C14	MDI2n	F14	PHY_REF	D12
MDI0p	C13	MDI2p	F13	XTAL1	K14
MDI1n	E14	MDI3n	H14	XTAL2	J14
MDI1p	E13	MDI3p	H13		

4.3.5 Test Signals

Table 30. 82573E/V MAC Test Signals[1]

Signal	Pin	Signal	Pin	Signal	Pin
TEST_EN	A13	TEST1	H2	TEST9	M3
ALT_CLK125	N10	TESTPT2	H3	TEST10	N2
JTAG_TCK	N5	TESTPT3	J1	TEST11	P1
JTAG_TDI	P4	TESTPT4	J2	TEST12	N3
JTAG_TDO	P6	TEST5	J3	TEST13	M8
JTAG_TMS	N4	TEST6	K1	TEST14 (82573E/V only)	P9
CLK_VIEW	L14	TEST7	L1	TEST15 (82573E/V only)	E3
TEST0	H1	TEST8	M1	TEST16 (82573E/V only)	A14

1. These test signals do not apply to the 82573L.

Table 31. 82573L MAC Test Signals[1]

Signal	Pin	Signal	Pin	Signal	Pin
TEST_EN	A13	CLK_VIEW	L14	TEST5	J3
ALT_CLK125	N10	TEST0	H1	TEST6	K1
JTAG_TCK	N5	TEST1	H2	TEST7	L1
JTAG_TDI	P4	TESTPT2	H3	TEST8	M1
JTAG_TDO	P6	TESTPT3	J1	TEST9	M3
JTAG_TMS	N4	TESTPT4	J2		

1. These test signals do not apply to the 82573E or 82573V devices.

Table 32. PHY Test Interface Signals

Signal	Pin	Signal	Pin	Signal	Pin
PHY_HSDACn	B13	PHY_HSDACp	B12	PHY_TSTPT	B14

Table 33. 82573E/V Other Test Signals[1]

Signal	Pin	Signal	Pin	Signal	Pin
SDP[0]	A8	SDP[1]	B8	SDP[2]	C8
SDP[3]	C7				

1. These test signals do not apply to the 82573L.

4.3.6 Power Supply Signals

Table 34. Power Support Signals

Signal	Pin	Signal	Pin	Signal	Pin
CTRL_25	A4	CTRL_12	P3	EN25REG	B5

Table 35. Power Signals

Signal	Pin	Signal	Pin	Signal	Pin
VCC33	A7	VCC25	J12	VCC12	J6
VCC33	D9	VCC25	K13	VCC12	J7
VCC33	F3	VCC25	L12	VCC12	J8
VCC33	J4	VCC25	M4	VCC12	J9
VCC33	M10	VCC25	N7	VCC12	J10
VCC33	N6	VCC25_OUT	B1	VCC12	J11
VCC33	N8	VCC25_OUT	B2	VCC12	K3
VCC33	P2	VCC12	A10	VCC12	K4
VCC33	P12	VCC12	C4	VCC12	K5
IREG25_IN	A2	VCC12	C5	VCC12	K6
IREG25_IN	A3	VCC12	F12	VCC12	K7
FUSEV	M2	VCC12	G6	VCC12	K8
VCC25	A11	VCC12	G12	VCC12	K9
VCC25	B6	VCC12	G13	VCC12	K10
VCC25	G3	VCC12	H6	VCC12	K11
VCC25	G5	VCC12	H7	VCC12	L5
VCC25	H4	VCC12	H8	VCC12	L9
VCC25	H5	VCC12	H11	VCC12	L10
VCC25	J5	VCC12	H12		

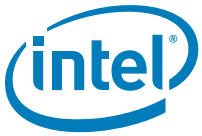


Table 36. Ground Signals

Signal	Pin	Signal	Pin	Signal	Pin
VSS	A1	VSS	E5	VSS	G4
VSS	B3	VSS	E6	VSS	G7
VSS	C2	VSS	E7	VSS	G8
VSS	C10	VSS	E8	VSS	G9
VSS	C12	VSS	E9	VSS	G10
VSS	D2	VSS	E10	VSS	G11
VSS	D4	VSS	F4	VSS	G14
VSS	D5	VSS	F5	VSS	H9
VSS	D6	VSS	F6	VSS	H10
VSS	D7	VSS	F7	VSS	K2
VSS	D8	VSS	F8	VSS	N1
VSS	D13	VSS	F9	VSS	N12
VSS	E2	VSS	F10	VSS	P8
VSS	E4	VSS	F11		

Table 37. 82573E/V No Connect Signals[1]

Signal	Pin	Signal	Pin	Signal	Pin
NC	B7	NC	K12	NC	M9
NC	C3	NC	L4	NC	M12
NC	D10	NC	L6	NC	M13
NC	D11	NC	L8	NC	M14
NC	D14	NC	L11	NC	N9
NC	E1	NC	L13	NC	N13
NC	E11	NC	M5	NC	N14
NC	E12	NC	M6	NC	P13
NC	J13	NC	M7	NC	P14

1. These test signals do not apply to the 82573L.

Table 38. 82573L No Connect Signals[1] (Sheet 1 of 2)

Signal	Pin	Signal	Pin	Signal	Pin
NC	A8	NC	E12	NC	M9
NC	A14	NC	J13	NC	M12
NC	B7	NC	K12	NC	M13
NC	B8	NC	L4	NC	M14
NC	C3	NC	L6	NC	N2
NC	C7	NC	L8	NC	N3
NC	C8	NC	L11	NC	N9
NC	D10	NC	L13	NC	N13

Table 38. 82573L No Connect Signals[1] (Sheet 2 of 2)

Signal	Pin	Signal	Pin	Signal	Pin
NC	D11	NC	M5	NC	N14
NC	D14	NC	M6	NC	P1
NC	E1	NC	M7	NC	P13
NC	E3	NC	M8	NC	P14
NC	E11				

1. These test signals do not apply to the 82573E or 82573V devices.

4.4 Visual Pin Assignments

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
1	VSS	VCC25_ OUT	PE_T0n	PE_TR0p	NC	PE_R0n	PE_CLKp	TEST0	TEST3	TEST6	TEST7	TEST8	VSS	TEST11
2	IREG25_IN	VCC25_ OUT	VSS	VSS	VSS	PE_R0p	PE_CLKn	TEST1	TEST4	VSS	THERMn	FUSEV	TEST10	VCC33
3	IREG25_IN	VSS	NC	NVM_ SHARED	TEST15	VCC33	VCC25	TEST2	TEST5	VCC12	THERMp	TEST9	TEST12	CTRL_12
4	CTRL_25	NVM_REQ	VCC12	VSS	VSS	VSS	VSS	VCC25	VCC33	VCC12	NC	VCC25	JTAG_TMS	JTAG_TDI
5	NVM_ PROT	EN25REG	VCC12	VSS	VSS	VSS	VCC25	VCC25	VCC25	VCC12	VCC12	NC	JTAG_ TCK	LAN_PWR_ GOOD
6	NVM_ TYPE	VCC25	AUX_ PRESENT	VSS	VSS	VSS	VCC12	VCC12	VCC12	VCC12	NC	NC	VCC33	JTAG_TDO
7	VCC33	NC	SDP[3]	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	DEVICE_ OFF#	NC	VCC25	PE_RST#
8	SDP[0]	SDP[1]	SDP[2]	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	NC	TEST13	VCC33	VSS
9	NVM_SI	NVM_SO	NVM_SK	VCC33	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	NC	NC	TEST14
10	VCC12	NVM_CS#	VSS	NC	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	VCC33	ALT_CLK125	PE_WAKE#
11	VCC25	LED0#	LED1#	NC	NC	VSS	VSS	VCC12	VCC12	VCC12	NC	SMB_DAT	SMB_ALRT#/ ASF_PWR_ GOOD	SMB_CLK
12	LED2#	PHY_ HSDACp	VSS	PHY_REF	NC	VCC12	VCC12	VCC12	VCC25	NC	VCC25	NC	VSS	VCC33
13	TEST_EN	PHY_ HSDACn	MDI0p	VSS	MDI1p	MDI2p	VCC12	MDI3p	NC	VCC25	NC	NC	NC	NC
14	TEST16	PHY_ TSTPT	MDI0n	NC	MDI1n	MDI2n	VSS	MDI3n	XTAL2	XTAL1	CLK_VIEW	NC	NC	NC

Figure 8. 82573E and 82573V Gigabit Ethernet Controller Pinout

Figure 9. 82573L Gigabit Ethernet Controller Pinout

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
1	VSS	VCC25_ OUT	PE_T0n	PE_TR0p	NC	PE_R0n	PE_CLKp	TEST0	TEST3	TEST6	TEST7	TEST8	VSS	NC
2	VCC3.3_ REG25	VCC25_ OUT	VSS	VSS	VSS	PE_R0p	PE_CLKn	TEST1	TEST4	VSS	THERMn	FUSEV	TEST10	VCC33
3	VCC3.3_ REG25	VSS	NC	NVM_ SHARED	NC	VCC33	VCC25	TEST2	TEST5	VCC12	THERMp	TEST9	NC	CTRL_12
4	CTRL_25	NVM_REQ	VCC12	VSS	VSS	VSS	VSS	VCC25	VCC33	VCC12	NC	VCC25	JTAG_TMS	JTAG_TDI
5	NVM_ PROT	EN25REG	VCC12	VSS	VSS	VSS	VCC25	VCC25	VCC25	VCC12	VCC12	NC	JTAG_ TCK	LAN_PWR_ GOOD
6	NVM_ TYPE	VCC25	AUX_PWR	VSS	VSS	VSS	VCC12	VCC12	VCC12	VCC12	NC	NC	VCC33	JTAG_TDO
7	VCC33	NC	NC	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	DEVICE_ OFF#	NC	VCC25	PE_RST#
8	NC	NC	NC	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	NC	NC	VCC33	VSS
9	NVM_SI	NVM_SO	NVM_SK	VCC33	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	NC	NC	CLK_REQ#
10	VCC12	NVM_CS#	VSS	NC	VSS	VSS	VSS	VSS	VCC12	VCC12	VCC12	VCC33	ALT_CLK125	PE_WAKE#
11	VCC25	LED0#	LED1#	NC	NC	VSS	VSS	VCC12	VCC12	VCC12	NC	RSVD	RSVD	RSVD
12	LED2#	PHY_ HSDACp	VSS	PHY_REF	NC	VCC12	VCC12	VCC12	VCC25	NC	VCC25	NC	VSS	VCC33
13	TEST_EN	PHY_ HSDACn	MDI0p	VSS	MDI1p	MDI2p	VCC12	MDI3p	NC	VCC25	NC	NC	NC	NC
14	NC	PHY_ TSTPT	MDI0n	NC	MDI1n	MDI2n	VSS	MDI3n	XTAL2	XTAL1	CLK_VIEW	NC	NC	NC