4 M x 1-Bit Dynamic RAM — HYB 514100BJ/BT-60/-70/-80
Low Power 4 M x 1-Bit Dynamic RAM — HYB 514100BJL/BTL-60/-70/-80

Advanced Information

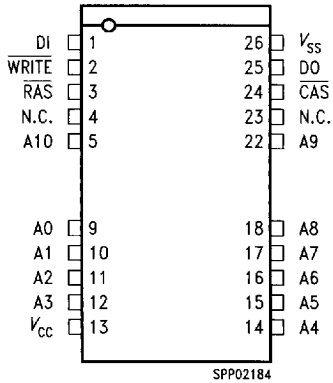
- 4 194 304 words by 1-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  RAS access time:
  60 ns (-60 version)
  70 ns (-70 version)
  80 ns (-80 version)
  CAS access time:
  20 ns
  Cycle time:
  110 ns (-60 version)
  130 ns (-70 version)
  150 ns (-80 version)
- Fast page mode cycle time
  45 ns (-60 version)
  45 ns (-70 version)
  50 ns (-80 version)
- Single + 5 V (± 10 %) supply with a built-in V_{bb} generator
- Low power dissipation
  max. 605 mW active (-60 version)
  max. 550 mW active (-70 version)
  max. 468 mW active (-80 version)
- Standby power dissipation:
  11 mW standby standby (TTL)
  5.5 mW max.standby (CMOS)
  1.1 mW max.standby (CMOS) for Low Power Version
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify write, CAS-before-RAS refresh, RAS-only refresh, hidden refresh, fast page mode capability and test mode capability
- All inputs and outputs TTL-compatible
- 1024 refresh cycles / 16 ms
- 1024 refresh cycles / 128 ms Low Power Version only
- Plastic Packages: P-SOJ-26/20-5 and P-TSOPII-26/20-1 with 300 mil width

The HYB 514100B is the new generation dynamic RAM organized as 4 194 304 words by 1-bit. The HYB 514100B utilizes CMOS silicon gate process as well as advances circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514100B to be packed in a standard plastic P-SOPJ-26/20 or P-TSOPII-26/20 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented feature include single + 5 V (± 10 %) power supply, direct interfacing with high performance logic device families such as Schottky TTL.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 514100BJ-60	Q67100-Q759	P-SOJ-26/20-5	DRAM (access time 60 ns)
HYB 514100BJ-70	Q67100-Q760	P-SOJ-26/20-5	DRAM (access time 70 ns)
HYB 514100BJ-80	Q67100-Q761	P-SOJ-26/20-5	DRAM (access time 80 ns)
HYB 514100BJL-60	on request	P-SOJ-26/20-5	DRAM (access time 60 ns)
HYB 514100BJL-70	Q67100-Q763	P-SOJ-26/20-5	DRAM (access time 70 ns)
HYB 514100BJL-80	Q67100-Q765	P-SOJ-26/20-5	DRAM (access time 80 ns)
HYB 514100BT-60	Q67100-Q746	P-TSOPII-26/20-1	DRAM (access time 60 ns)
HYB 514100BT-70	Q67100-Q747	P-TSOPII-26/20-1	DRAM (access time 70 ns)
HYB 514100BT-80	Q67100-Q748	P-TSOPII-26/20-1	DRAM (access time 80 ns)
HYB 514100BTL-60	on request	P-TSOPII-26/20-1	DRAM (access time 60 ns)
HYB 514100BTL-70	on request	P-TSOPII-26/20-1	DRAM (access time 70 ns)
HYB 514100BTL-80	on request	P-TSOPII-26/20-1	DRAM (access time 80 ns)

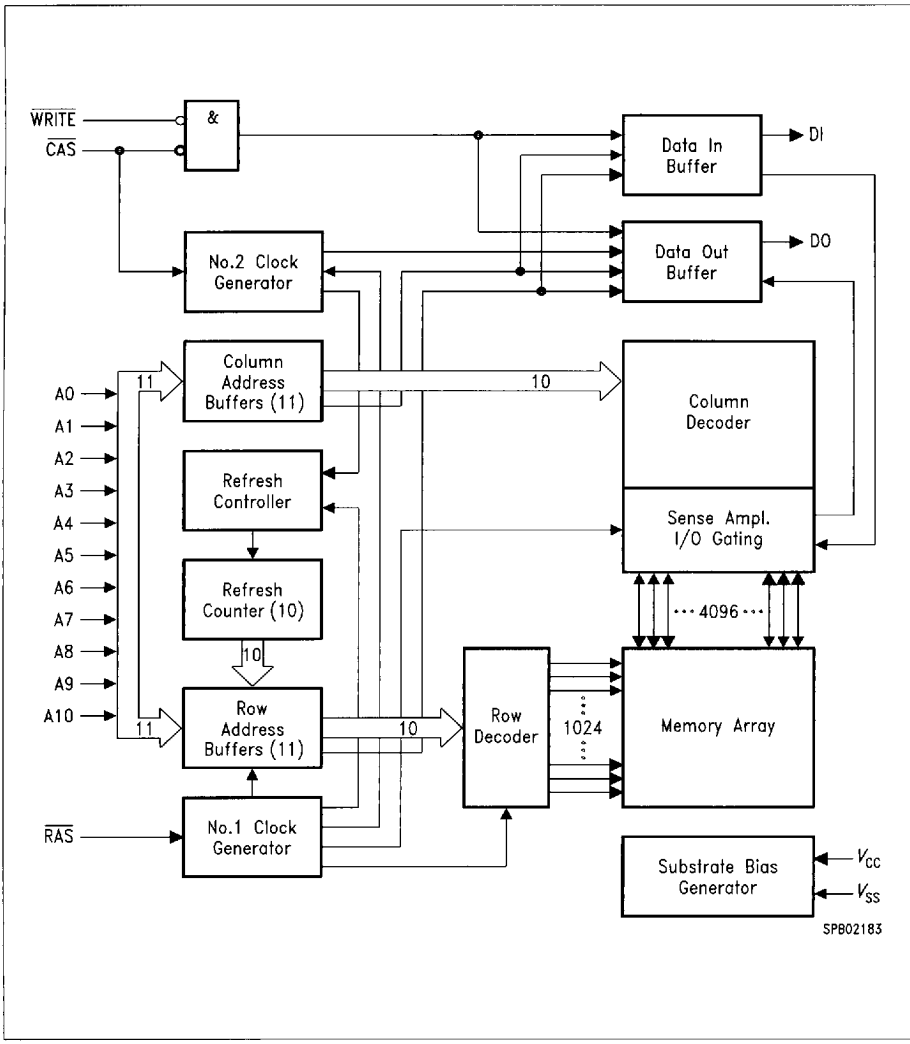
P-SOJ-26/20-5
P-TSOPII-26/20-1



Pin Configuration

Pin Names

A0-A10	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
DI	Data In
DO	Data Out
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to + 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power Supply voltage ..... – 1 to + 7 V
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{ih}	2.4	6.5	V	1)
Input low voltage	V_{il}	– 1.0	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{oh}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{ol}	–	0.4	V	1)
Input leakage current, any input (0 V < V_{in} < 7, all other input = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 < V_{OUT} < V_{cc})	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current	I_{CC1}			mA	2) 3)
-60 version		–	110		
-70 version		–	100		
-80 version		–	85		
Standby V_{CC} supply current (RAS = CAS = V_{ih})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current during RAS-only refresh cycles	I_{CC3}			mA	2)
-60 version		–	110		
-70 version		–	100		
-80 version		–	85		
Average V_{CC} supply current during fast page mode operation	I_{CC4}			mA	2) 3)
-60 version		–	70		
-70 version		–	70		
-80 version		–	50		

Notes see page 84.

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Standby V_{CC} supply current (RAS = CAS = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Standby V_{CC} supply current (RAS = CAS = V_{CC} – 0.2 V) for Low Power Version	I_{CC5}	–	200	µA	–
Average V_{CC} supply current during CAS before RAS refresh mode	I_{CC6}			mA	2)
-60 version		–	110		
-70 version		–	100		
-80 version		–	85		
For Low Power Version only: Battery backup current (average power supply current in battery backup mode): (CAS = CAS before RAS cycling or 0.2 V, WRITE = V_{CC} – 0.2 V or 0.2 V, A0 to A10 = V_{CC} – 0.2 V or 0.2 V; DI = V_{CC} – 0.2 V or 0.2 V or open, t_{RC} = 125 µs, t_{RAS} = t_{RAS} min = 1 µs)	I_{CC7}	–	300	µA	–

Notes see page 84.

AC Characteristics [4]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
Random read or write time	t_{RC}	110	–	130	–	150	–	ns
Read-write cycle time	t_{RCW}	165	–	185	–	205	–	ns
Fast page mode cycle time	t_{PC}	45	–	45	–	50	–	ns
Fast page mode read/write cycle time	t_{PRWC}	100	–	100	–	105	–	ns
Access time from RAS [6) 11)]	t_{RAC}	–	60	–	70	–	80	ns
Access time from CAS [6) 11)]	t_{CAC}	–	20	–	20	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	–	40	ns
Access time from CAS precharge [6)]	t_{CPA}	–	40	–	40	–	45	ns
CAS to output in low-Z [6)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay from CAS [7)]	t_{OFF}	0	20	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	3	50	ns
RAS precharge time	t_{RP}	40	–	50	–	60	–	ns
RAS pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns
RAS pulse width in fast page mode	t_{RASP}	60	200000	70	200000	80	200000	ns
RAS hold time	t_{RSH}	20	–	20	–	20	–	ns
CAS hold time	t_{CSH}	60	–	70	–	80	–	ns
CAS pulse width	t_{CAS}	20	10000	20	10000	20	10000	ns
RAS to CAS delay time [11)]	t_{RCD}	20	40	20	50	20	60	ns
RAS to column address delay time [12)]	t_{RAD}	15	30	15	35	15	40	ns

Notes see page 84.

AC Characteristics (cont'd)[4]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
CAS to RAS precharge time	t_{CRP}	5	–	5	–	10	–	ns
CAS precharge time	t_{CPN}	10	–	10	–	10	–	ns
CAS precharge time in fast page mode	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	15	–	ns
Column address to RAS lead time	t_{RAL}	30	–	35	–	40	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [8]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time ref. to RAS [8]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	15	–	ns
Write command hold time ref. to RAS	t_{WCR}	50	–	55	–	60	–	ns
Write command pulse width	t_{WP}	10	–	15	–	15	–	ns
Write command to RAS lead time	t_{RWL}	20	–	20	–	20	–	ns
Write command to CAS lead time	t_{CWL}	20	–	20	–	20	–	ns
Data setup time [9]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [9]	t_{DH}	15	–	15	–	15	–	ns

Notes see page 84.

AC Characteristics (cont'd)[4]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
Refresh period	t_{REF}	–	16	–	16	–	16	ms
Refresh period Low Power Version	t_{REF}	–	128	–	128	–	128	ms
Write command setup time [10]	t_{WCS}	0	–	0	–	0	–	ns
CAS to WRITE delay time [10]	t_{CWD}	50	–	50	–	50	–	ns
RAS to WRITE delay time [10]	t_{RWD}	90	–	100	–	110	–	ns
Column address to WRITE delay time [10]	t_{AWD}	60	–	65	–	70	–	ns
CAS setup time (CBR cycle)	t_{CSR}	5	–	5	–	5	–	ns
CAS hold time (CBR cycle)	t_{CHR}	15	–	15	–	15	–	ns
RAS to CAS precharge time	t_{RPC}	0	–	0	–	0	–	ns
CAS precharge time (CAS before RAS counter test cycle)	t_{CPT}	30	–	40	–	40	–	ns
Write command setup time (test mode entry)	t_{WTS}	10	–	10	–	10	–	ns
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	10	–	ns
Write to RAS precharge time (CBS cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write to RAS hold time (CBR cycle)	t_{WRH}	10	–	10	–	10	–	ns

Notes see page 84.

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10, DI)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	C_{I2}	–	7	pF
Output capacitance (DO)	C_{IO}	–	7	pF

Notes for pages 79 to 83:

1) All voltages are referenced to V_{SS}

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1}, I_{CC4} depend on output loading.

4) An initial pause of 200 µs is required after power-up followed by 8 RAS cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.

5) V_{ih} (min.) and V_{il} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{ih} and V_{il}.

6) Measured with a load equivalent to 2 TTL loads and 100 pF.

7) T_{off} (max.) defines the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are references to the CAS leading edge in early write and to the WRITE leading edge in read-write cycles.

10) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only.
If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.) and $t_{AWD} > t_{AWD}$ (min.), the cycle is a read-write cycle and DO will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of D/O (at access time) is indeterminate.

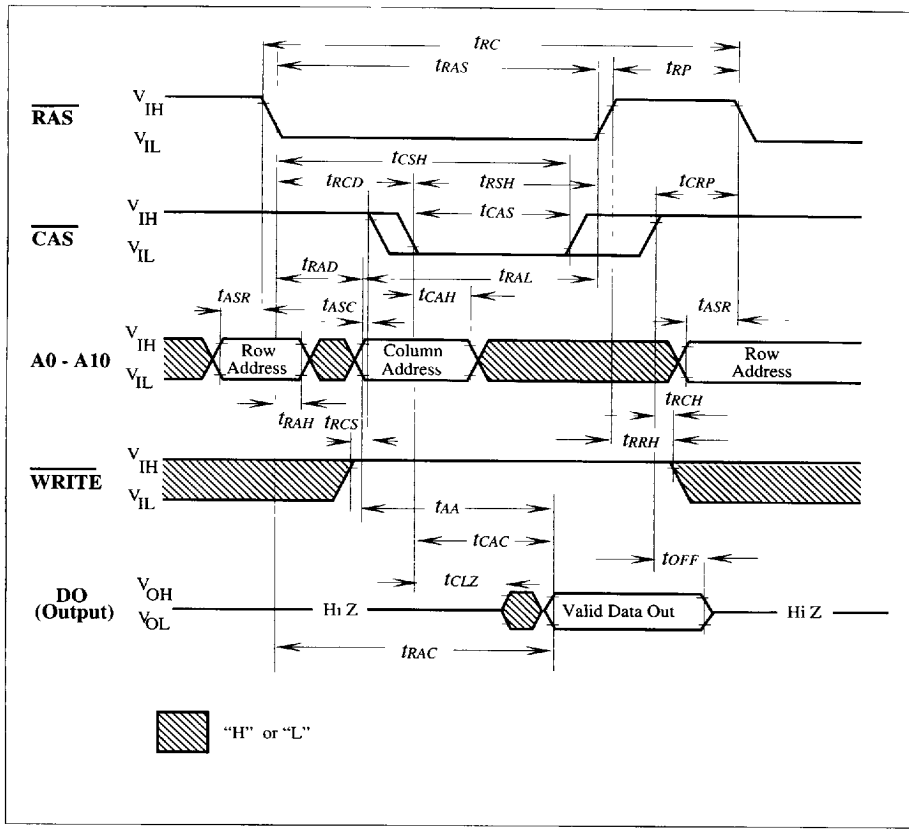
11) Operation within the t_{RCD} (max.) limit ensure that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit ensured that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

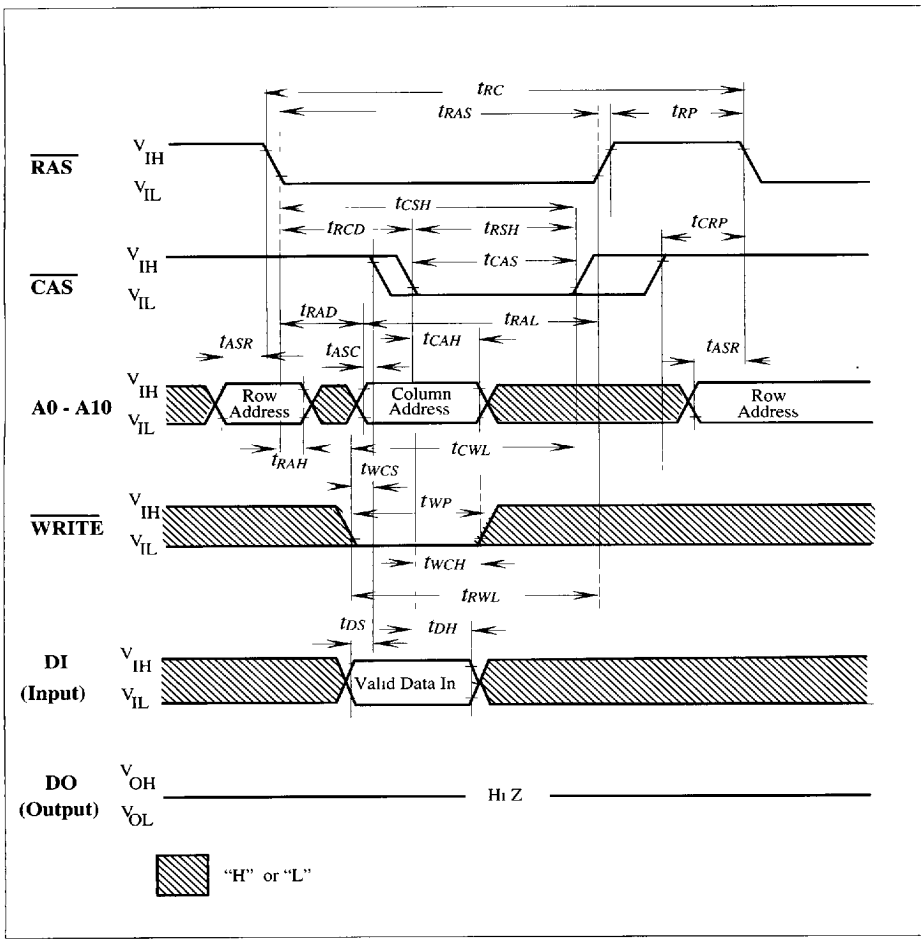
13) AC mesurements assume t_T = 5 ns

14) Either t_{DZC} or t_{DZO} must be satisfied.

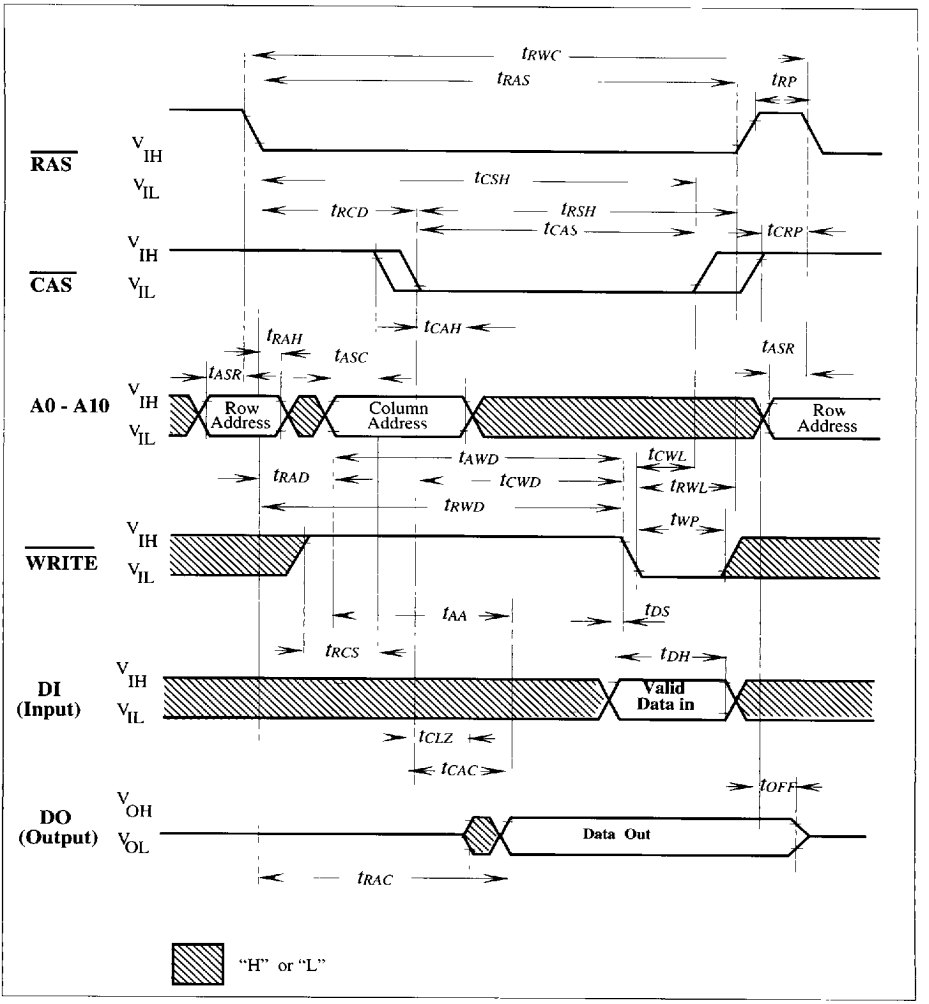
15) Either t_{CDD} or t_{ODD} must be satisfied.



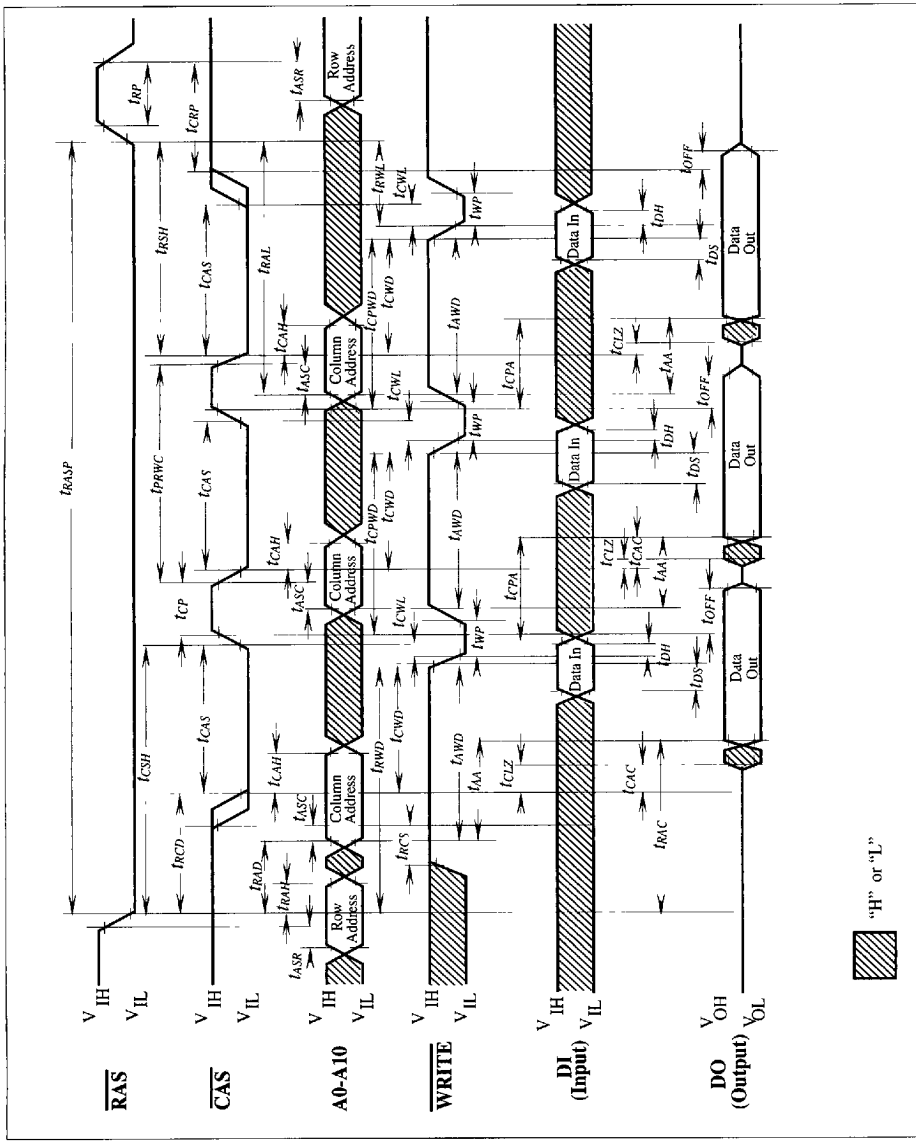
Read Cycle



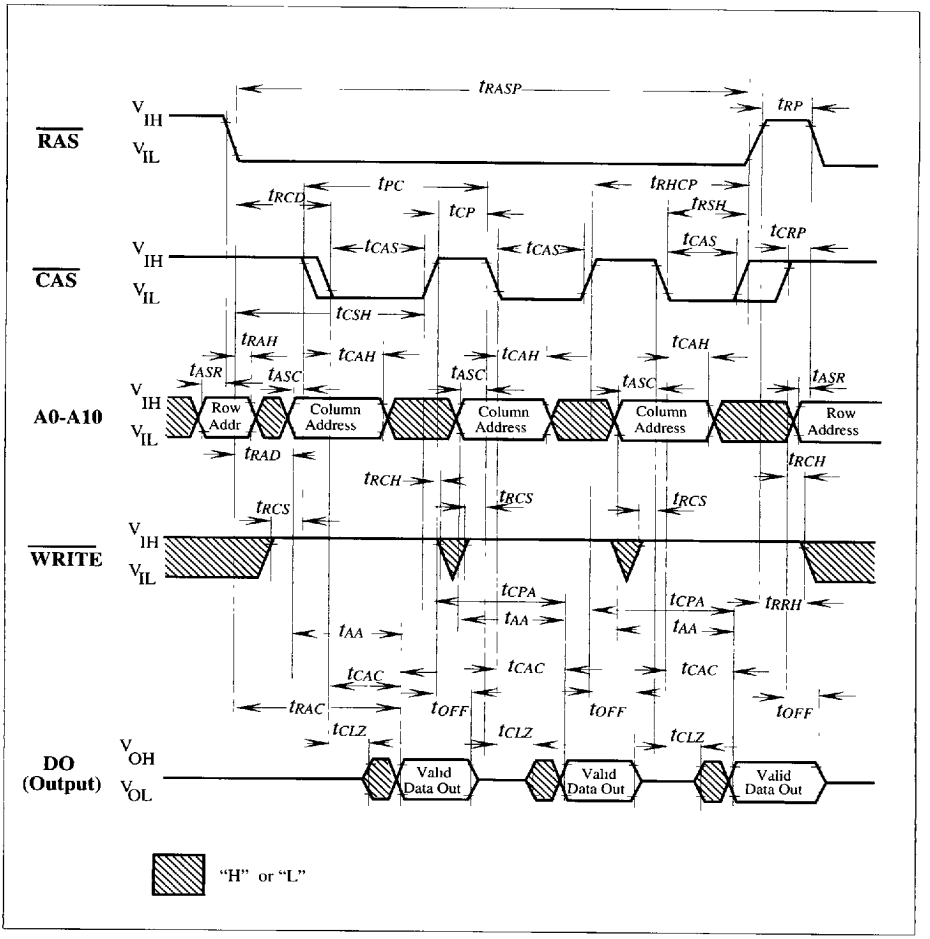
Write Cycle (Early Write)



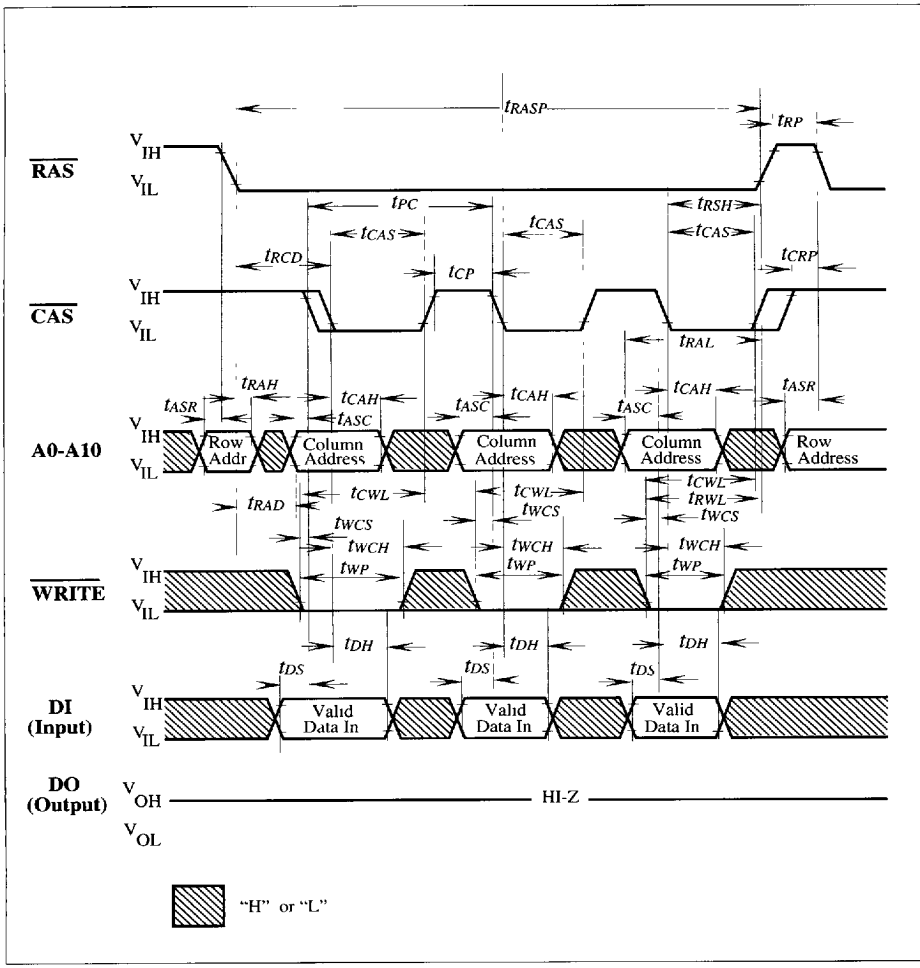
Read-Write (Read-Modify-Write) Cycle



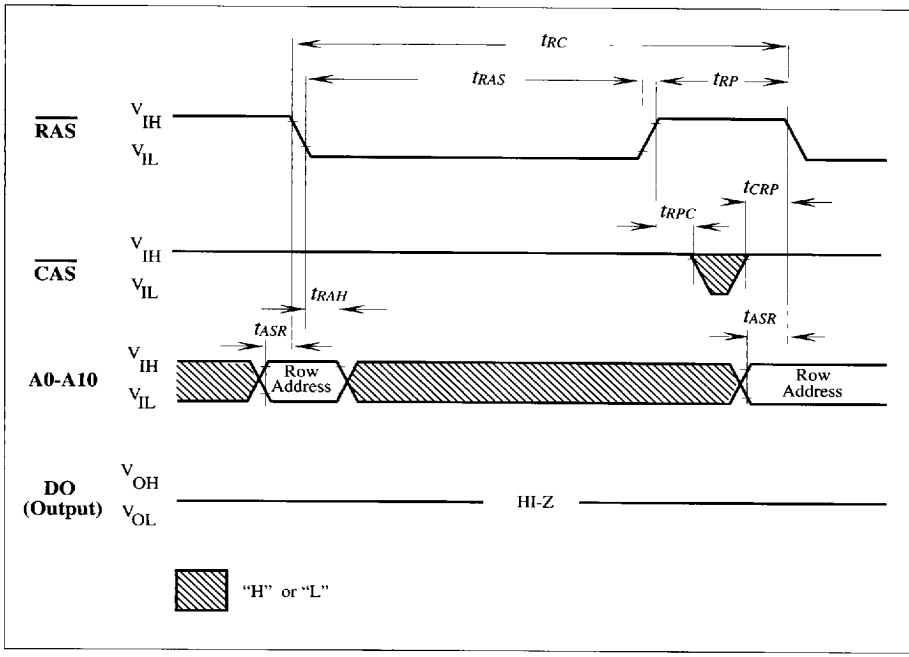
Fast Page Mode Read-Modify-Write Cycle



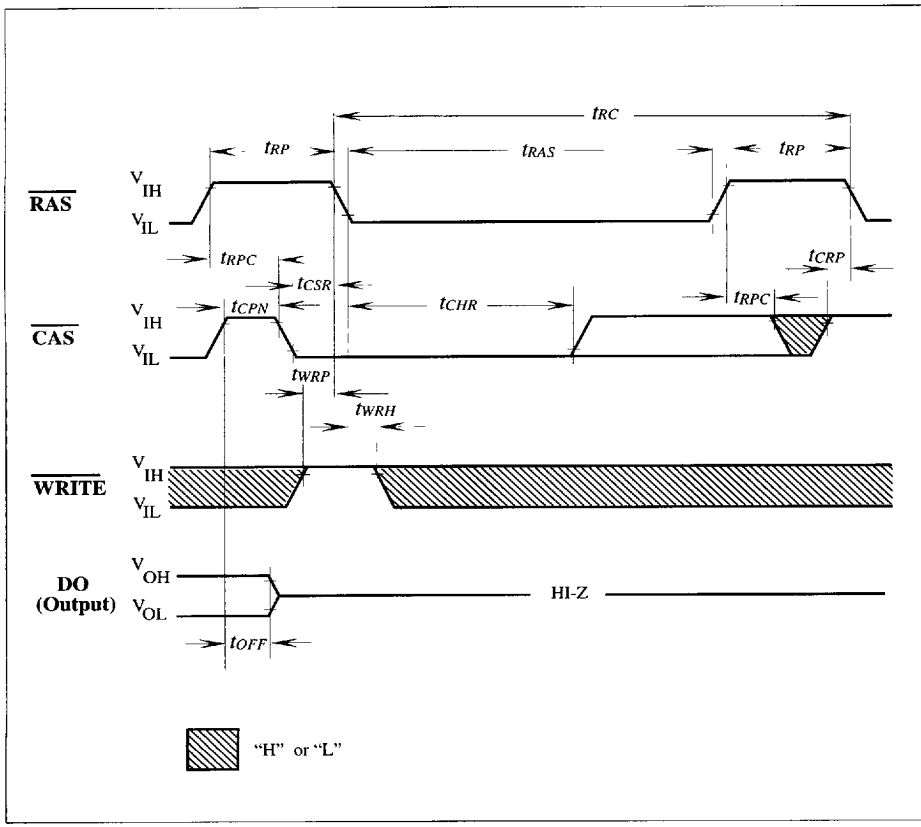
Fast Page Mode Read Cycle



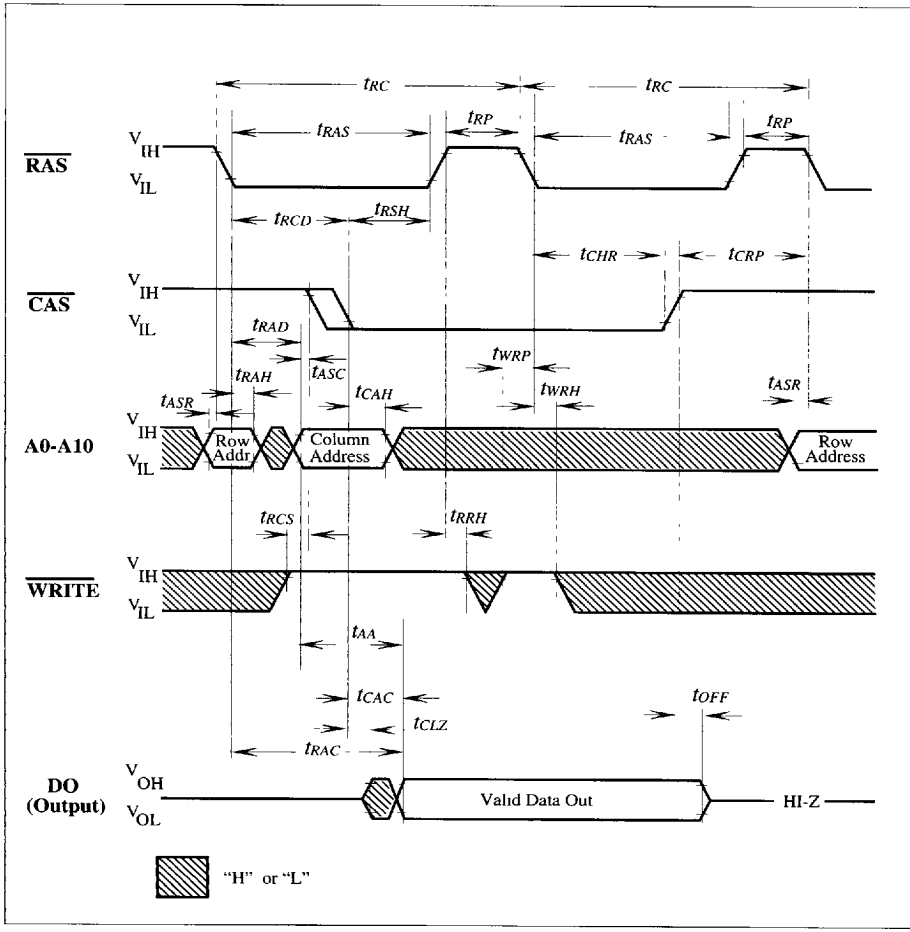
Fast Page Mode Early Write Cycle



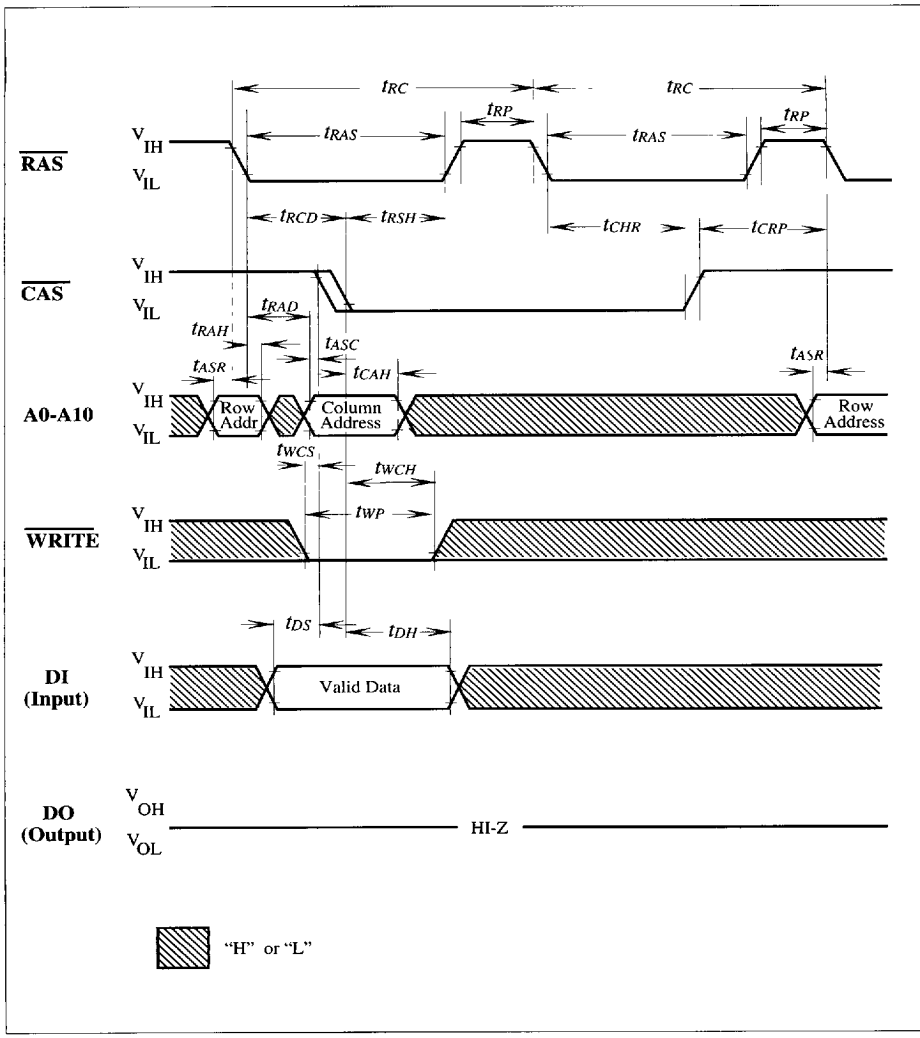
$\overline{\text{RAS}}$-Only Refresh Cycle



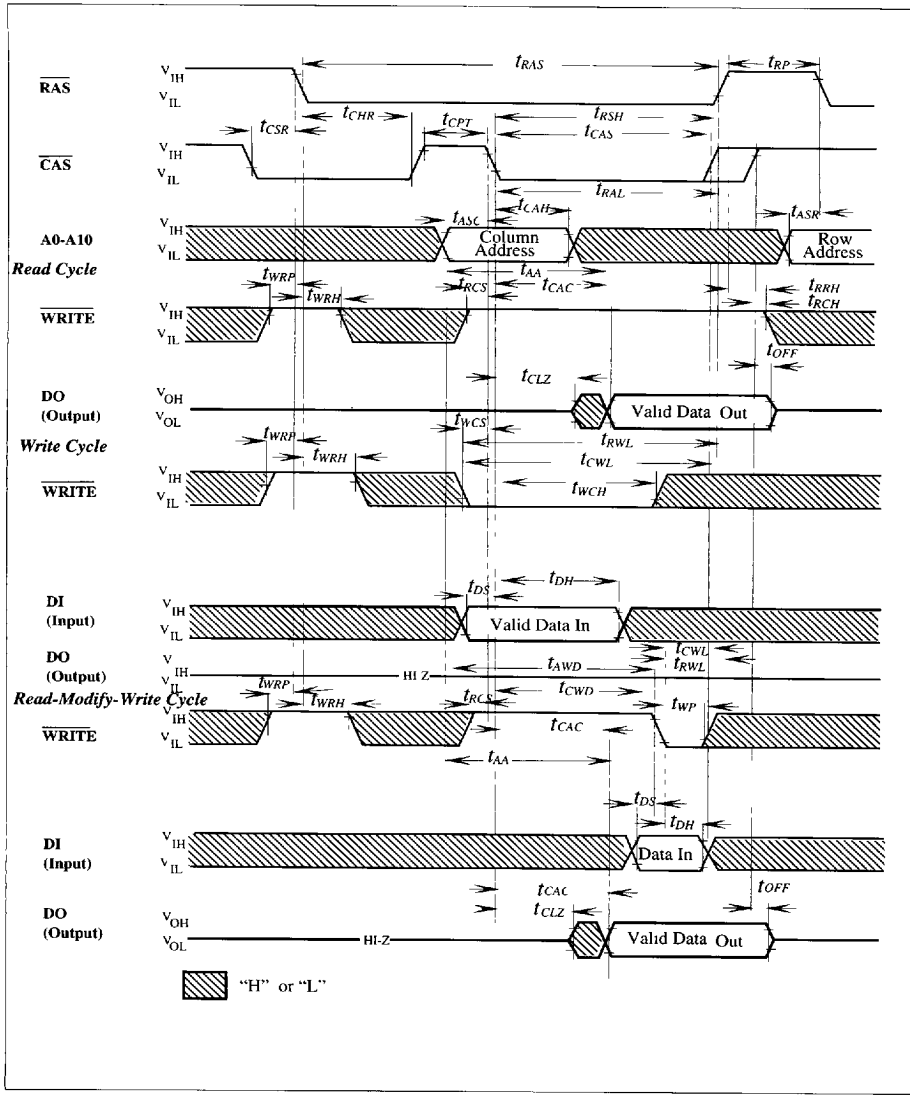
CAS-Before-RAS Refresh Cycle



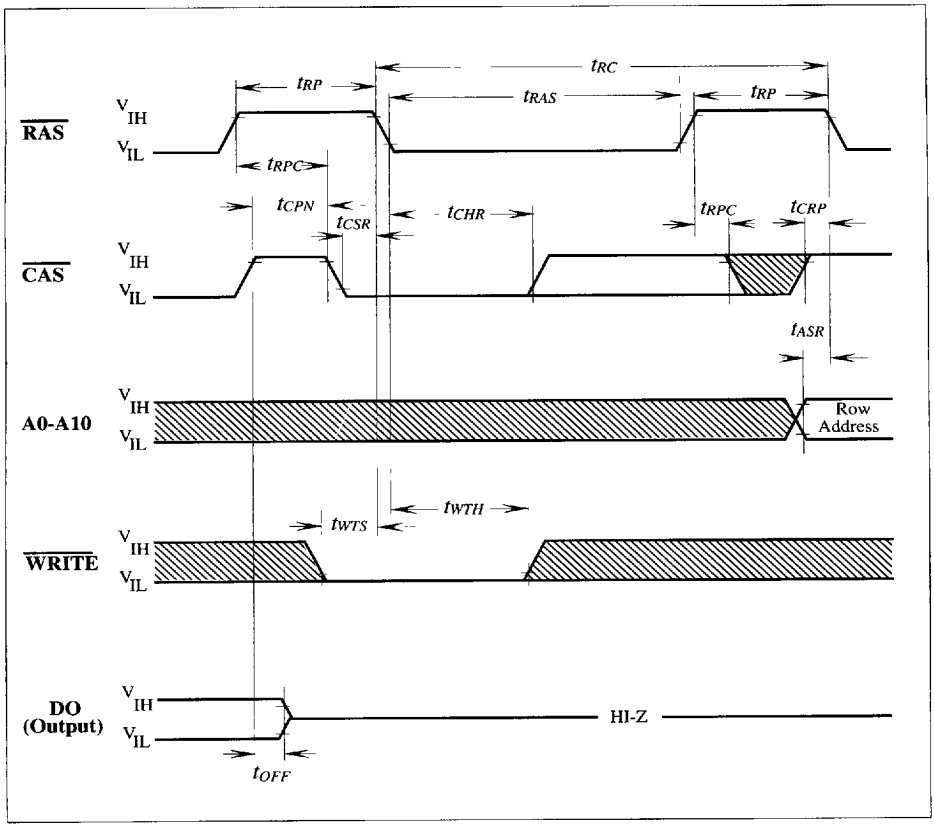
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

Test Mode

The HYB514100BJ/BT/BJL/BTL is organized 4 194 304 words by 1- bit but can internally be configured as 524 288 words by 8-bits. A $\overline{\text{WRITE}}$, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle puts the device into Test Mode.

In Test Mode, data is written into 8 sectors in parallel and retrieved the same way. If, upon reading, all bits are equal, the data output pin indicates a "1". If any of the bits differ, the data output pin indicates a "0". In Test Mode the 4M DRAM can be tested as if it were a 512K DRAM. Test Mode is exited by any refresh operation which is not a $\overline{\text{WRITE}}$, $\overline{\text{CAS}}$- before-$\overline{\text{RAS}}$ cycle. Addresses A10R, A10C and A0C do not care during Test Mode.