tyco Electronics

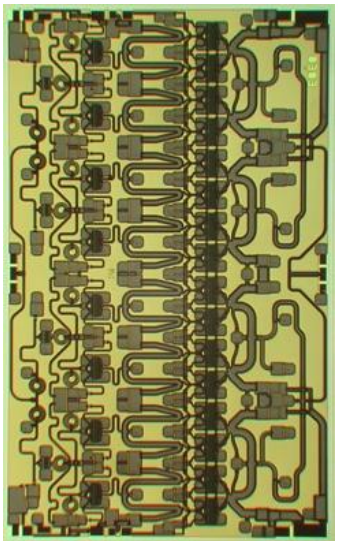
MACOM

Amplifier, Power, 20W
7.5-10.5 GHz

MAAPGM0079-DIE
Rev A
Preliminary Datasheet

Features

- **17 Watt Saturated Output Power Level**
- **20 Watt Saturated Output Power Level over 8-10 GHz Band**
- **Variable Drain Voltage (8-10V) Operation**
- **MSAG™ Process**
- **Robust Stability**



Description

The MAAPGM0079-DIE is a 3 stage 20W power amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG)Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- **SatCom**
- **Commercial Avionics**
- **Radar**

Also Available in:

Description	Ceramic Package	Sample Board (Die)	Sample Board (Pkg)	Mechanical Sample (Die)
Part Number	MAAP-000079-PKG001	MAAP-000079-SMB004	MAAP-000079-SMB001	MAAP-000079-MCH000

Electrical Characteristics: T_B = 40°C[1], Z_0 = 50 Ω, V_{DD} = 10V, I_{DQ} = 4A[2], P_{in} = 18 dBm, R_g = 20 Ω

Parameter	Symbol	Typical	Units
Bandwidth	f	7.5-10.5	GHz
Output Power	P_{OUT}	42	dBm
Output Power, 8-10 GHz	P_{OUT}	43	dBm
1-dB Compression Point	P1dB	42	dBm
Small Signal Gain	G	29	dB
Power Added Efficiency	PAE	30	%
Input VSWR	VSWR	2.5:1	
Output VSWR	VSWR	2.5:1	
Gate Current	I_{GG}	50	mA
Drain Current, under RF Drive	I_{DD}	6	A
Output Third Order Intercept	TOI	48	dBm
Output Third Order Intermod, Pout = 39 dBm (DCL)	IM3	18.5	dBc

1. **T_B = MMIC Base Temperature**
2. **Adjust V_{GG} between –2.6 and –1.5V to achieve specified Idq.**

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Maximum Ratings[3]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	23	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF)	I_{DQ}	6.6	A
Quiescent DC Power Dissipated (No RF)	P_{DISS}	65.8	W
Junction Temperature	T_J	170	°C
Storage Temperature	T_{STG}	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

Recommended Operating Conditions[4]

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Voltage	V_{DD}	4.0	10.0	10.0	V
Gate Voltage	V_{GG}	-2.6	-2.2	-1.5	V
Input Power	P_{IN}		18.0	21.0	dBm
Thermal Resistance	Θ_{JC}		2.2		°C/W
MMIC Base Temperature	T_B			Note 5	°C

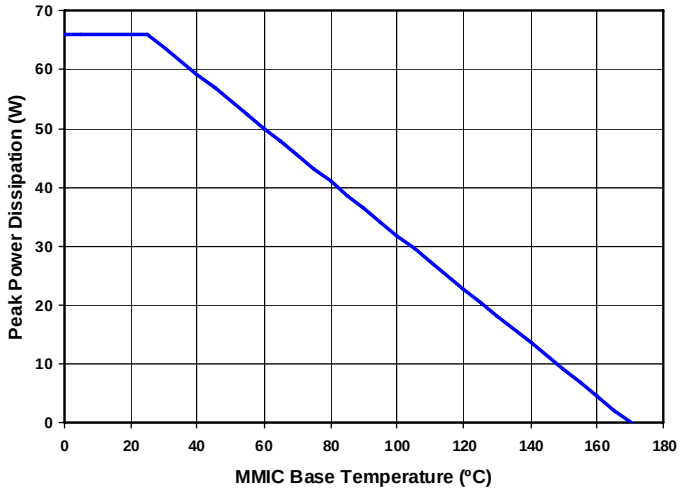
4. Operation outside of these ranges may reduce product reliability.
5. MMIC Base Temperature = 170°C — Θ_{JC}* V_{DD} * I_{DQ}

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -2.7 V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 10.0 V.
3. Adjust V_{GG} to set I_{DQ}, (approximately @ –2.2 V).
4. Set RF input.
5. Power down sequence in reverse. Turn V_{GG} off last.

Power Derating Curve, Quiescent (No RF)



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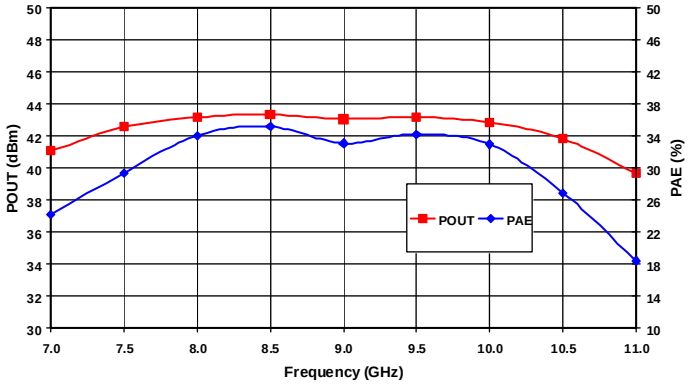

Figure 1. Output Power and Power Added Efficiency vs. Frequency at V_{DD} = 10V and P_{in} = 18 dBm

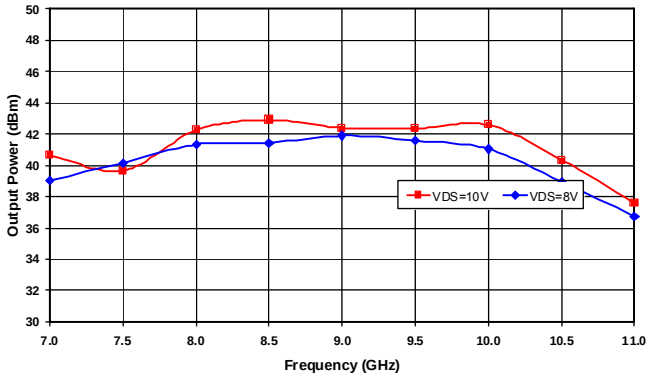

Figure 2. 1dB Compression Point vs. Drain Voltage

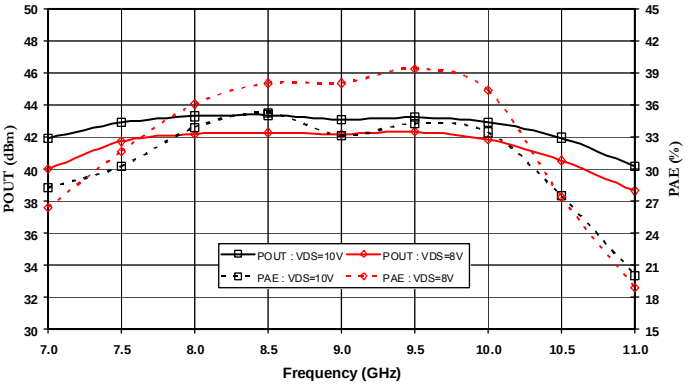

Figure 3. Saturated Output Power and Power Added Efficiency vs. Frequency and Drain Voltage

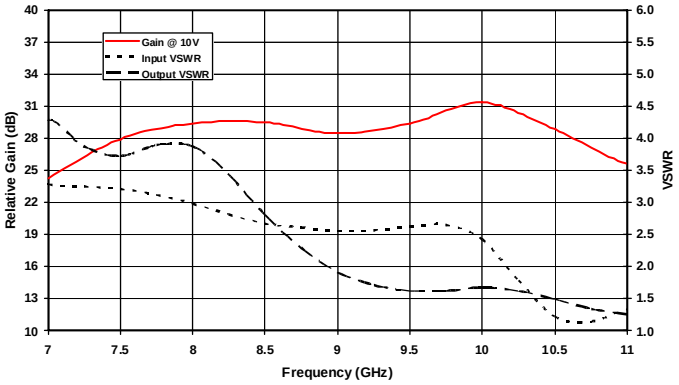

Figure 4. Small Signal Gain and Input and Output VSWR vs. Frequency.

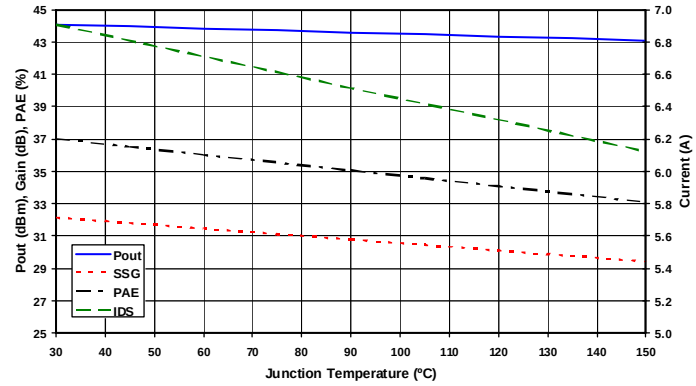

Fig 5. Output Power, Power Added Efficiency, and Drain Current vs. Junction Temperature at V_D=10V, f=9GHz, and P_{in}=18dBm.

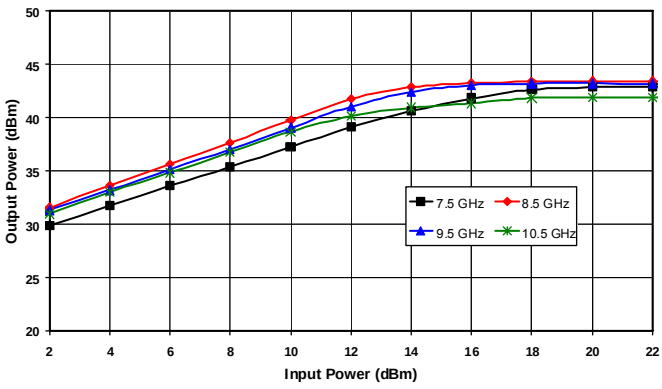

Figure 6. Output Power vs. Input Power at V_{DD} = 10V

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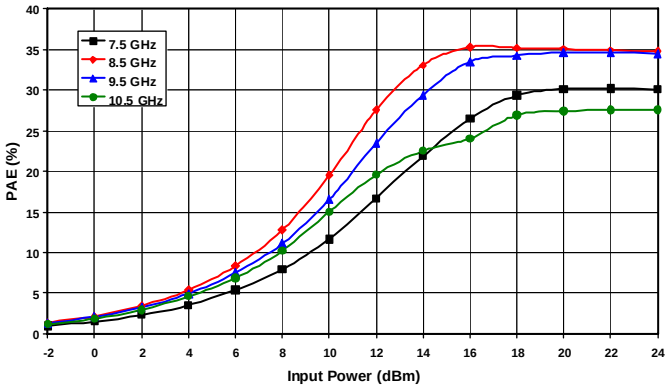

Fig 7. Power Added Efficiency vs. Input Power at V_D=10V.

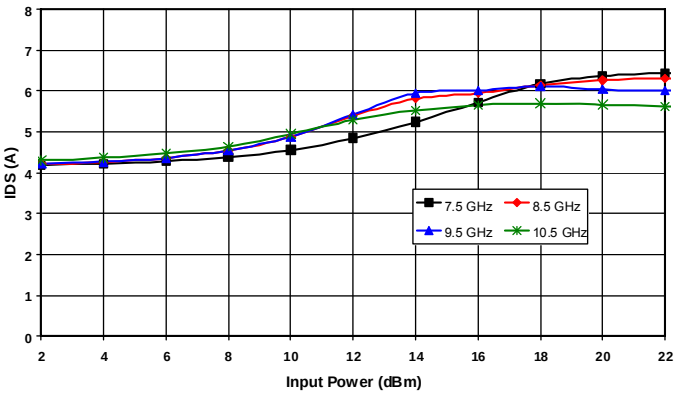

Figure 8. Drain Current vs. Input Power at V_{DD} = 10V

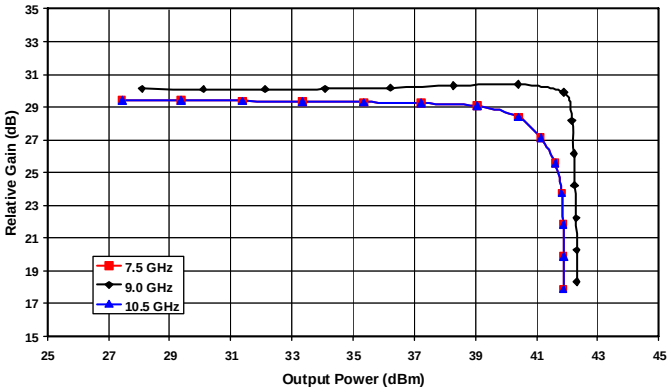

Figure 9. Relative Gain vs. Output Power by Frequency at V_D=8V and 25% IDSS

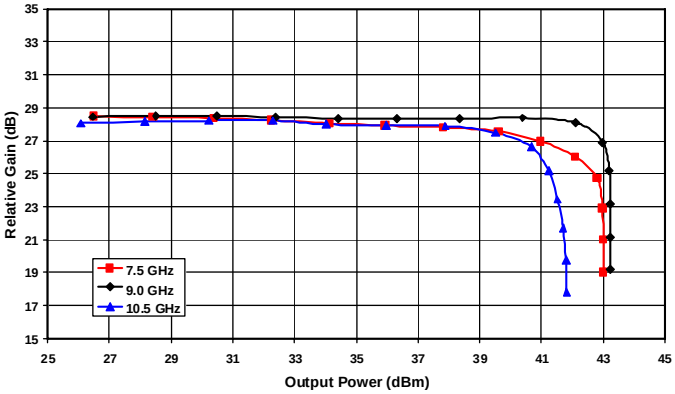

Figure 10. Relative Gain vs. Output Power by Frequency at V_D=10V and 25% IDSS

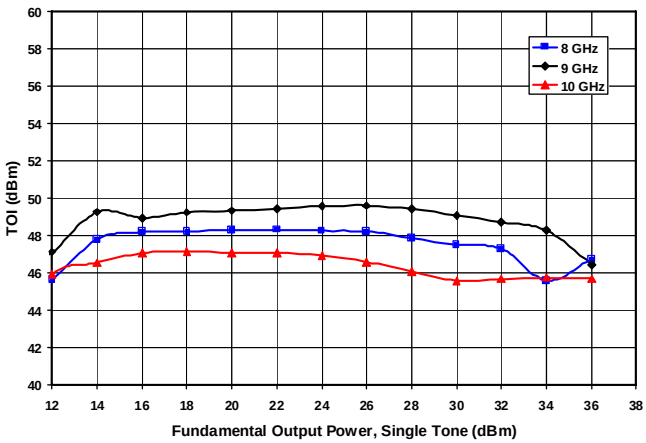

Figure 11. Third Order Intercept vs. Output Power and Frequency at 8V.

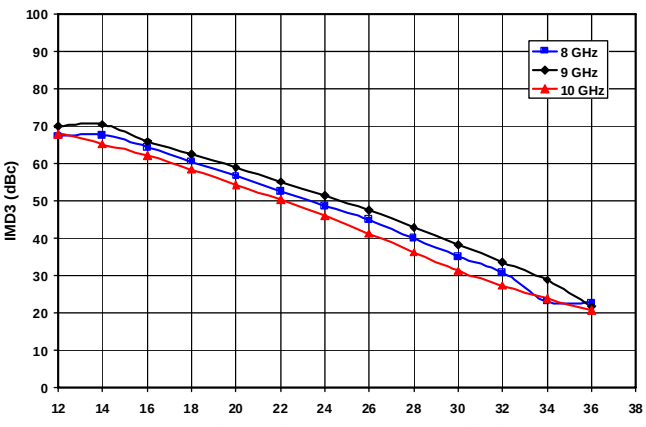

Figure 12. Third Order Intermod vs. Output Power and Frequency at 8V.

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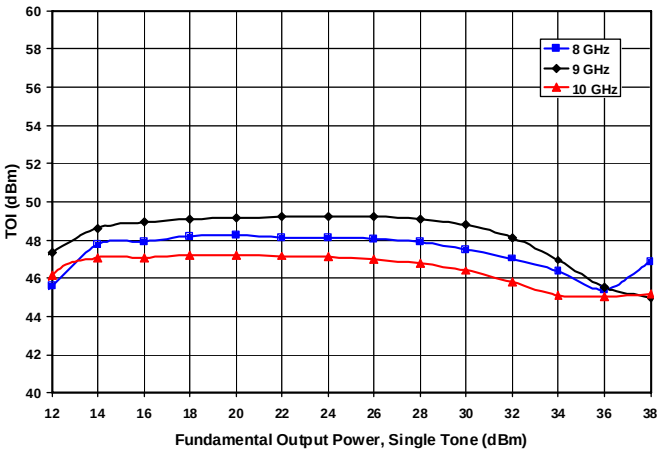

Figure 13. Third Order Intercept vs. Output Power and Frequency at 10V.

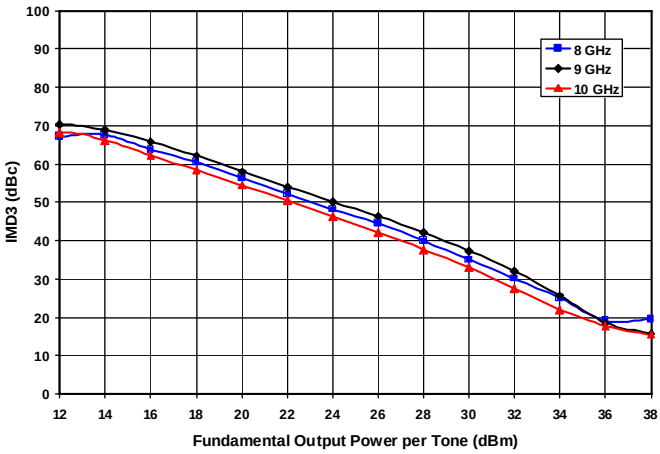

Figure 14. Third Order Intermod vs. Output Power and Frequency at 10V.

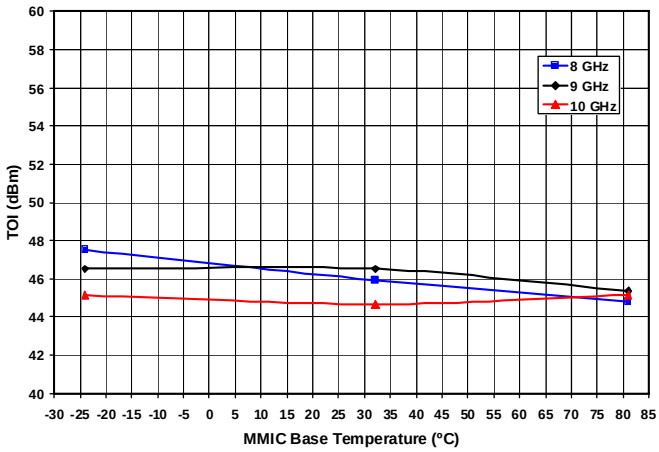

Figure 15. Third Order Intercept vs. Temperature and Frequency at 10V and P_{out} = 39 dBm DCL.

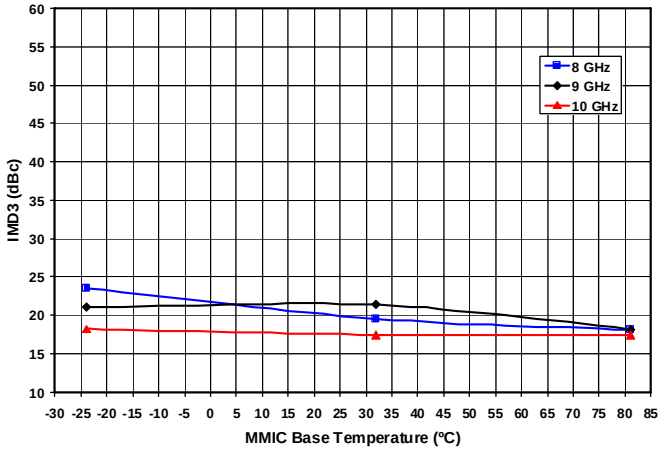

Figure 16. Third Order Intermod vs. Temperature and Frequency at 10V and P_{out} = 39 dBm DCL.

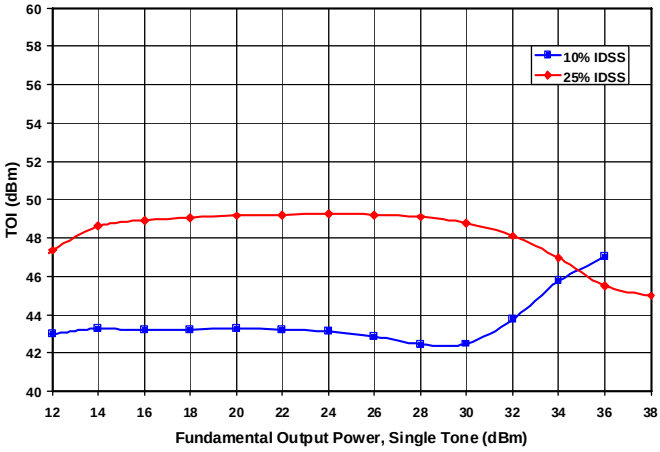

Figure 17. Third Order Intercept vs. Output Power and %IDSS at 10V and 9GHz.

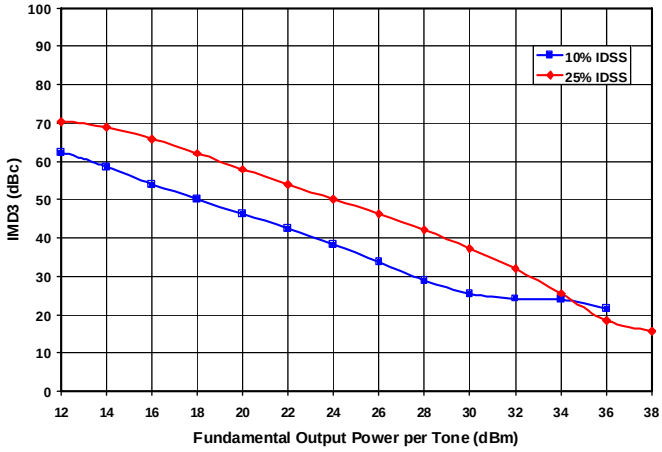

Figure 18. Third Order Intermod vs. Output Power and %IDSS at 10V and 9GHz.

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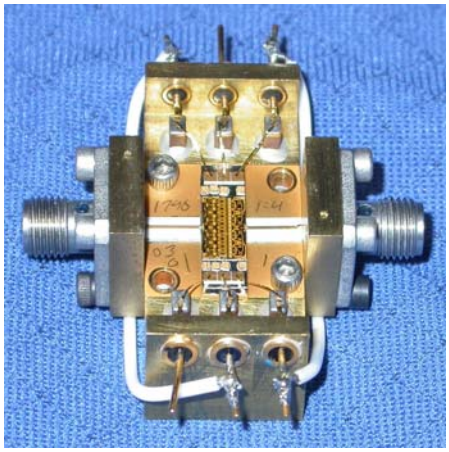

Figure 11. Fixture used to characterize MAAPGM0079-DIE under CW stimulus.

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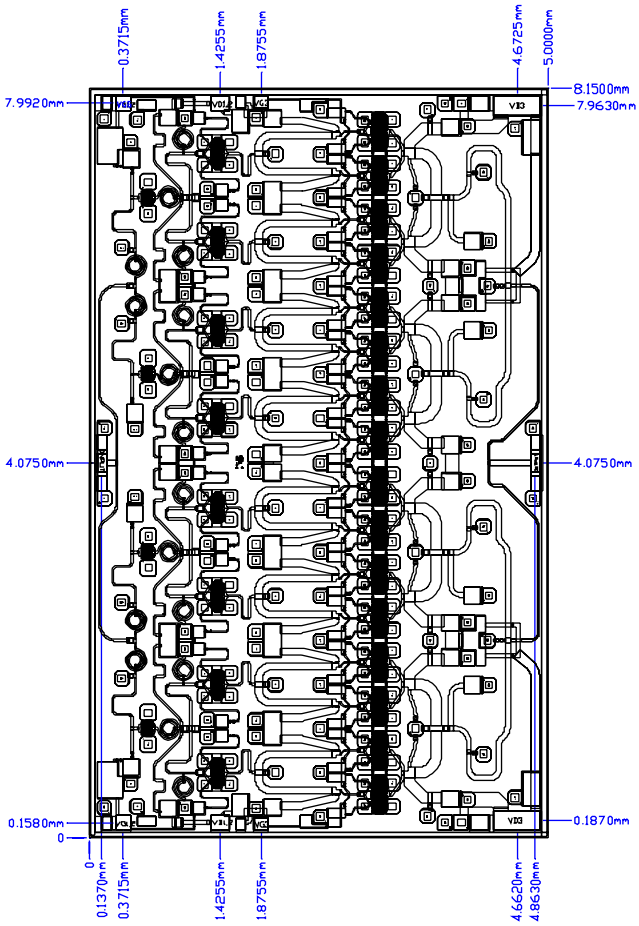
Mechanical Information

Chip Size: 5.000 x 8.150 x 0.075 mm (197 x 321 x 3 mils)



Chip edge to bond pad dimensions are shown to the center of the bond pad.

Figure 12. Die Layout

Bond Pad Dimensions

Pad	Size (µm)	Size (mils)
RF In and Out	100 x 200	4 x 8
DC Drain Supply Voltage $V_{D1,2}$	200 x 150	8 x 6
DC Drain Supply Voltage V_{D3}	500 x 200	20 x 8
DC Gate Supply Voltage $V_{G1,2}$	150 x 150	6 x 6
DC Gate Supply Voltage V_{G3}	150 x 125	6 x 5

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Assembly and Bonding Diagram

Thermal Management is critical on this part. Refer to Application Note AN3019 for applicable guidelines.

NOTE 1: All Application Notes may be accessed by going to http://www.macom.com/Application%20Notes/index.htm.

NOTE 2: In implementing the DC/ RF crossover shown, the following rules must applied.

1. the DC crossovers should approach and cross the RF trace at a 90 degree angle;
2. the printed DC traces that approach the RF line should be stopped 2 substrate heights from the RF line edge;
3. the rated current capability of the DC crossovers should be greater than the maximum current of the device; and
4. the wires or ribbons used to make the DC crossovers should clear the RF trace by ~ 1 substrate height.

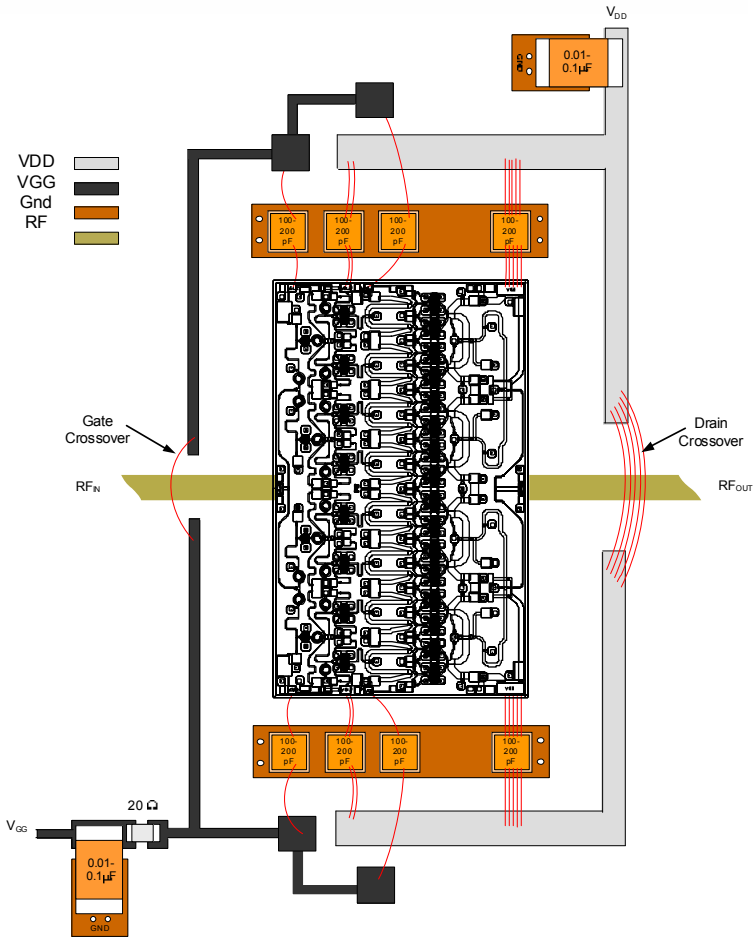


Figure 13. Recommended operational configuration. Wire bond as shown.

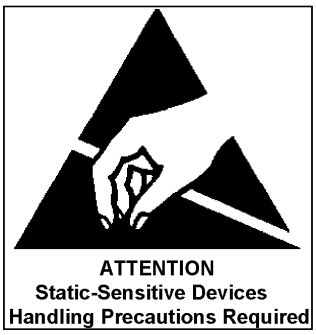
Die Handling:

Refer to Application Note AN3016.

Assembly Instructions:

Die Attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 310 °C to less than 7 minutes. Refer to Application Note AN3017 for more detailed information.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.



Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

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