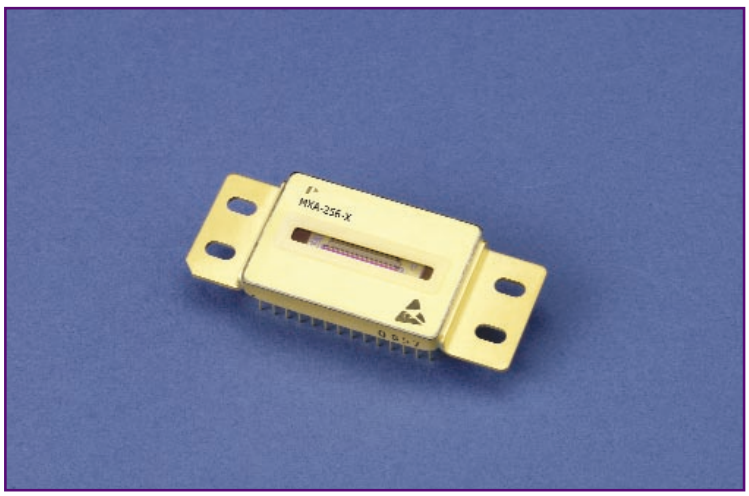
MXA-256-1, 2 (800-1700 nm)

Multiplexed InGaAs PIN Photodiode Array



Description

The MXA-256-X detector is a hybrid focal plane Indium Gallium Arsenide PIN photodiode array with wavelength response ranging from 800 nm to 1700 nm. The array has 256 elements configured in a linear orientation with standard pixel height of 0.5 mm. A buffered multiplexer provides individual CMOS amplifiers for each photodiode. The integrating amplifier maintains zero volt bias across each InGaAs photodiode, minimizing dark current and low frequency noise allowing for longer exposure times with increased sensitivity.

A static shift register scanning circuit sequentially selects sample-and-hold integrator output voltages which are proportional to input optical power. On-chip correlated double sampling (samples are taken at the beginning and end of integration, and are available at the output) removes integrator offsets and further suppresses low frequency noise. The array is available in a 28 pin dual-in-line package. Included in the assembly are a thermoelectric cooler (ΔT max > 60° C), silicon multiplexer and bypass capacitors. The MXA-256 series is available in two classes, the MXA-256-1 and the MXA-256-2. MXA-256-1 units exhibit no pixel drop-outs, while the MXA-256-2 devices exhibit five or fewer drop-outs (excluding the first and last pixels) that occur non-consecutively.

Applications

- Fiber optics
- DWDM power monitoring
- NIR spectroscopy
- NIR imaging
- NIR astronomy
- Far-field analysis

Features

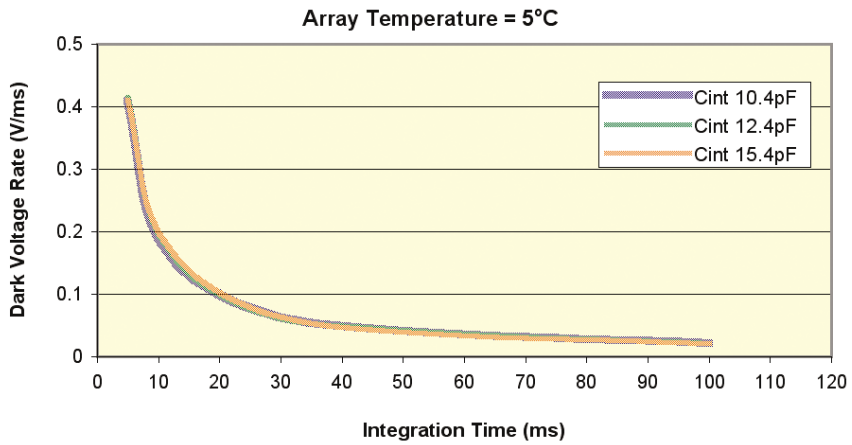
- 256 multiplexed elements
- High resolution (50 µm pitch)
- Variable Exposure Time: 10 micro sec. to 10 sec.
- Wide dynamic range (>39 dB)
- Correlated double sampling
- 800 - 1700 nm frequency response
- User selectable integration time

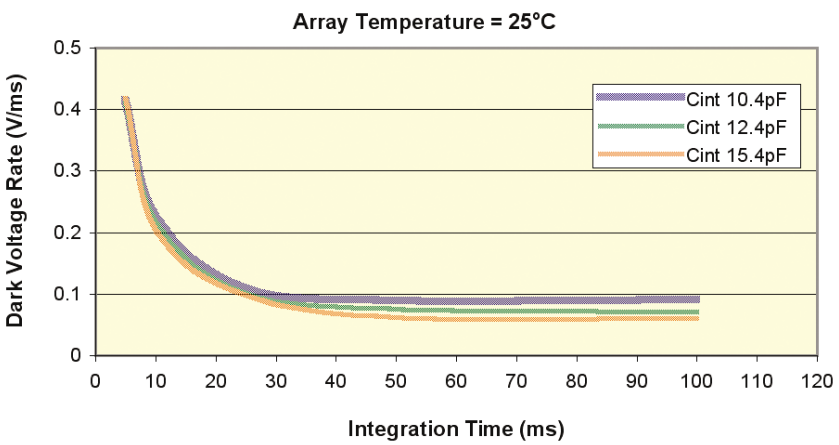
PerkinElmer™ optoelectronics

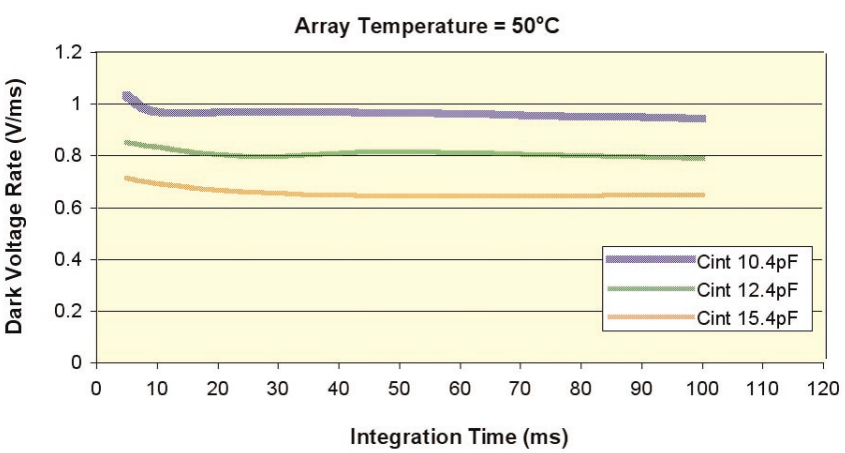
PARAMETER	CONDITIONS	MXA-256-X
Number of Elements		256
Pixel Height		0.5 mm
Pixel Pitch		50 µm
Package		28 pin with TE cooler
Dark Current		±5 pA
Response	Typical @ 1550 nm *Cint* = 15pF	65 mV/pJ (0.97 A/W onto 15 pF)
	Minimum @ 1550 nm *Cint* = 15pF	60 mV/pJ
Wavelength Response		800 to 1700 nm
Response Uniformity	@ 1550 nm	±10%
Pixel dropouts		Grade 1 = none, Grade 2 = maximum 5 No two consecutive, excluding first and last
Noise Equivalent Charge		1.8 fC
Full Well Capacity		435 M e- (4V onto 17.4 pF)
Read Noise	100 KHz readout	23500 e- (250 µV onto 15 pF)
NEP @ 25° C	t=1 msec	0.15 pW/√ Hz
	t=100 msec	0.025 pW/√ Hz
*Optical Dynamic Range @ 25° C	Typical for t ≤ 10 msec	40 dB(>13 bits)
Dark Voltage Rate @ 25° C, t=10 ms	Typical pixel	0.2 V/sec
	Maximum pixel	2.0 V/sec
Dark Voltage Rate @ 5° C, t=10 ms	Typical pixel	0.1 V/sec
	Maximum pixel	1.0 V/sec
Pixel readout rate		10 KHz to 1 MHz
TE cooler (One stage)	Hot side temperature 27° C	ΔT max = 64° C @ 1.8A, 8V ΔT = 45° C @ 0.85A, 5V (Nominal)
Storage Temperature		-40° C to 70° C
Case Operating Temperature range	No cooler	0 to 40° C
	With cooling	-5° C to 70° C

**Optical dynamic range defined as: 10 log (V_{max} - V_{dark})/V_{noise}*
V_{max} = 3.0 V @ V_{ref} = 3.0 volts

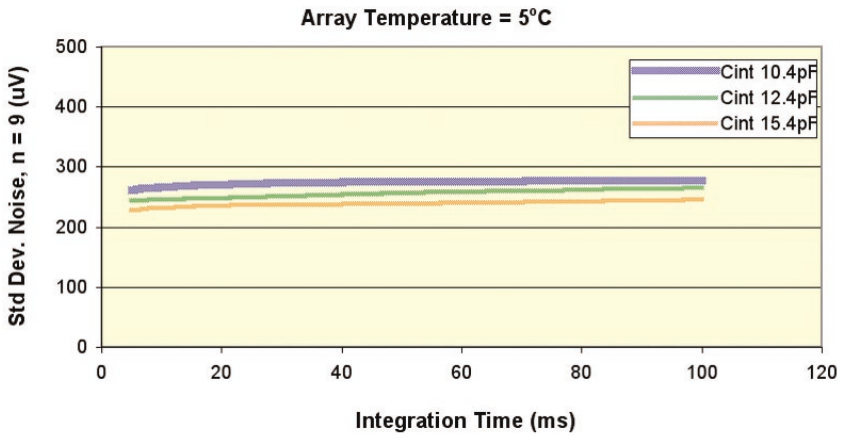
Dark Voltage Rate

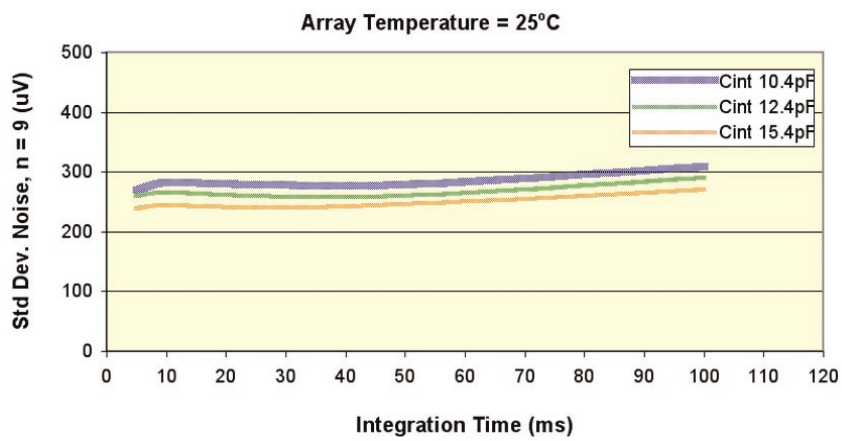


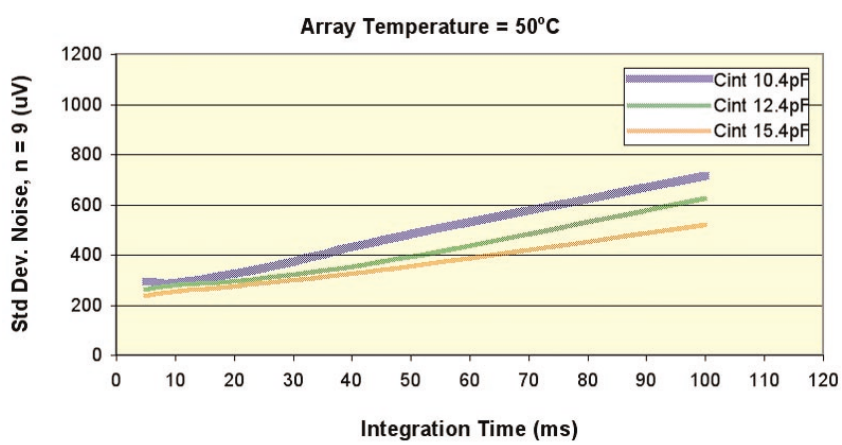




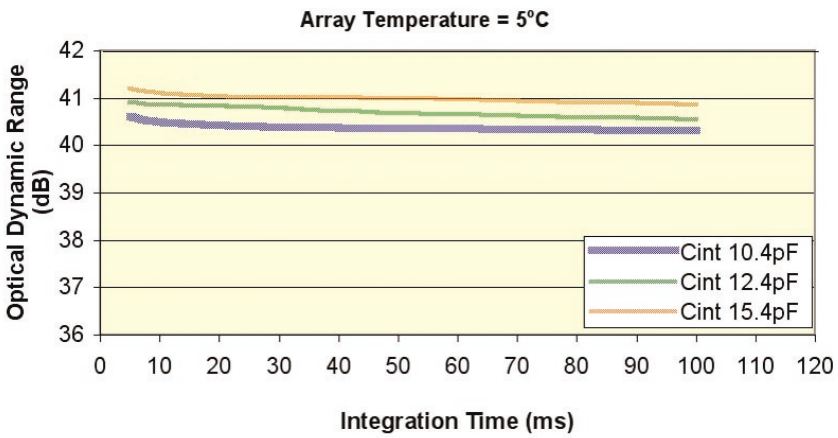
Standard Deviation Noise

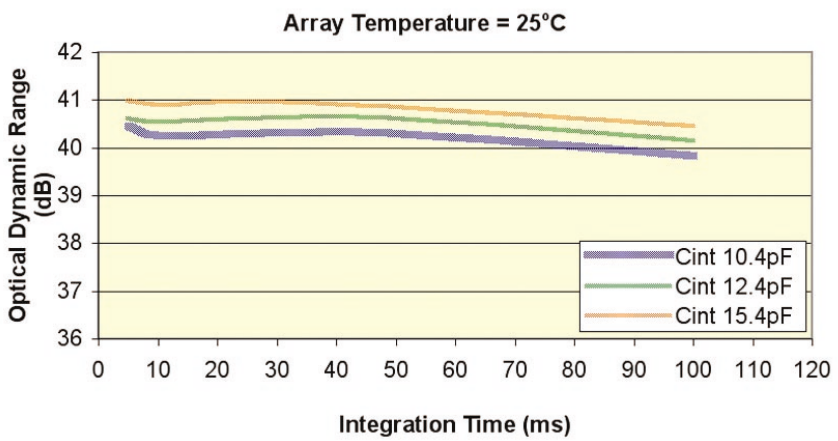


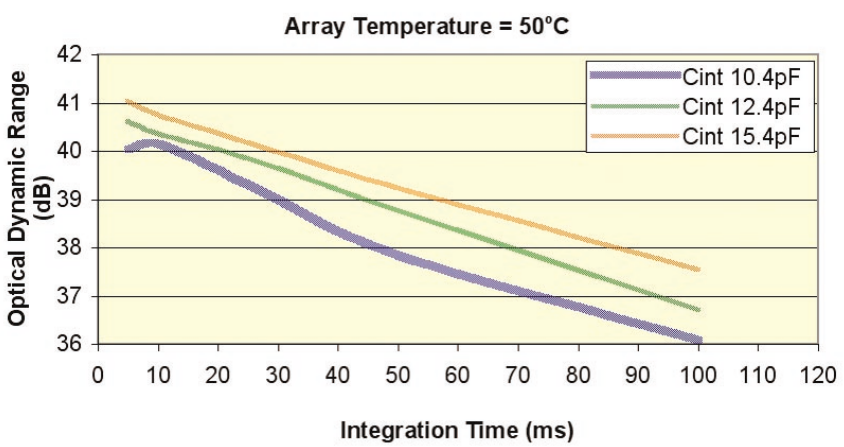




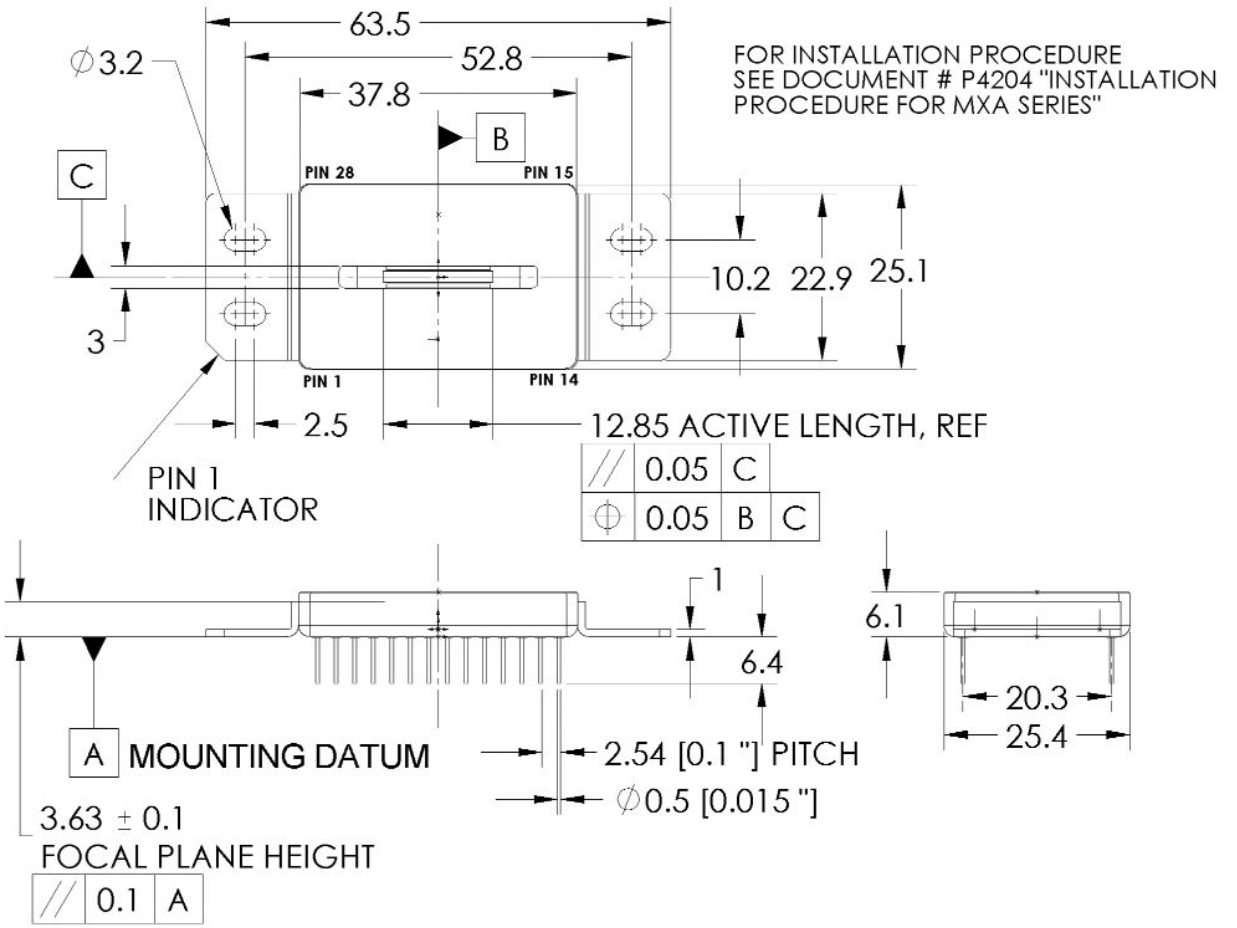
Optical Dynamic Range







MXA-256 Basic Dimensions



Units: mm	
DWG # SK-03491	Rev. 0

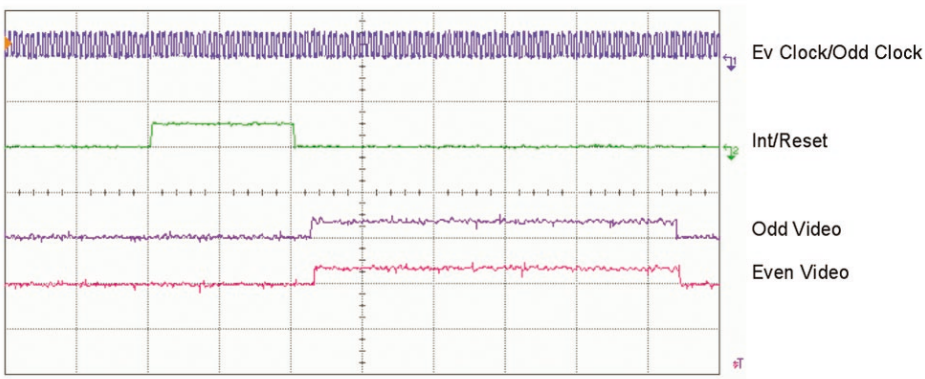
Timing Diagrams

Readout:

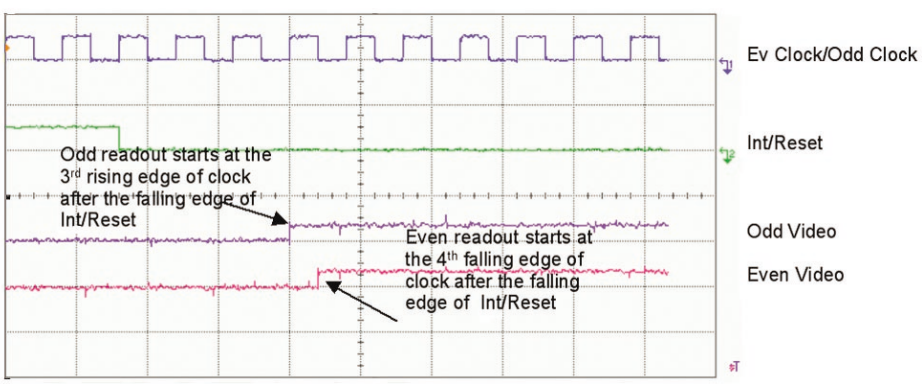
There are only two control signals required to operate the array, clock (Even and Odd) and Int/Reset. The clock is applied continuously to operate the array. During the high state of Int/Reset, the signal is integrated. The signals are read out during the low state of Int/Reset. The first sample (Video 1) is taken at the beginning of an integration. During Reset at the low state of Int/Reset and immediately prior to integration, the pixels are held at reset so that Video 1 captures the "zero" level.

The second sample (actual signal) is taken at the end of the integration and is available at pin Video 2.
The Video 1 and Video 2 are differentially amplified for correlated double sampling (CDS).
CDS removes integrator offsets and further suppresses low frequency noise.

Readout:



The first pixel of Odd Video appears at the third rising edge of the clock after the falling edge of Int/Reset. The first pixel of Even Video will appear at the fourth falling edge of the clock after the falling edge of Int/Reset.

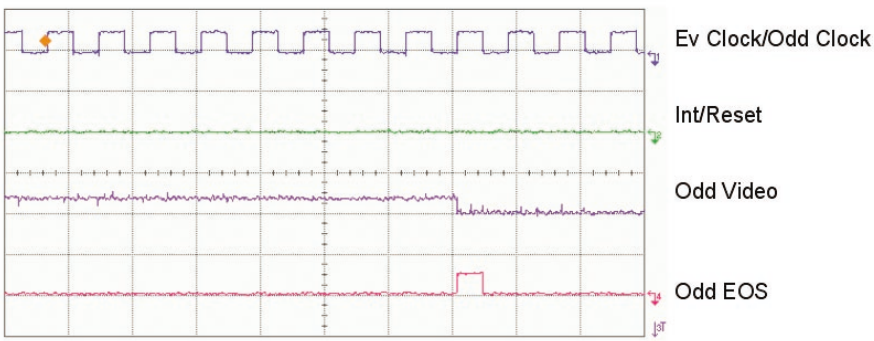


Timing Diagrams

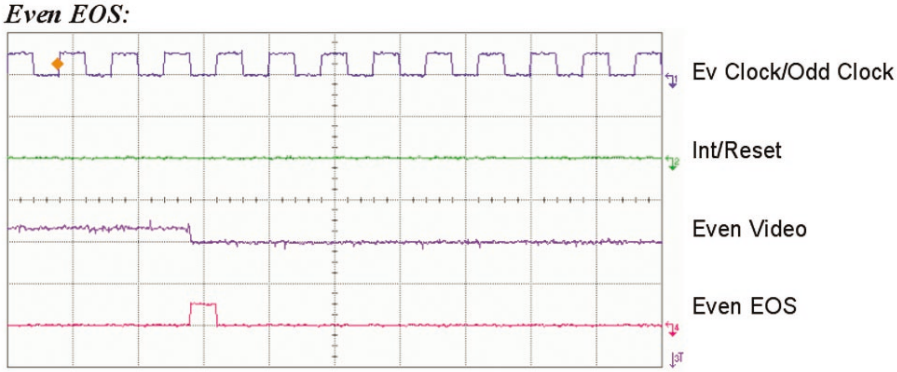
End of Signal:

The End of Signal (EOS) is a timing marker that indicates the end of the readout cycle. This occurs immediately after the end of readout. The EOS pulse is half the clock width and swings from VSS to VDD.

Odd EOS:



Even EOS:



Pin-Out Table

PIN #	FUNCTION	PIN #	FUNCTION
1	NC	28	NC
2	Cap 5pF Dis	27	Int/Reset
3	TEC +	26	TEC
4	CAP 2PF Dis	25	NC
5	NC	24	Cap 10pF Dis
6	Thermistor	23	Vdd
7	Thermistor	22	Vss
8	NC	21	Vref
9	Ev Clock	20	Odd Clock
10	NC	19	NC
11	Ev EOS	18	Odd EOS
12	NC	17	NC
13	Ev Video 1	16	Odd Video 1
14	Ev Video 2	15	Odd Video 2

Definitions

Cap 5pF Dis/ Cap 2pF Dis/ Cap 10pF Dis: These 3 TTL inputs control the size of the integration capacitance well. When the pin is at high state (default) that particular capacitor is added to the integration well size. When all the three pins are in the low state, the well size is set to the default base value of 0.4pF well size. This provides a variable size of integration well - 0.4, 2.4, 5.4, 7.4, 10.4, 12.4, 15.4, and 17.4pF

TEC +/- : These are the thermoelectric cooler pins

Thermistor: Thermistor resistance at 25°C: 5 KΩ

Ev Clock/Odd Clock: These are the timing and readout clock inputs. These are TTL compatible inputs. Both the Ev Clock and Odd Clock can be fed with the same clock, so the odd and even pixels are synchronized

Int/Reset: This is a TTL compatible input used to control the integration and reset of the integration well. Integration occurs when this signal is high and reset occurs when this signal is low. Readout occurs during the reset time. Care should be taken to provide enough time to readout the data. The Int/Reset signal does not have to be synchronous with the Ev Clock/Odd Clock.

Device Timing Parameters

Ev EOS/Odd EOS

The EvEOS and OdEOS are timing markers that indicate the end of the even and odd readout cycle respectively. These output pulses occur immediately after the end of readout. The pulse is half the clock width and swings from Vss to Vdd.

Ev Video1, 2 / Odd Video 1, 2

These are analog outputs of the multiplexer. These outputs are low impedance op-amp outputs and have a limited drive capability. They should be buffered as close as possible to the package output . The load on these outputs should not exceed 60 pF. Video 1 is the sample taken at the beginning of the integration and Video 2 at the end of integration. The output voltage swing is equal to Vref, which is from Vss+1. Please refer to the timing diagrams for the timing of these video signals.

Vref

This is the input voltage reference. The output voltage swing is equal to Vref. The range of Vref voltage is 2.5V to 3.5V, with current requirement of <5mA.

Power

- Vss - Ground
- Vdd - 5V, <50mA

Operating Conditions

Parameters	Units	Minimum	Typical	Maximum
VDD	V	4.90	5.00	5.20
VSS	V		0.00	
Vref	V	2.5	3.00	3.5
Clock				
High	V		VDD	
Low	V		VSS	
Frequency	Hz	10×10^3		1×10^6
Duty Cycle	%	45	50	55
Int/Reset				
High	V		VDD	
Low	V		VSS	
Cap Sel				
Select	V		VDD	
Deselect	V		VSS	
Output Impedance	KΩ		2.00	

Miscellaneous

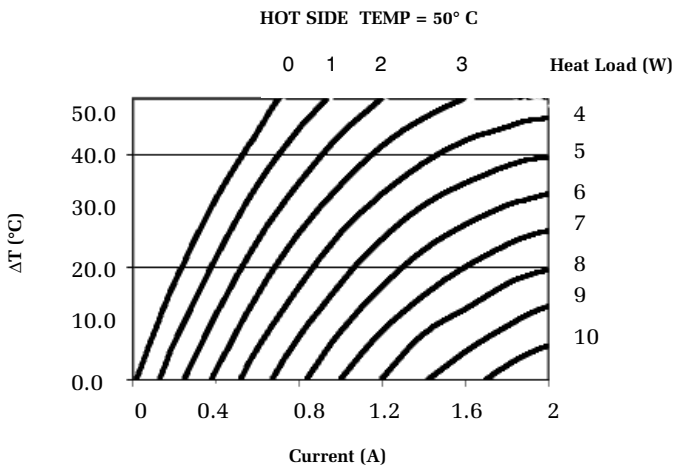
Thermistor:

To calculate thermistor resistance Rt at temperature T, use the following equation:

$$R_t = R_{25} \exp (A + B/T + C/T^2 + D/T^3)$$

$$R_{25} = 5K\Omega$$

Typical Thermoelectric Cooler



Temperature Range (°C)	A	B	C	D
-50 to 0	-1.4122478E+01	4.4136033E+03	-2.9034189E+04	-9.3875035+06
0 to 50	-1.4141963E+01	4.4307830E+03	-3.4078983+04	-8.8941929E+06
50 to 100	-1.4202172E+01	4.4975256E+03	-5.8421357E+04	-5.9658796E+06

Ordering Guide

MXA-256-1: No pixel dropouts

MXA-256-2: No two consecutive, excluding first and last pixel dropouts

PerkinElmer Optoelectronics reserve the right to change or amend specifications and/or configurations at any time without notice.

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