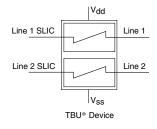


#### **General Information**

The TBU-PK Series of Bourns<sup>®</sup> TBU<sup>®</sup> products are low capacitance dual bidirectional high speed protection components, constructed using MOSFET semiconductor technology, and designed to protect against faults caused by short circuits, AC power cross, induction and lightning surges.

In addition to overcurrent protection, an added feature is the voltage monitoring on the two lines. If the voltage on the line drops below  $V_{SS}$  then the voltage will trigger the device to switch to the blocking state.

The TBU<sup>®</sup> high speed protector placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics will not be exposed to large voltages or currents during surge events. The TBU<sup>®</sup> device is provided in a surface mount DFN package and meets industry standard requirements such as RoHS and Pb Free solder reflow profiles.



#### **Agency Approval**

#### Industry Standards (in Conjunction with OVP Device)

 Description

 UL
 File Number: E315805

Solutions available for GR-1089-CORE, ITU-T and a combination of both.

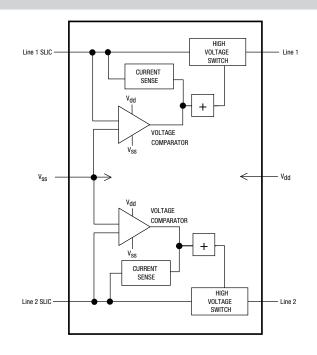
Symbol	Parameter	Part Number	Value	Unit	
V <sub>imp</sub>	Peak impulse voltage withstand with duration less than 10 ms	TBU-PK050-100-WH	500		
		TBU-PK060-100-WH	600	v	
		TBU-PK075-100-WH	750	v	
		TBU-PK085-100-WH	850		
V <sub>rms</sub>	Continuous A.C. RMS voltage	TBU-PK050-100-WH	300		
		TBU-PK060-100-WH	350	v	
		TBU-PK075-100-WH	400	v	
		TBU-PK085-100-WH	425		
Т <sub>ор</sub>	Operating temperature range		-55 to +125	°C	
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C	
T <sub>imax</sub>	Maximum junction temperature		+125	°C	
ESD	HBM ESD protection per IEC 61000-4-2 on line pads		±2	kV	

### Electrical Characteristics (@ T<sub>A</sub> = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Min.	Тур.	Max.	Unit
I <sub>trigger</sub>	Current required for the device to go from operating state to protected state	100	150	200	mA
R <sub>device</sub>	Series resistance of the TBU® device	65	80	90	Ω
R <sub>match</sub>	Package resistance matching of the TBU <sup>®</sup> device #1 - TBU <sup>®</sup> device #2		±0.5	±1.6	Ω
t <sub>block</sub>	Time taken for the device to go into current limiting			1	μs
lQ	Current through the triggered TBU® device with 50 Vdc circuit voltage	0.25	0.70	1.50	mA
I <sub>SS</sub>	Operating current with $V_{SS} = -50 V$		100		μA
V <sub>reset</sub>	Voltage below which the triggered TBU <sup>®</sup> device will transition to normal operating state	12	15	22	V
V <sub>to</sub>	Voltage threshold offset with 60 Hz applied voltage, with V <sub>ss</sub> -50 V (V <sub>ss</sub> - V <sub>lineSLIC</sub> )	-1.0		0.2	V
V <sub>ss</sub>	Operating voltage range relative to V <sub>dd</sub>	-180		-20	V
R <sub>th(j-l)</sub>	Junction to package pads - FR4 using minimum recommended pad layout		65		°C/W
R <sub>th(j-l)</sub>	Junction to package pads - FR4 using heat sink on board (6 cm <sup>2</sup> ) (0.5 in. <sup>2</sup> )		40		°C/W

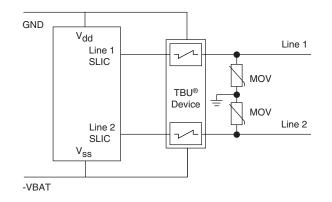
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**Functional Block Diagram** 



#### **Reference Application**

The TBU-PK Series are high-speed protectors used in voice/ VoIP SLIC applications. The maximum voltage rating of the TBU® device should never be exceeded. Where necessary, an OVP device should be employed to limit the maximum voltage. A cost-effective protection solution combines Bourns® TBU® protection devices with a pair of Bourns® MOVs. For bandwidth sensitive applications, a Bourns® GDT may be substituted for the MOV.



### **Basic TBU Operation**

The TBU<sup>®</sup> device, constructed using MOSFET semiconductor technology, placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics are not exposed to large voltages or currents during surge events. The TBU<sup>®</sup> device operates in approximately 1  $\mu$ s - once line current exceeds the TBU<sup>®</sup> device's trigger current I<sub>trigger</sub>. When operated, the TBU<sup>®</sup> device restricts line current to less than 1 mA typically. When operated, the TBU<sup>®</sup> device will block all system voltages and any other voltages including the surge in each case up to rated limits.

When the voltage on the SLIC output is driven below  $(V_{bat} - V_{to})$  the TBU-PK series device switches to the blocking state, regardless of output current in the device.

After the surge, the TBU<sup>®</sup> device resets when the voltage across the TBU<sup>®</sup> device falls to the V<sub>reset</sub> level. The TBU<sup>®</sup> device will automatically reset on lines which have no DC bias or have DC bias below V<sub>reset</sub> (such as unpowered signal lines).

If the line has a normal DC bias above  $V_{reset}$ , the voltage across the TBU<sup>®</sup> device may not fall below  $V_{reset}$  after the surge. In such cases, special care needs to be taken to ensure that the TBU<sup>®</sup> device will reset, with software monitoring as one method used to accomplish this. Bourns application engineers can provide further assistance.

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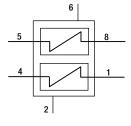
## Bourns® TBU® Device Solution

Industry Standard	Surge & AC Tests	TBU® Device P/N	Qty.	OVP Device P/N	Qty.
Telcordia GR-1089-CORE Intra-building	1500 V, 100 A 2/10 μs 120V RMS, 25 A, 900 s	TBU-PK050-100-WH	1	MOV-07D201K	2
Telcordia GR-1089-CORE	5000 V, 500 A 2/10 μs 120V RMS, 25 A, 900 s	TBU-PK060-100-WH	1	MOV-10D201K	2
Enhanced Intra-building	1500 V, 100 A 2/10 μs 277V RMS, 25 A, 900 s	TBU-PK085-100-WH	1	MOV-10D431K	2
ITU-T	1500 V, 40 $\Omega$ 10/700 $\mu s$ 4000 V, 40 $\Omega$ 10/700 $\mu s$ 230 V rms 10 $\Omega$ -1000 $\Omega$ , 900 s 600 V rms 600 $\Omega$ , 0.2 s	TBU-PK075-100-WH	1	MOV-10D361K	2
K.20, K.21, K.45 Basic	1500 V, 40 Ω 10/700 μs 4000 V, 40 Ω 10/700 μs 230 V rms 10 Ω -1000 Ω, 900 s 600 V rms 600 Ω, 1 s	TBU-PK060-100-WH	1	TISP4400M3BJ	2
ITU-T		TBU-PK085-100-WH	1	MOV-10D391K	2
K.20, K.21, K.45 Enhanced	1500 V, 40 Ω 10/700 μs 6000 V, 40 Ω 10/700 μs 230 V rms 10 Ω -1000 Ω, 900 s 600 V rms 600 Ω, 0.2 s 600 V rms 600 Ω, 1 s 1500 V rms, 200 Ω 2s	TBU-PK060-100-WH	1	TISP4500H3BJ	2
Telcordia GR-1089-CORE Intra-building and ITU-T K.20, K.21, K.45 Enhanced	$\begin{array}{c} 5000 \text{ V}, 500 \text{ A } 2/10 \ \mu\text{s} \\ 120\text{V RMS}, 25 \text{ A}, 900 \ \text{s} \\ 1500 \text{ V}, 40 \ \Omega \ 10/700 \ \mu\text{s} \\ 6000 \text{ V}, 40 \ \Omega \ 10/700 \ \mu\text{s} \\ 230 \text{ V rms} \ 10 \ \Omega \ -1000 \ \Omega, 900 \ \text{s} \\ 600 \text{ V rms} \ 600 \ \Omega, 0.2 \ \text{s} \\ 600 \text{ V rms} \ 600 \ \Omega, 1 \ \text{s}^* \\ 1500 \text{ V rms}, 200 \ \Omega \ 2\text{ s}^* \end{array}$	TBU-PK085-100-WH	1	MOV-10D391K	2

 $^{\ast}$  GDT Special Test Protector with DC breakdown (DCBD) of less than 330 V .

Note: The Le9500, Le9520 and Le9530 (VE950 series) require a 200 mA  $I_{trigger}$  TBU<sup>®</sup> device for normal operation.

## **Device Pin Out**



### Pad Designation

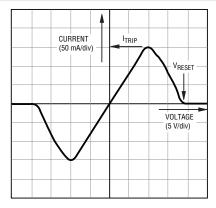
r da Beolghadon					
Pad #	Pin Out				
1	Line 1				
2	V <sub>dd</sub>				
3	Not Used				
4	Line 1 SLIC				
5	Line 2 SLIC				
6	V <sub>SS</sub>				
7	Not Used				
8	Line 2				

Specifications are subject to change without notice. Customers should verify actual device performance in their specific applications.

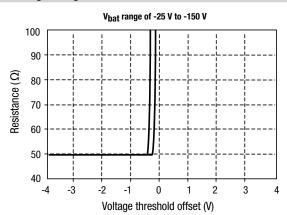
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## **Performance Graphs**

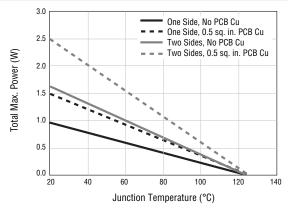
## Typical V-I Characteristics (TBU-PK085-100-WH)



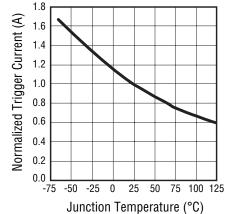
#### **Tracking Voltage Characteristics**



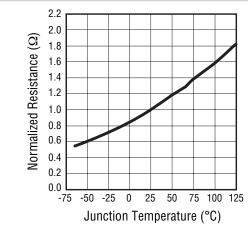
## **Power Derating Curve**



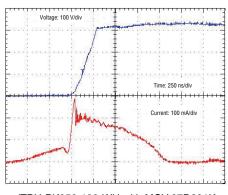
Typical Trigger Current vs. Temperature



### Typical Resistance vs. Temperature



#### **Typical Surge Response**

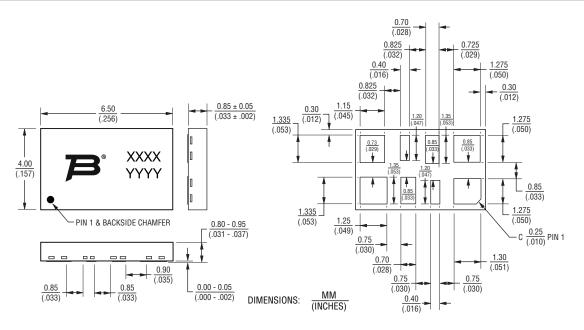


(TBU-PK050-100-WH with MOV-07D201K Using 1800 V 1.2/50 ms Surge Pulse)

Specifications are subject to change without notice. Customers should verify actual device performance in their specific applications.

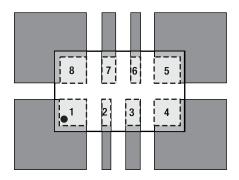
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**Product Dimensions** 



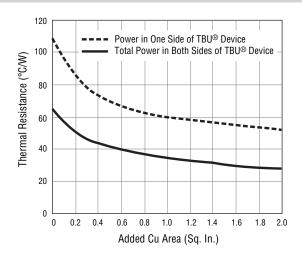
#### **Recommended Pad Layout**

TBU<sup>®</sup> protectors have matte-tin termination finish. The suggested layout should use Non-Solder Mask Define (NSMD). The recommended stencil thickness is 0.10-0.12 mm (.004-.005 in.) with a stencil opening size 0.025 mm (.0010 in.) less than the device pad size. As when heat sinking any power device, it is recommended that wherever possible, extra PCB copper area is allowed. For minimum parasitic capacitance, do not allow any signal, ground or power signals beneath any of the pads of the device.



Dark grey areas show added PCB copper area for better thermal resistance.

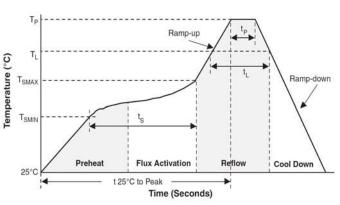
Thermal Resistance vs Additional PCB Cu Area



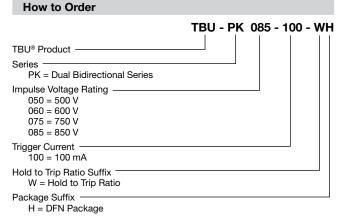
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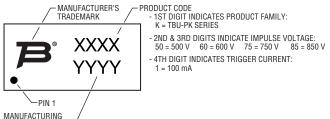
### **Reflow Profile**

Profile Feature	Pb-Free Assembly	
Average Ramp-Up Rate (Tsmax to Tp)	3 °C/sec. max.	
Preheat - Temperature Min. (Tsmin) - Temperature Max. (Tsmax) - Time (tsmin to tsmax)	150 °C 200 °C 60-180 sec.	
Time maintained above: - Temperature (TL) - Time (tL)	217 °C 60-150 sec.	
Peak/Classification Temperature (Tp)	260 °C	
Time within 5 °C of Actual Peak Temp. (tp)	20-40 sec.	
Ramp-Down Rate	6 °C/sec. max.	
Time 25 °C to Peak Temperature	8 min. max.	



## **Typical Part Marking**





MANUFACTURING DATE CODE - 1ST DIGIT INDICATES THE YEAR'S 6-MONTH PERIOD. - 2ND DIGIT INDICATES THE WEEK NUMBER IN THE 6-MONTH PERIOD. - 3RD & 4TH DIGITS INDICATE SPECIFIC LOT FOR THE WEEK.

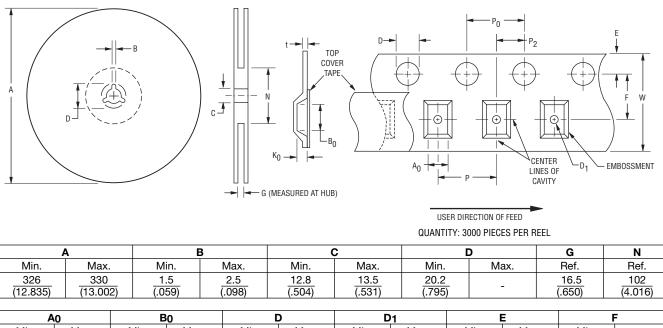
6-MONTH PERIOD CODES:

. C = JAN-JUN 2010 A = JAN-JUN 2009 B = JUL-DEC 2009 D = JUL-DEC 2010

E = JAN-JUN 2011 F = JUL-DEC 2011

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### **Packaging Specifications**



	F	
Max.	Min.	max.
1.85	7.4	7.6
) (.073)	(.291)	(.299)
t	W	
Max.	Min.	Max.
0.35	15.7	16.3
) (.014)	(.618)	(.642)
	i         1.85 (.073)           t         Max.           i         0.35	1.85         7.4           (.073)         (.291)           t         W           Max.         Min.           0.35         15.7

DIMENSIONS:  $\frac{MM}{(INCHES)}$ 

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REV. 01/11

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