DALLAS SEMICONDUCTOR

DS1251Y
4096K NV SRAM with Phantom Clock

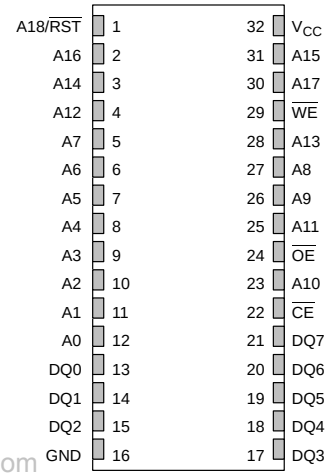
FEATURES

- Real time clock keeps track of hundredths of seconds, minutes, hours, days, date of the month, months, and years
- 512K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains calendar operation and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month; valid up to 2100
- Standard 32–pin JEDEC pinout
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C
- Over 10 years of data retention in the absence of power
- Available in 120 ns and 150 ns access time

ORDERING INFORMATION

DS1251Y–120	120 ns access
DS1251Y–150	150 ns access

PIN ASSIGNMENT



32–PIN ENCAPSULATED PACKAGE
740 MIL FLUSH

PIN DESCRIPTION

A_0–A_{18}	–	Address Inputs
$\overline{CE}$	–	Chip Enable
GND	–	Ground
DQ_0–DQ_7	–	Data In/Data Out
V_{CC}	–	Power (+5V)
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable
$\overline{RST}$	–	Reset

DESCRIPTION

The DS1251Y 4096K NV SRAM with Phantom Clock is a fully static nonvolatile RAM (organized as 512K words by 8 bits) with a built–in real time clock. The DS1251Y has a self–contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out–of–tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock.

The Phantom Clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Phantom Clock operates in either 24–hour or 12–hour format with an AM/PM indicator.

RAM READ MODE

The DS1251Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 17 address inputs (A0–A18) defines which of the 512K bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times and states are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

RAM WRITE MODE

The DS1251Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1251Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by approximately 4.0 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become “don’t care” and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power–up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

PHANTOM CLOCK OPERATION

Communication with the Phantom Clock is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64–bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the Phantom Clock, and memory access is inhibited.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Write Enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the Phantom Clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64–bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the Phantom Clock. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the Phantom Clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a Phantom Clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64–bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64–bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the Phantom Clock to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

PHANTOM CLOCK REGISTER INFORMATION

The Phantom Clock information is contained in eight registers of 8–bits, each of which is sequentially accessed one bit at a time after the 64–bit pattern recognition sequence has been completed. When updating the Phantom Clock registers, each register must be handled in groups of 8–bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the Phantom Clock register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all eight registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

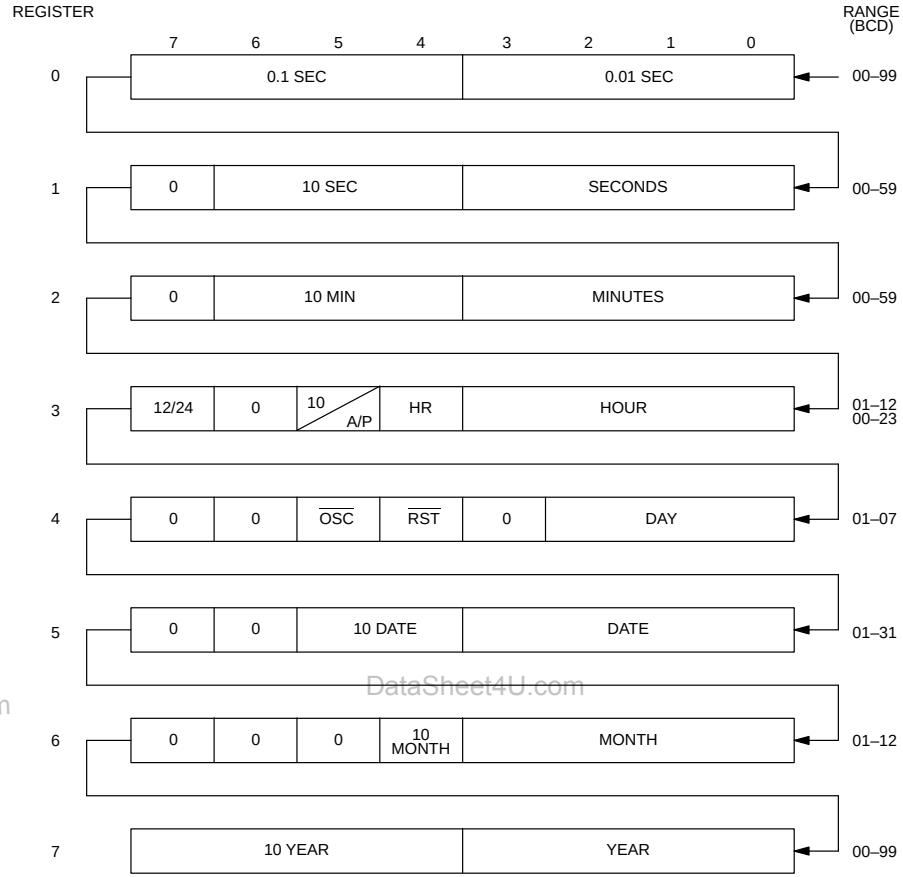
PHANTOM CLOCK REGISTER DEFINITION Figure 1

	7	6	5	4	3	2	1	0	HEX VALUE
BYTE 0	1	1	0	0	0	1	0	1	C5
BYTE 1	0	0	1	1	1	0	1	0	3A
BYTE 2	1	0	1	0	0	0	1	1	A3
BYTE 3	0	1	0	1	1	1	0	0	5C
BYTE 4	1	1	0	0	0	1	0	1	C5
BYTE 5	0	0	1	1	1	0	1	0	3A
BYTE 6	1	0	1	0	0	0	1	1	A3
BYTE 7	0	1	0	1	1	1	0	0	5C

NOTE:

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Phantom Clock is less than 1 in 10^{19}. This pattern is sent to the Phantom Clock LSB to MSB.

PHANTOM CLOCK REGISTER DEFINITION Figure 2



AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12– or 24–hour mode select bit. When high, the 12–hour mode is selected. In the 12–hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24–hour mode, bit 5 is the second 10-hour bit (20–23 hours).

OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logic 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logic 0, a low input on the $\overline{\text{RESET}}$ pin will cause the Phantom Clock to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds (See Note 13)

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	
Input Logic 0	V_{IL}	–0.3		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	–1.0		+1.0	µA	12
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	–1.0		+1.0	µA	
Output Current @ 2.4 volts	I_{OH}	–1.0			mA	
Output Current @ 0.4 volts	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2 volts	I_{CCS1}		5.0	10	mA	
Standby Current $\overline{CE}$ = V_{CC} – 0.5 volts	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC} = 200 ns	I_{CC01}			85	mA	

DC TEST CONDITIONS

Outputs are open; all voltages are referenced to ground.

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

MEMORY AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	DS1251Y-120		DS1251Y-150		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	
Access Time	t_{ACC}		120		150	ns	
$\overline{OE}$ to Output Valid	t_{OE}		60		70	ns	
$\overline{CE}$ to Output Valid	t_{CO}		120		150	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		40		70	ns	5
Output Hold from Address Change	t_{oH}	5		5		ns	
Write Cycle Time	t_{WC}	120		150		ns	
Write Pulse Width	t_{WP}	90		100		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	20		20		ns	
Output High Z from $\overline{WE}$	t_{ODW}		40		70	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	50		60		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	20		20		ns	4

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0–3 volts

Timing Measurement Reference Levels
Input: 1.5 volts
Output: 1.5 volts
Input Pulse Rise and Fall Times: 5 ns

PHANTOM CLOCK AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{CE}$ Access Time	t_{CO}			100	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output High Z	t_{OD}			40	ns	5
$\overline{OE}$ to Output High Z	t_{ODO}			40	ns	5
Read Recovery	t_{RR}	20			ns	
Write Cycle Time	t_{WC}	120			ns	
Write Pulse Width	t_{WP}	100			ns	
Write Recovery	t_{WR}	20			ns	10
Data Setup Time	t_{DS}	40			ns	11
Data Hold Time	t_{DH}	10			ns	11
$\overline{CE}$ Pulse Width	t_{CW}	100			ns	
$\overline{RESET}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ High to Power–Fail	t_{PF}			0	ns	

POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power–Down	t_{PD}	0			µs	
V_{CC} Slew from 4.5V to 0 volts ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to 4.5 volts ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power–Up	t_{REC}			2	ms	

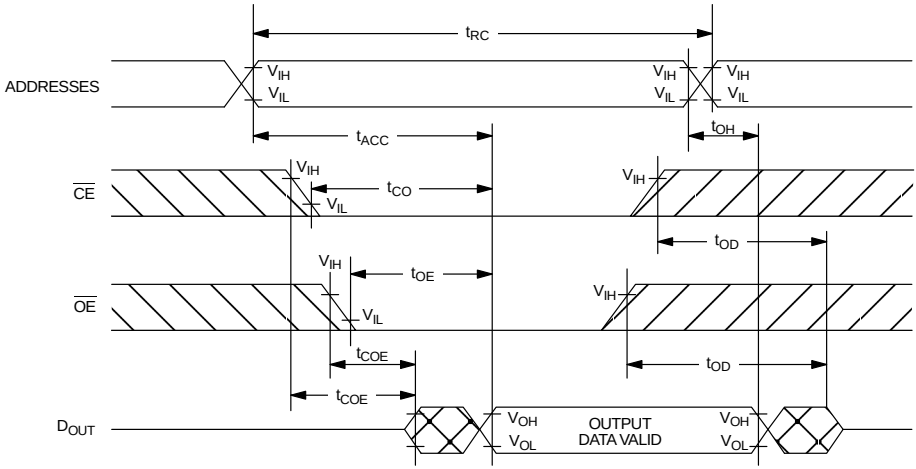
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

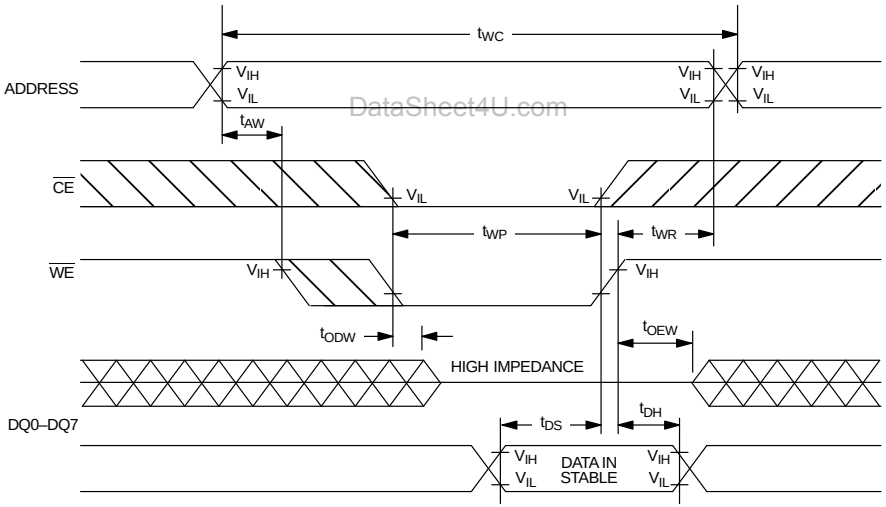
WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

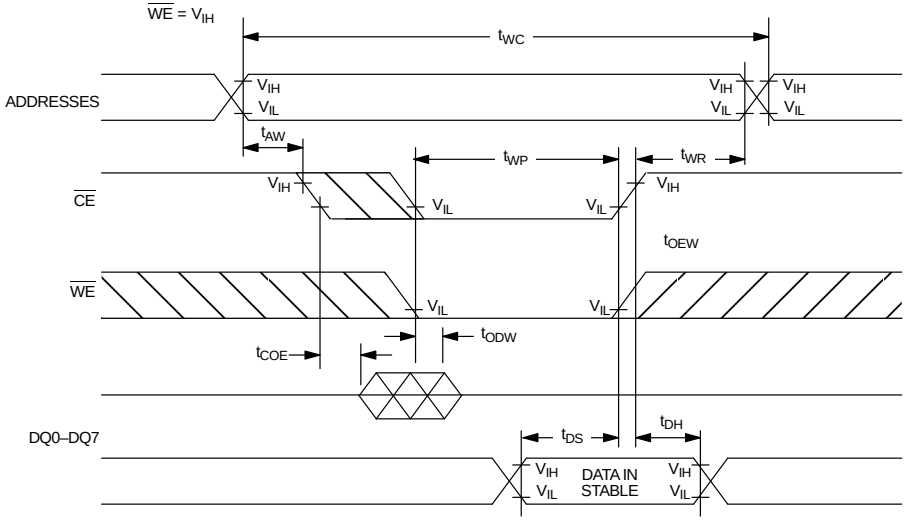
MEMORY READ CYCLE (NOTE 1)



MEMORY WRITE CYCLE 1 (NOTES 2, 6, AND 7)

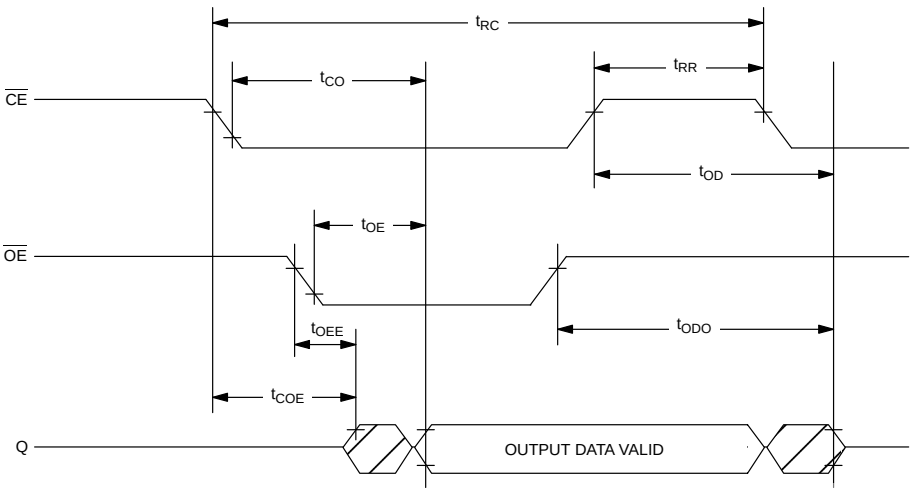


MEMORY WRITE CYCLE 2 (NOTES 2 AND 8)

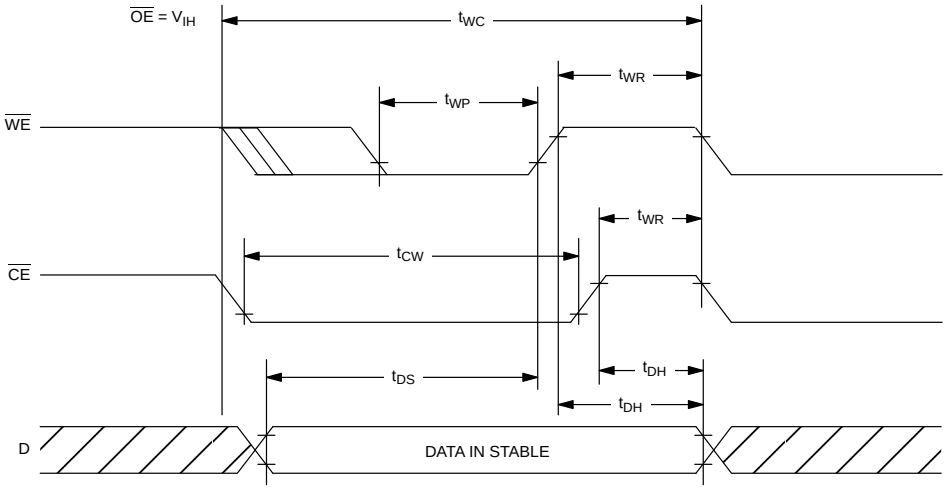


RESET FOR PHANTOM CLOCK

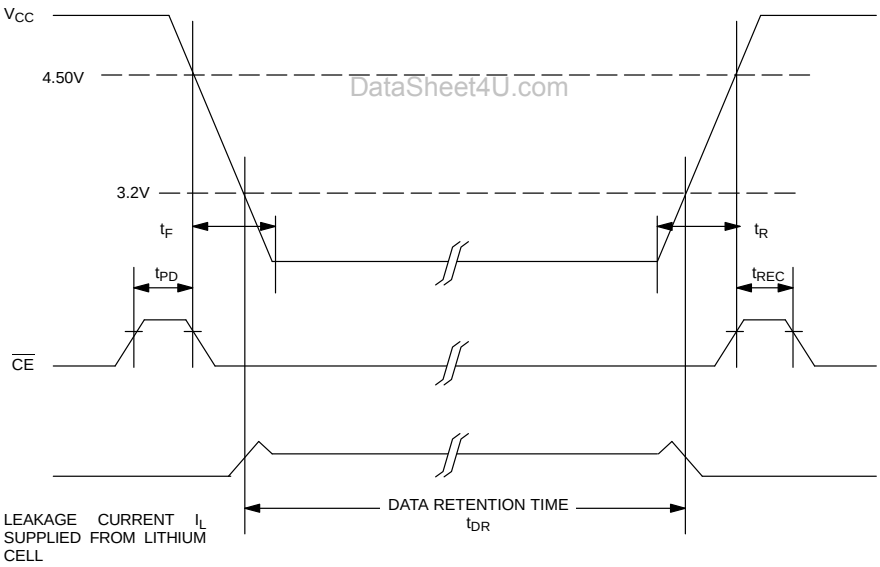
READ CYCLE TO PHANTOM CLOCK



WRITE CYCLE TO PHANTOM CLOCK



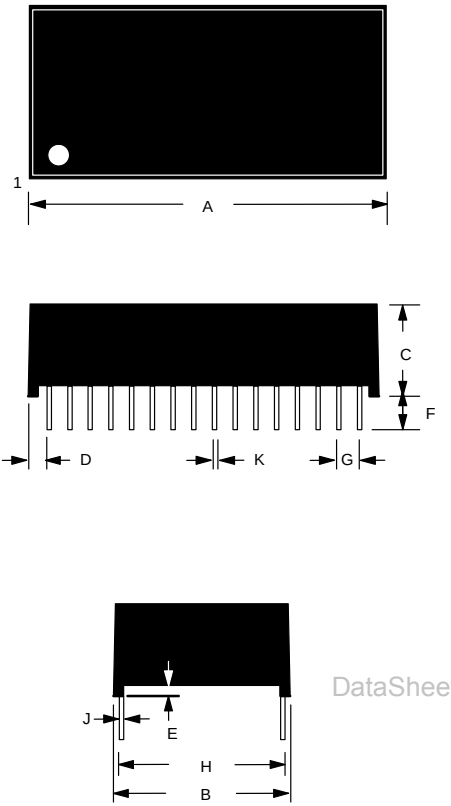
POWER-DOWN/POWER-UP CONDITION



NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 50 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} with the clock oscillator running.
10. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
11. t_{DH} and t_{DS} are a function of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
12. $\overline{RST}$ (Pin1) has an internal pull–up resistor.
13. Real–Time Clock Modules can be successfully processed through conventional wave–soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used.

DS1251Y 4096K NV SRAM WITH PHANTOM CLOCK



PKG	32–PIN	
DIM	MIN	MAX
A IN.	1.720	1.740
MM	43.69	44.20
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.090	0.120
MM	2.29	3.05
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53