MC10H680, MC10H680

4-Bit Differential ECL Bus to TTL Bus Transceiver

The MC10H/100H680 is a dual supply 4–bit differential ECL bus to TTL bus transceiver. It is designed to allow the system designer to no longer be limited in bus speed associated with standard TTL busses. Using a differential ECL Bus will increase the frequency of operation and increase noise immunity.

Both the TTL and the ECL ports are capable of driving a bus. The ECL outputs have the ability to drive 25 Ω, allowing both ends of the bus line to be terminated in the characteristic impedance of 50 Ω. The TTL outputs are specified to source 15 mA and sink 48 mA, allowing the ability to drive highly capacitive loads.

The ECL output levels are V_{OH} approximately equal to –1.0 V and V_{OL} cutoff equal to –2.0 V (VTT). When the ECL ports are disabled both EIOx and EIOxB go to the V_{OL} cutoff level. The ECL input receivers have special circuitry which detects this disabled condition, prevents oscillation, and forces the TTL output to the low state. The noise margin in this disabled state is greater than 600 mV. Multiple ECL V_{CCO} pins are utilized to minimize switching noise.

The TTL ports have standard levels. The TTL input receivers have PNP input devices to significantly reduce loading. Multiple TTL power and ground pins are utilized to minimize switching noise.

The control pins (EDIR and ECEB) of the 10H version is compatible with MECL 10H ECL logic levels. The control pins of the 100H version are compatible with 100K levels.

- Differential ECL Bus (25 Ω) I/O Ports
- High Drive TTL Bus I/O Ports
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- Direction and Chip Enable Control Pins

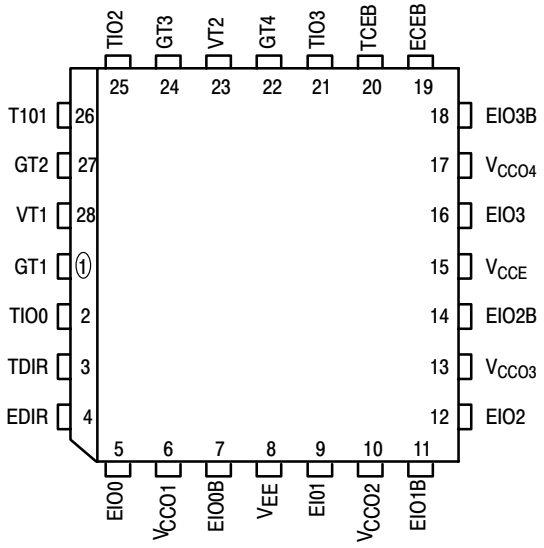

Figure 1. Pinout: 28–Lead PLCC (Top View)

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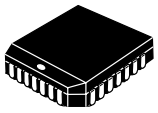
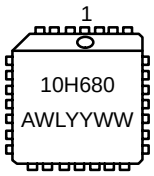


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H680FN	PLCC–28	37 Units/Rail
MC100H680FN	PLCC–28	37 Units/Rail

PIN DESCRIPTIONS

Pin	Symbol	Function
1	GT1	TTL Ground 1
2	TIO0	TTL I/O Bit 0
3	TDIR	TTL Direction Control
4	EDIR	ECL Direction Control
5	EIO0	ECL I/O Bit 0
6	VCCO1	ECL VCC 1 (0V) – Outputs
7	EIO0B	ECL I/O Bit 0 Bar
8	VEE	ECL Supply (–5.2/–4.5V)
9	EIO1	ECL I/O Bit 1
10	VCCO2	ECL VCC 2 (0V) – Outputs
11	EIO1B	ECL I/O Bit 1 Bar
12	EIO2	ECL I/O Bit 2
13	VCCO3	ECL VCC 3 (0V) – Outputs
14	EIO2B	ECL I/O Bit 2 Bar
15	VCCE	ECL VCC (0V)
16	EIO3	ECL I/O Bit 3
17	VCCO4	ECL VCC 4 (0V) – Outputs
18	EIO3B	ECL I/O Bit 3 Bar
19	ECEB	ECL Chip Enable Bar Control
20	TCEB	TTL Chip Enable Bar Control
21	TIO3	TTL I/O Bit 3
22	GT4	TTL Ground 4
23	VT2	TTL Supply 2 (5V)
24	GT3	TTL Ground 3
25	TIO2	TTL I/O Bit 2
26	TIO1	TTL I/O Bit 1
27	GT2	TTL Ground 2
28	VT1	TTL Supply 1 (5V)

TRUTH TABLE

TDIR — Direction Control TTL Levels
EDIR — Direction Control ECL Levels
TCEB — Chip Enable Bar Control TTL Levels
ECEB — Chip Enable Bar Control ECL Levels
TIN — TTL Input
TOUT — TTL Output
EIN — ECL Input
EINB — ECL Input Bar
EOUT — ECL Output
EOUTB — ECL Output Bar

H — HIGH
L — LOW
LC — ECL Low Cutoff (VTT = –2.0 V)
X — Don’t Care
Z — High Impedance

ECEB	TCEB	EDIR	TDIR	EIN	EINB	EOUT	EOUTB	TIN	TOUT	COMMENTS
H	X	X	X	X	X	LC	LC	X	Z	ECL and TTL Outputs Disabled
X	H	X	X	X	X	LC	LC	X	Z	ECL and TTL Outputs Disabled
L	L	H	X	H	LC			NA	H	ECL to TTL Direction
L	L	H	X	LC	H			NA	L	ECL to TTL Direction
L	L	H	X	LC	LC			NA	L	ECL to TTL Direction (L–L Cond.)
L	L	X	H	H	LC			NA	H	ECL to TTL Direction
L	L	X	H	LC	H			NA	L	ECL to TTL Direction
L	L	X	H	LC	LC			NA	L	ECL to TTL Direction (L–L Cond.)
L	L	L	L	NA	NA	H	LC	H		TTL to ECL Direction
L	L	L	L	NA	NA	LC	H	L		TTL to ECL Direction

ABSOLUTE RATINGS (Do not exceed):

Power Supply Voltage	V_{EE} (ECL)	–8.0 to 0	Vdc
Power Supply Voltage	V_{CCT} (TTL)	–0.5 to +7.0	Vdc
Input Voltage	V_I (ECL) V_I (TTL)	0.0 to V_{EE} –0.5 to +7.0	Vdc
Disabled 3–State Output	V_{out} (TTL)	0.0 to V_{CCT}	Vdc
Output Source Current Continuous	I_{out} (ECL)	100	mAdc
Output Source Current Surge	I_{out} (ECL)	200	mAdc
Storage Temperature	T_{stg}	–65 to 150	°C
Operating Temperature	T_{amb}	0.0 to +75	°C

ECL DC CHARACTERISTICS: V_{CCT} = +5.0 V ±10%, V_{EE} = –5.2 ±5% (10H Version); V_{EE} = –4.2 V to –5.5 V (100H Version)

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	Supply Current/ECL		–110		–110		–110	mA	
I_{INH}	Input HIGH Current		225		145		145	μA	
I_{INL}	Input LOW Current	0.5		0.5		0.3		μA	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	–1100 –2.1	–840 –2.03	–1100 –2.1	–810 –2.03	–1100 –2.1	–735 –2.03	mV V	25 Ω to –2.1 V

CONTROL INPUTS ONLY

10H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 ±10%, V_{EE} = –5.2 ±5%

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1170 –1950	–840 –1480	–1130 –1950	–810 –1480	–1070 –1950	–735 –1450	mV	

CONTROL INPUTS ONLY

100H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 ±10%, V_{EE} = –4.2 V to –5.5 V

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	–1165 –1810	–880 –1475	mV	

TTL DC CHARACTERISTICS: V_{CCT} = +5.0 V ±10%, V_{EE} = –5.2 ±5% (10H Version); V_{EE} = –4.2 V to –5.5 V (100H Version)

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Standard Input Standard Input	2.0	 0.8	2.0	 0.8	2.0	 0.8	Vdc	
V_{IK}	Input Clamp		–1.2		–1.2		–1.2	Vdc	I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0 mA I_{OH} = –15 mA
V_{OL}	Output LOW Voltage		0.55		0.55		0.55	V	I_{OL} = 48 mA
I_{IH}*	TTL (Input HIGH) TTL (Input HIGH)		20 100		20 100		20 100	μA	V_{in} = 2.7 V V_{in} = 7.0 V
I_{IL}*	TTL (Input LOW)		–0.6		–0.6		–0.6	mA	V_{in} = 0.5 V
I_{CCL}	Supply Current		75		75		75	mA	
I_{CCH}	Supply Current		70		70		70	mA	
I_{CCZ}	Supply Current		70		70		70	mA	
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0 V

* NOTE: TTL Control Inputs only

TTL I/O DC CHARACTERISTICS ONLY

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
$I_{IH/IOZH}$ $I_{IL/IOZL}$	Output Disable Current		70 200		70 200		70 200	μA	V_{OUT} = 2.7 V V_{OUT} = 0.5 V

ECL TO TTL DIRECTION / AC TEST

Test Symbol	Parameter	Waveforms	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	2, 4	2.7	4.8	2.7	4.8	2.7	4.8	ns	C_L = 50 pF
t_{PZH} t_{PZL}	ECEB to Output Enable Time	2, 5, 6	3.5 3.5	6.5 6.0	3.5 3.5	6.5 6.0	3.7 3.7	6.7 6.4	ns	C_L = 50 pF
t_{PHZ} t_{PLZ}	ECEB to Output Disable Time	2, 5, 6	3.5 3.5	8.6 6.5	3.5 3.5	8.6 6.5	3.7 3.7	8.8 7.3	ns	C_L = 50 pF
t_{PZH} t_{PZL}	TCEB to Output Enable Time	2, 5, 6	5.7 5.4	7.7 6.9	5.7 5.4	7.7 6.9	5.9 5.9	7.9 7.4	ns	C_L = 50 pF
t_{PHZ} t_{PLZ}	TCEB to Output Disable Time	2, 5, 6	4.0 4.0	8.5 5.8	4.1 4.2	8.4 6.0	4.2 4.7	8.3 6.5	ns	C_L = 50 pF
t_r/t_f	1.0 to 2.0 Vdc	3	0.4	1.5	0.4	1.5	0.4	1.5	ns	C_L = 50 pF

TTL TO ECL DIRECTION / AC TEST

Test Symbol	Parameter	Waveforms	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	1, 4	1.8	4.6	1.8	4.6	2.0	4.9	ns	25 Ω to –2.0 V
t_{PLH} t_{PHL}	ECEB to Output	1, 4	2.9	5.1	3.0	5.2	3.4	5.7	ns	25 Ω to –2.0 V
t_{PLH} t_{PHL}	TCEB to Output	1, 4	3.4	6.3	3.5	6.6	3.8	7.4	ns	25 Ω to –2.0 V
t_r/t_f	Output Rise/Fall Time 20%–80%	1, 3	1.0	3.4	1.0	3.4	1.0	3.4	ns	25 Ω to –2.0 V

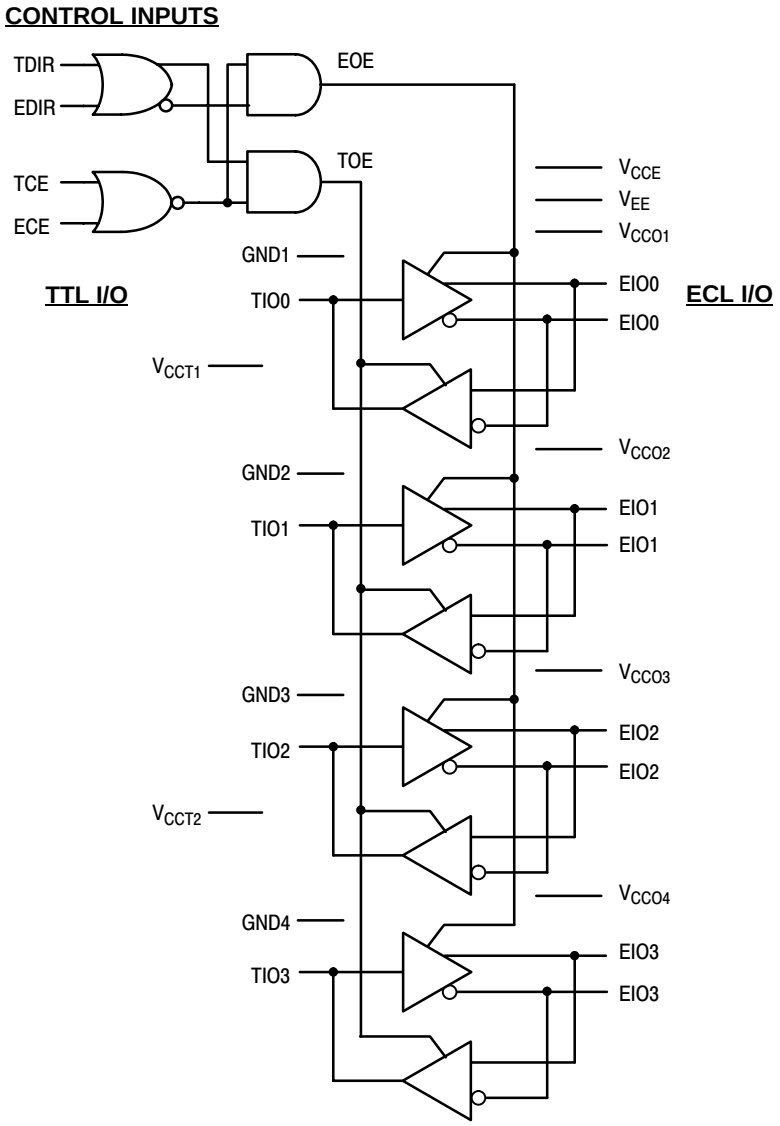


Figure 2. Block Diagram

SWITCHING CIRCUIT

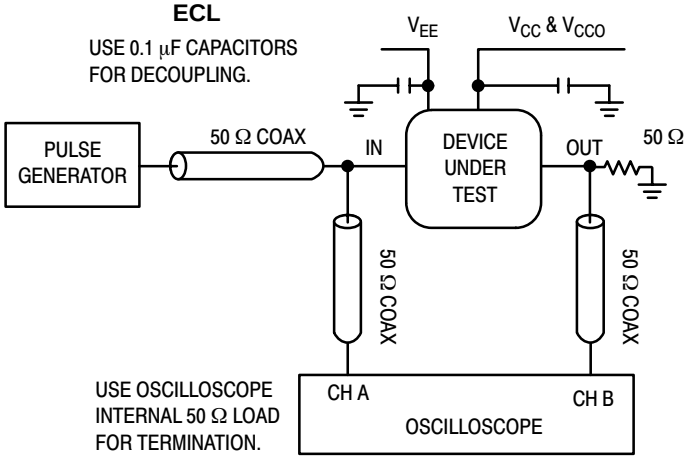


Figure 3. Switching Circuit ECL

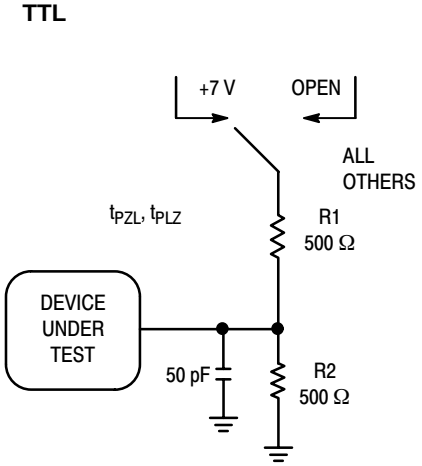


Figure 4.

WAVEFORMS

ECL/TTL

Figure 5. WAVEFORMS: Rise and Fall Times

ECL/TTL

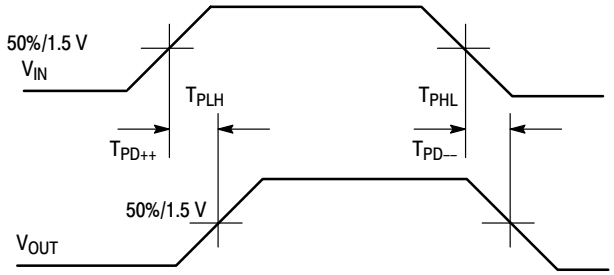


Figure 6. Propagation Delay — Single Ended

TTL

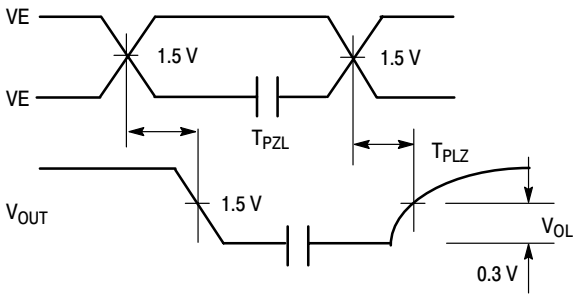


Figure 7. 3–State Output Low Enable and Disable Times

TTL

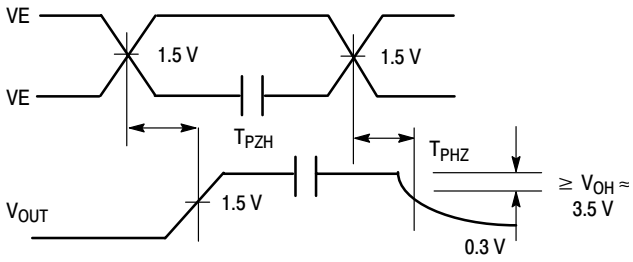


Figure 8. 3–State Output High Enable and Disable Times

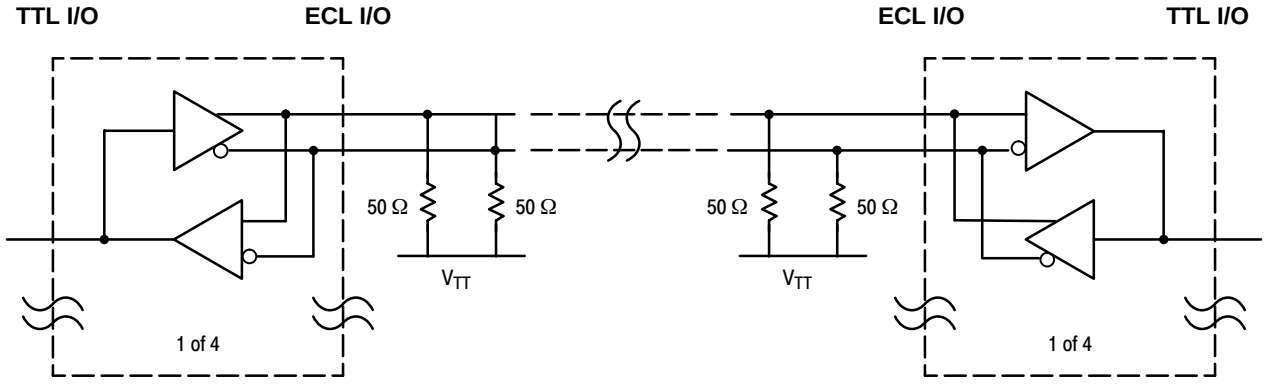
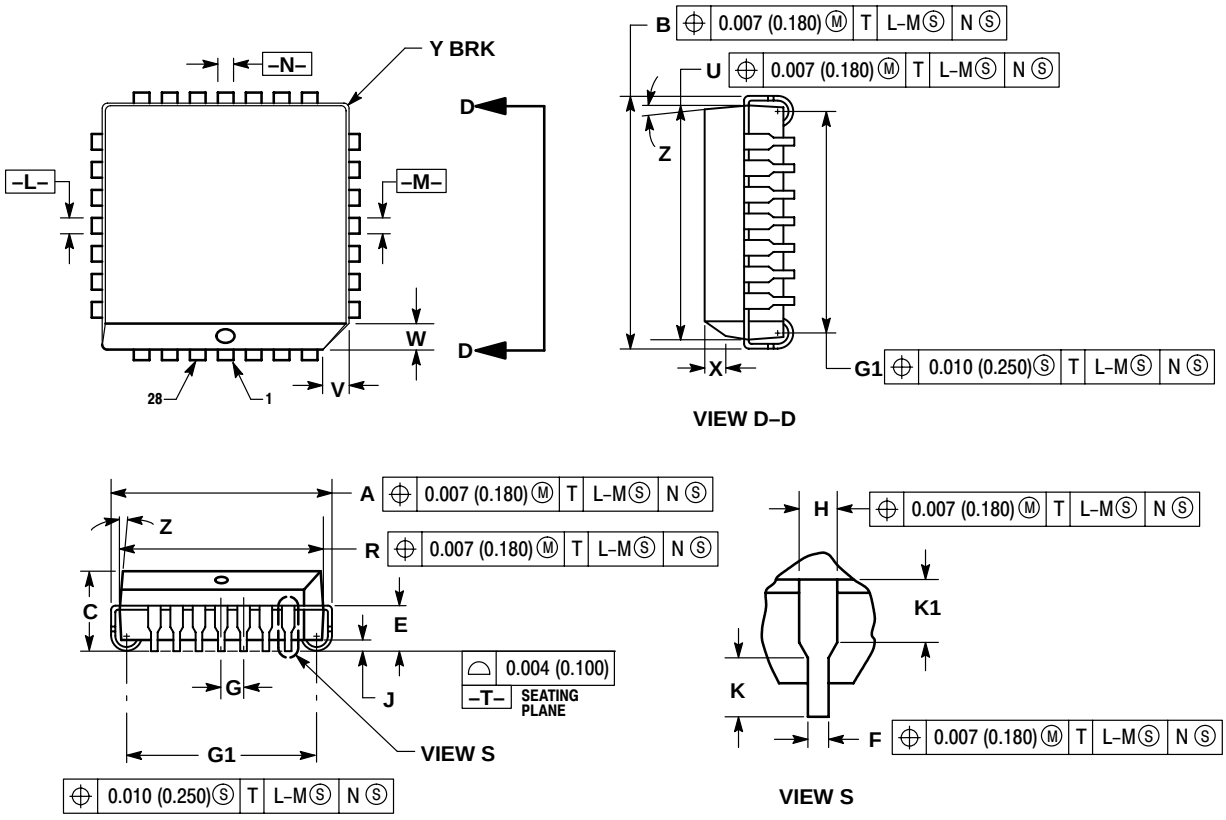


Figure 9. ECL I/O Link Application Recommended Termination
(Directional Control Intentionally Excluded)

PACKAGE DIMENSIONS

PLCC–28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE E



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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