To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

RENESAS

DATA SHEET

MOS FIELD EFFECT TRANSISTOR
2SK4212A

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK4212A is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 8.0 mΩ MAX. (V_{GS} = 10 V, I_D = 30 A)
  $R_{DS(on)2}$ = 14 mΩ MAX. (V_{GS} = 4.5 V, I_D = 20 A)
- Low total gate charge
  Q_G = 24 nC TYP. (V_{DD} = 15 V, V_{GS} = 10 V, I_D = 30 A)
- 4.5 V drive available
- Avalanche capability ratings

ORDERING INFORMATION

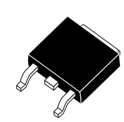
PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SK4212A-ZK-E1-AY Note	Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZK) typ. 0.27 g
2SK4212A-ZK-E2-AY Note			

Note Pb-free (This product does not contain Pb in external electrode).

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±48	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±125	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	35	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	16	A
Single Avalanche Energy Note2	E_{AS}	25	mJ

(TO-252)



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 0.1 mH

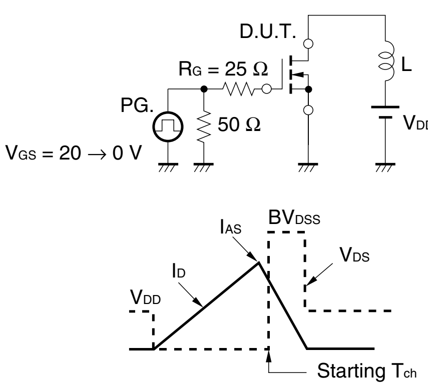
Document No. D20285EJ1V0DS00 (1st edition)
Date Published March 2010 NS
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

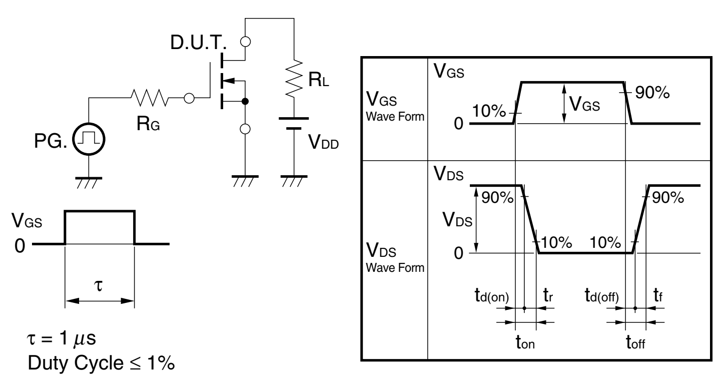
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.5		3.0	V
Forward Transfer Admittance Note	$\lvert y_{fs} \rvert$	V_{DS} = 5 V, I_D = 12 A	9	19		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 30 A		7.2	8.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 20 A		10.4	14	mΩ
Input Capacitance	C_{iss}	V_{DS} = 15 V,		1200		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		180		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		100		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 30 A,		14		ns
Rise Time	t_r	V_{GS} = 10 V,		11		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 3 Ω		43		ns
Fall Time	t_f			10		ns
Total Gate Charge	Q_G	V_{DD} = 15 V,		24		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V,		3		nC
Gate to Drain Charge	Q_{GD}	I_D = 30 A		7		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 30 A, V_{GS} = 0 V		0.89	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 30 A, V_{GS} = 0 V,		21		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		12		nC

Note Pulsed

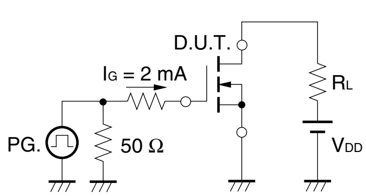
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

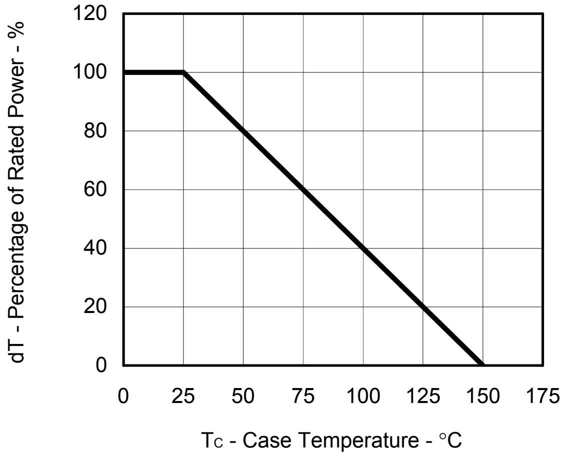


TEST CIRCUIT 3 GATE CHARGE

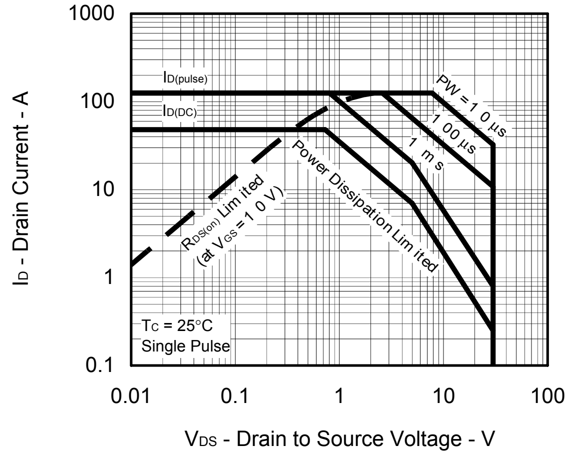


TYPICAL CHARACTERISTICS (T_A = 25°C)

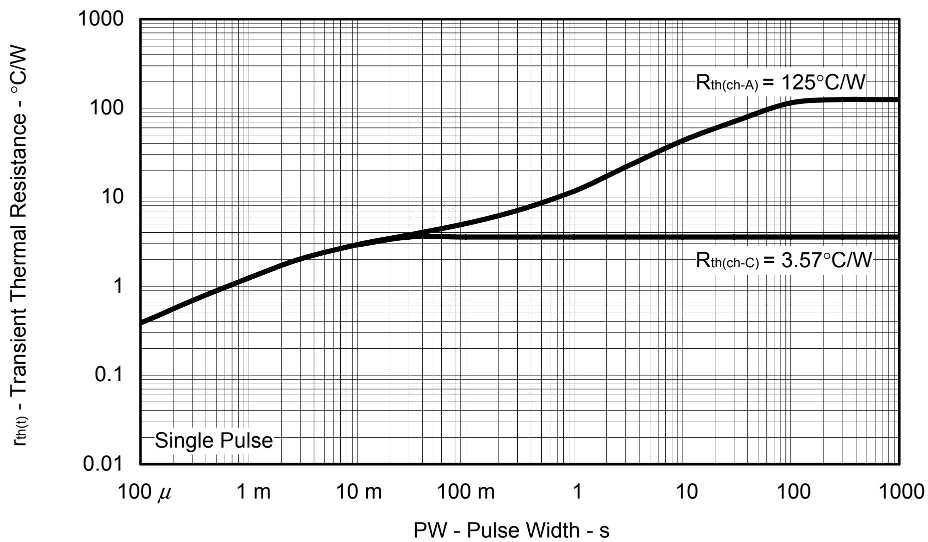
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



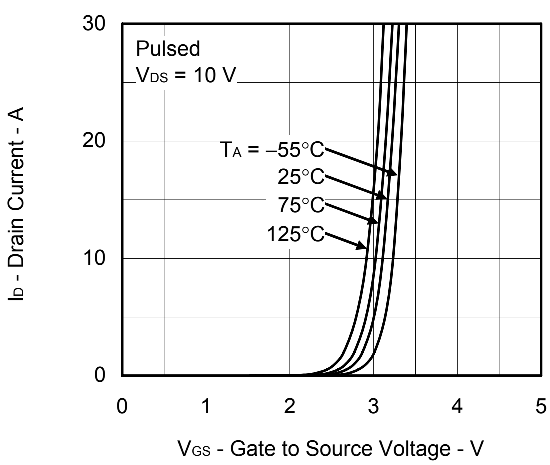
FORWARD BIAS SAFE OPERATING AREA



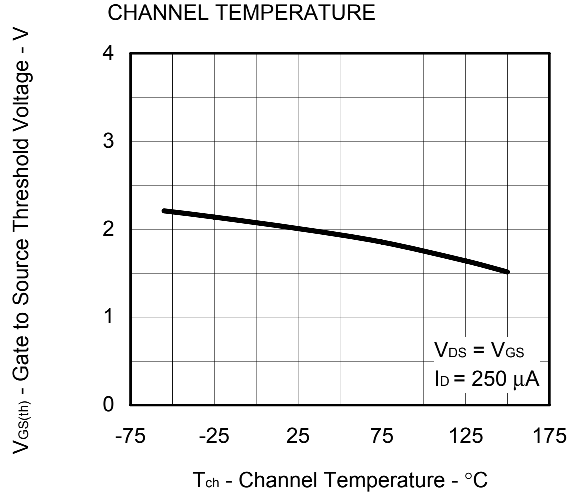
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



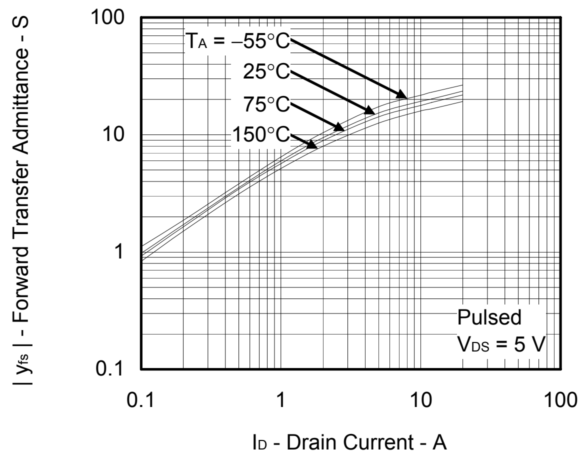
FORWARD TRANSFER CHARACTERISTICS



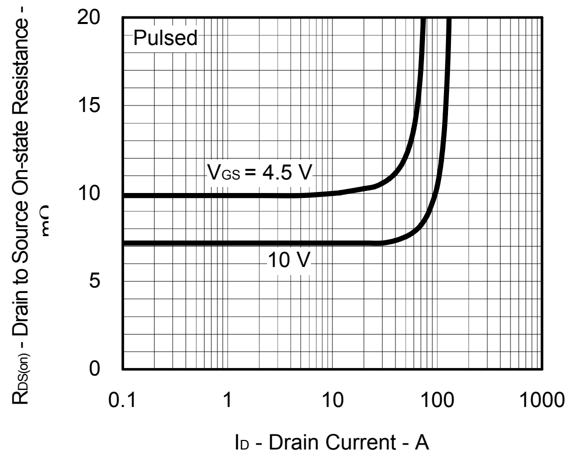
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



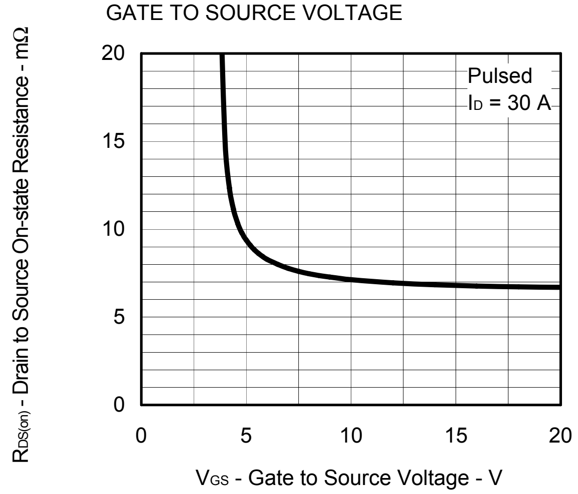
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



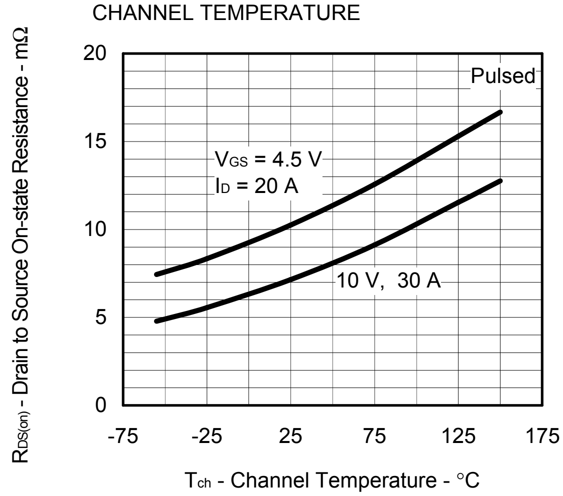
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



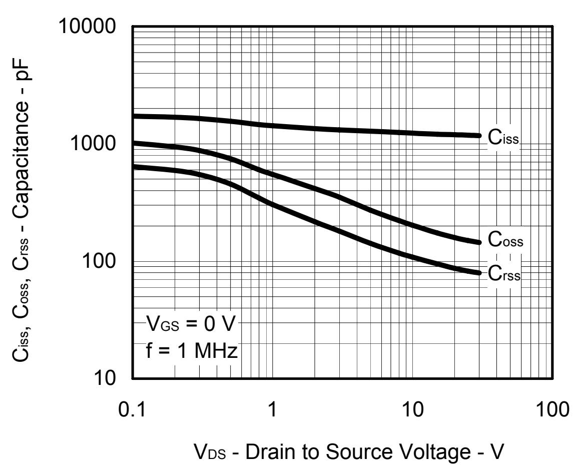
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



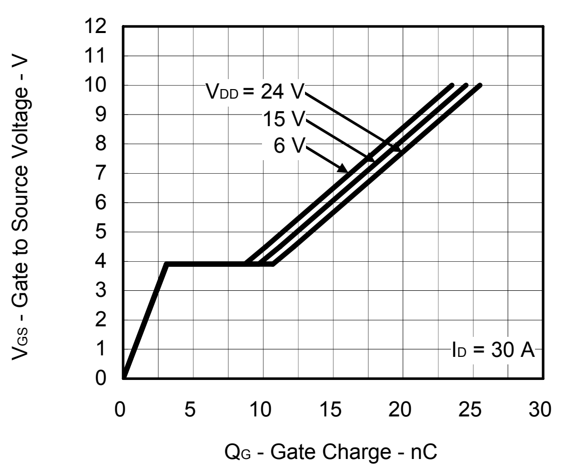
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



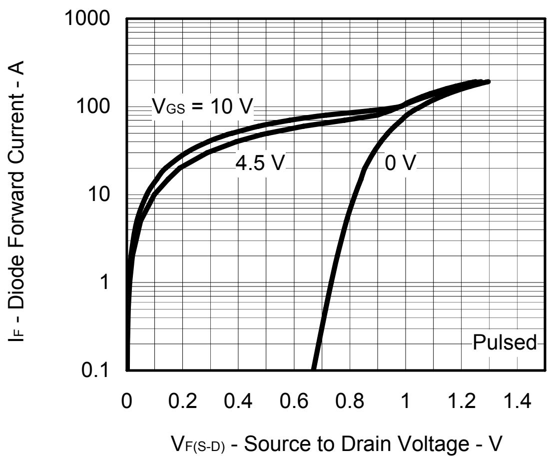
CAPACITANCE vs. DRAIN TOSOURCE VOLTAGE



DYNAMIC INPUT CHARACTERISTICS

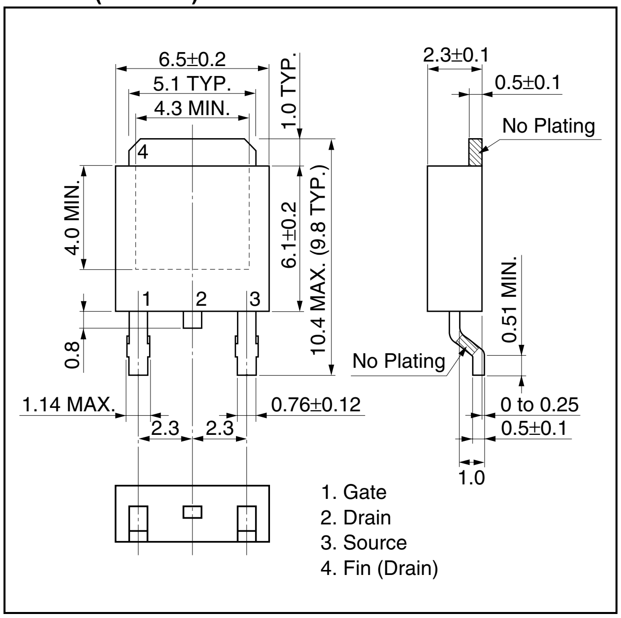


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

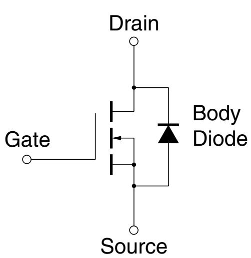


PACKAGE DRAWINGS (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.