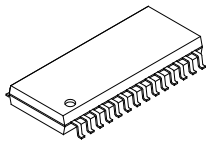
SONY

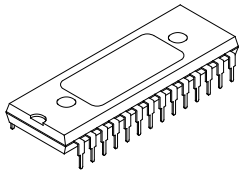
CXL1008M/P

CMOS-CCD Signal Processor for Skew Compensation

CXL1008M
28 pin SOP (Plastic)



CXL1008P
28 pin DIP (Plastic)



Description

CXL1008M/P are CMOS-CCD signal processors developed for the variable-speed video signal processor for home-use 8mm VCRs.

Features

- Low power consumption 105mW (Typ.)
- Built-in peripheral circuit
- Adjustment is necessary for one part.

Structure

CMOS-CCD

Functions

- 1/2H 359-bit, direct 20-bit CCD register
- Clock driver
- Timing oscillation circuit
- Automatic bias circuit
- Sync tip clamp circuit
- Dummy VD insert circuit
- Sample/hold circuit

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	11	V
	V_{CL}	6	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipaiton			
	P_D	CXL1008M 500	mW
		CXL1008P 1000	mW

Recommended Operating Conditions

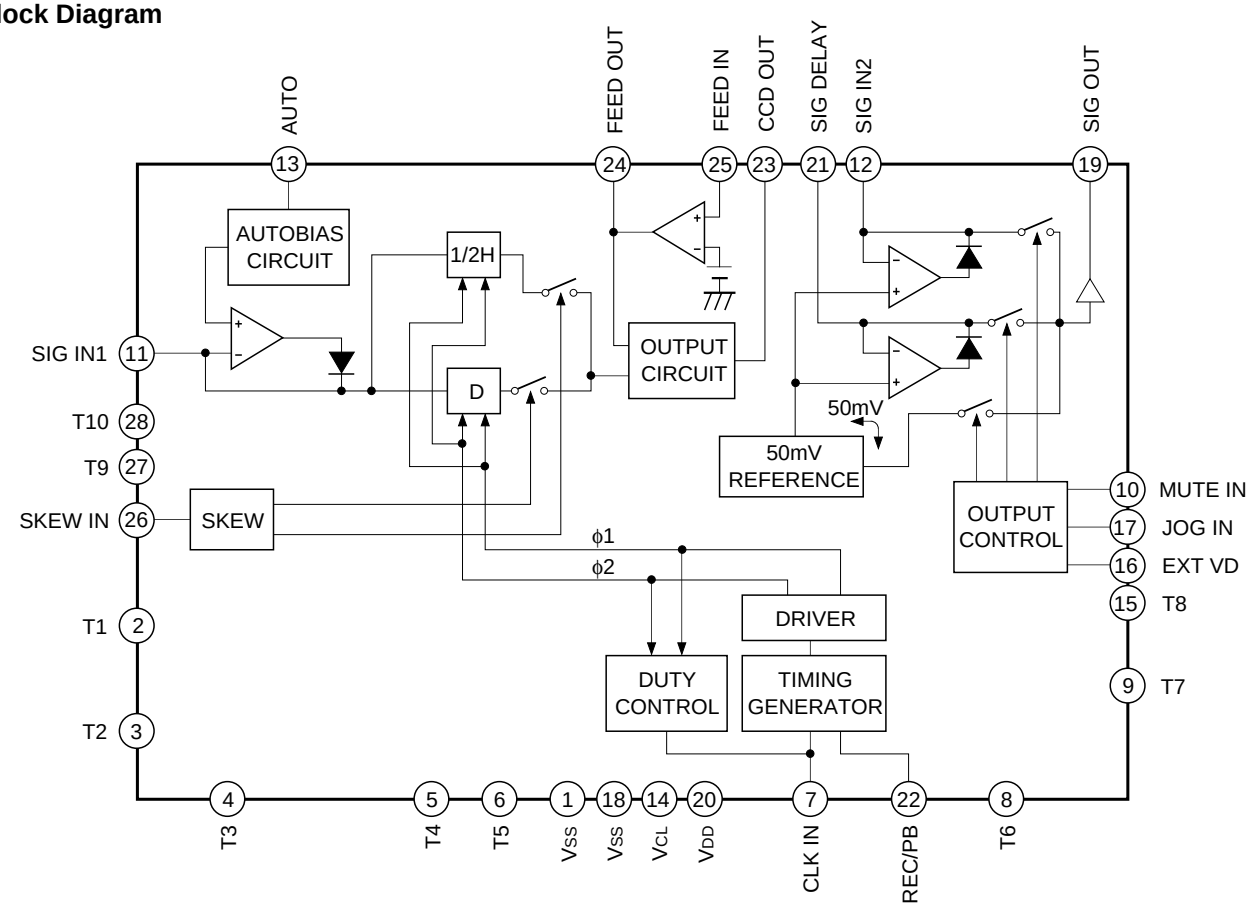
Supply voltage	V_{DD}	9V ± 5	%
	V_{CL}	5V ± 5	%

Recommended Clock Conditions

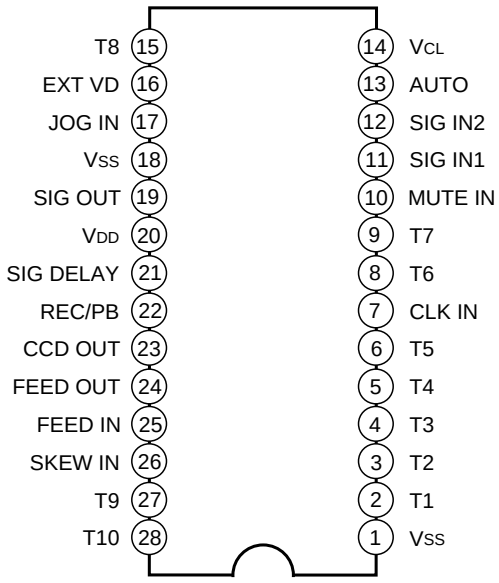
• Clock input amplitude	V_{CLK}	0.15 to 1.0 (0.3 Typ.)	Vp-p
• Clock frequency	f_{CLK}	10.738635	MHz

E60248-PS

Block Diagram



Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Supply voltage	Description	Impedance (Ω)
1	V_{SS}			GND	
7	CLK IN	I	0.3Vp-p	Input the sine wave of 3fsc (10.738635MHz)	> 50k
10	MUTE IN	I	5V when muting, normally 0V	The video signal mute is generated at High level. See the Logic Table of Signal Output Selection State (Table 1).	> 100k
11	SIG IN1	I	1.1Vp-p or less	Signal input pin of CCD DL. Input composite video signal.	> 100k
12	SIG IN2	I	2.2Vp-p or less	Signal input pin of the through side. Input composite video signal.	> 100k
13	AUTO	O		The DC level of automatic bias is output.	10k
14	V_{CL}		+5V	Power supply 1	
16	EXT VD	I	5V when VD is inserted	Use this pin when VD is inserted to the video signal with the extrenal dummy VD signal input.	> 100k
17	JOG IN	I	JOG mode 5V PB/REC mode 0V	JOG/NORMAL PB selection pin. See the Logic Table of Signal Output Selection State (Table 1).	> 100k
18	V_{SS}			GND	
19	SIG OUT	O		Final output	0.6 to 1.5k
20	V_{DD}		+9V	Power supply 2	
21	SIG DELAY	I		After the output from Pin 23 CCD OUT passes through LPF, input it to the same pin and insert clamp and VD.	> 100k
22	REC/PB	I	5V when PB 0V when REC	Operate the clock at High when PB. Stop the clock at Low when REC.	> 100k
23	CCD OUT	O		Direct output from CCD DL	0.6 to 1.5k
24	FEED OUT	O		Feedback DC output	10k
25	FEED IN	I		Smoothing capacitor connection pin of the bias commutation loop on the output circuit	> 100k
26	SKEW IN	I		Select Direct DL and 1/2H DL signals when High and Low, respectively. See the Logic Table of CCD DL Mode Selection (Table 2).	> 100k

Note) T1 through T10 test pins must be connected as shown in the application circuit because of the IC internal circuit.

Notes on Handling

Countermeasures for electrostatics are necessary because some pins have low electrostatic strength (particularly Pin 26: SKEW IN).

Electrical Characteristics

(See the Electrical Characteristics Test Circuit) (Ta = 25°C, V_{DD} = 9.0V, V_{CL} = 5.0V, f_{CLK} = 10.7MHz, V_{CLK} = 0.3Vp-p sine wave)

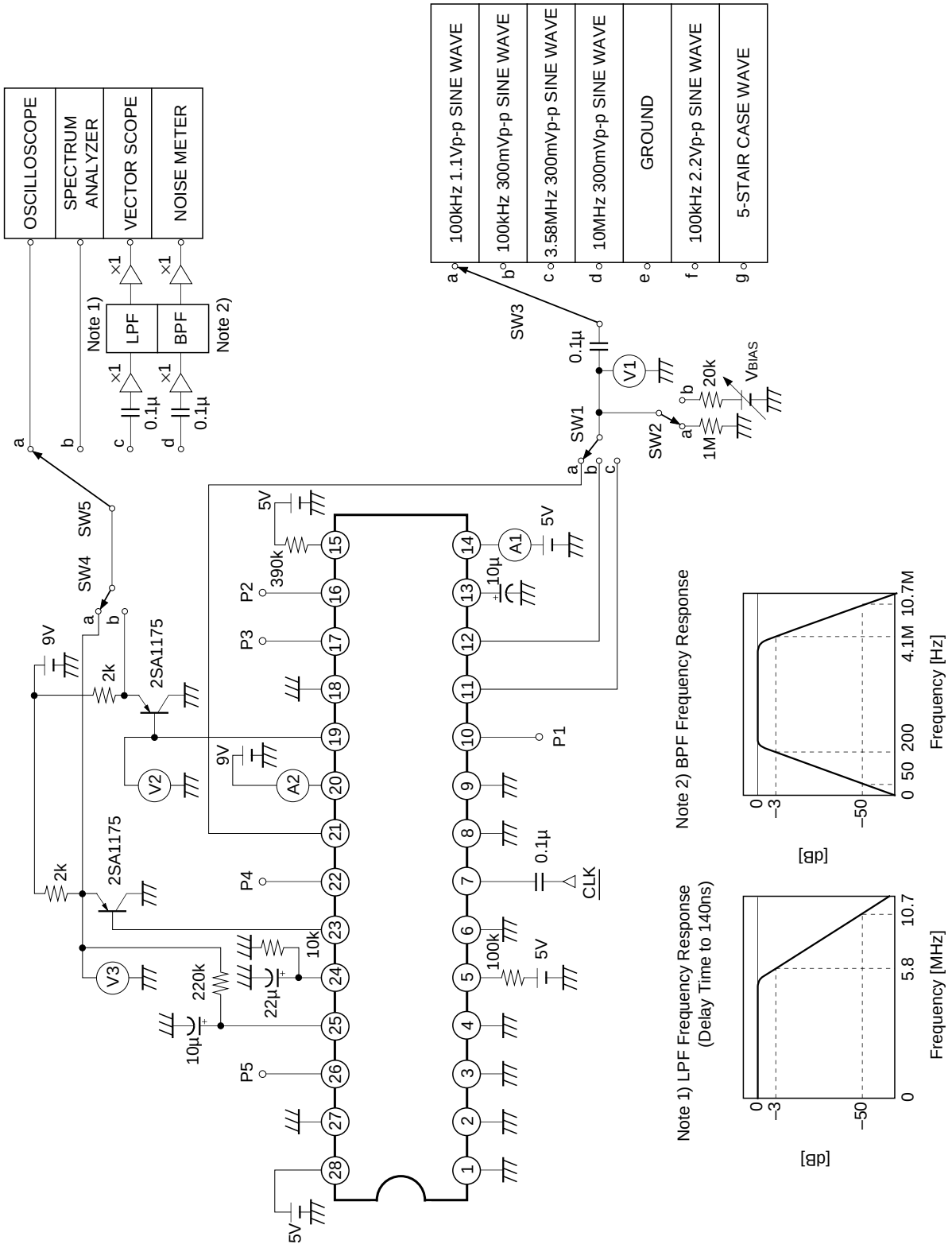
Items	Symbol	Test Conditions	Switch Conditions					Control Pin Conditions *1, *2					Min.	Typ.	Max.	Unit	Note
			1	2	3	4	5	P1	P2	P3	P4	P5					
Power current	I_{DD}	PB, JOG	c	a	a						H			7	12	mA	1
	I_{CL}		c	a	a						H			8	10	mA	1
Clock input level	CLK										H		0.15	0.3	1.0	V	
Signal input pin voltage	Vdi1		c	a	e						H		4.0	5.0	6.0	V	2
	Vdi2		b	a	e								4.0	4.2	4.4	V	2
	Vdi3		a	a	e								4.0	4.2	4.4	V	2
Signal output pin voltage	Vdo1		c	a	e						H		1.7	2.0	2.4	V	3
	Vdo2		b	a	e			L	L	L			1.5	2.0	2.5	V	3
CCD signal output voltage difference	ΔDab	Direct ↔ 1/2H	c	a	e	a	a				H	H ↔ L	–55	0	55	mV	4
Signal insert gain	IG_{CCD}		c	b	a	a	a				H		–3.0	0	3.0	dB	5
	IG_{In2}		b	b	f	b	a	L	L	L			–1.2	–0.8	0	dB	5
	IG_{DL}		a	b	f	b	a	L	L	H			–1.2	–0.8	0	dB	5
CCD output signal gain difference	ΔGab	Direct ↔ 1/2H	c	b	a	a	a				H	H ↔ L	–1.3	0	1.3	%	6
Frequency characteristics	f_{CCD}	3.58MHz/100kHz	c	b	b ↔ c	a	b				H		–3	–2	0	dB	7
	f_{In2}	10MHz/100kHz	b	b	b ↔ d	b	b	L	L	L			–0.5	0	—	dB	8
	f_{DL}	10MHz/100kHz	a	b	b ↔ d	b	b	L	L	H			–0.5	0	—	dB	8
Frequency characteristics difference	Δfab	Direct ↔ 1/2H at 3.58MHz	c	b	b ↔ c	a	b				H	H ↔ L	–0.2	0	0.2	dB	9
Differential gain	DG_{CCD}	1.1Vp-p input	c	b	g	a	c				H		0	3	10	%	10
	DG_{In2}	2.2Vp-p input	b	b	g	b	c	L	L	L			0	2	4	%	10
	DG_{DL}	2.2Vp-p input	a	b	g	b	c	L	L	H			0	2	4	%	10

Items	Symbol	Test Conditions	Switch Conditions					Control Pin Conditions *1, *2					Min.	Typ.	Max.	Unit	Note
			1	2	3	4	5	P1	P2	P3	P4	P5					
Differential phase	DP_{CCD}	1.1Vp-p input	c	b	g	a	c				H		0	3	5	deg	10
	DP_{In2}	2.2Vp-p input	b	b	g	b	c	L	L	L			0	3	5	deg	10
	DP_{DL}	2.2Vp-p input	a	b	g	b	c	L	L	H			0	3	5	deg	10
Allowable input amplitude	V_{IN1-AC}		c		g								—	—	1.1	Vp-p	
	V_{IN2-AC}		a/b		g								—	—	2.2	Vp-p	
S/N rate	S/N_{CCD}		c	b	a ↔ e	a	d				H		50	55	—	dB	11
	S/N_{In2}		b	b	f ↔ e	b	d	L	L	L			50	65	—	dB	11
	S/N_{DL}		a	b	f ↔ e	b	d	L	L	H			50	65	—	dB	11
VD insert depth	V_{VD}	2Vp-p video signal from sync tip	a	a	g	b	a	L	⎍	H			0	50	100	mV	12
Logical input	$V_{IN\,H}$												4.0		—	V	
	$V_{IN\,L}$												—		1.0	V	

*1 Control pins correspond to P1 through P5 of the Electrical Characteristics Test Circuit.

*2 Symbols "H" and "L" in control pin conditions represent "$V_{IN\,H}$" and "$V_{IN\,L}$" of logical input.

Electrical Characteristics Test Circuit

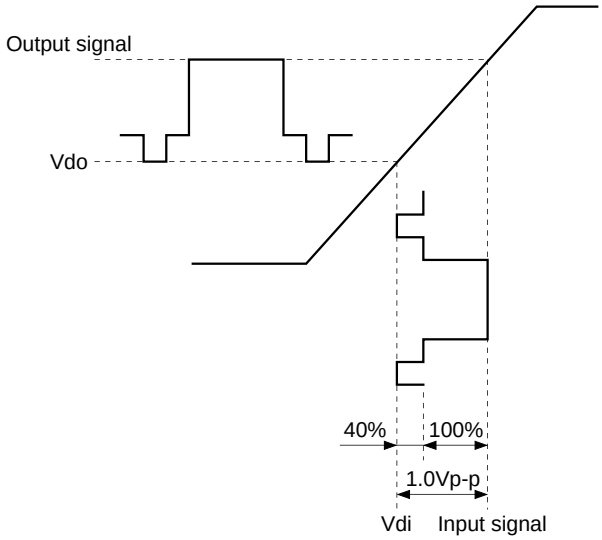


Notes)

1) Current value when the clock is in operation in the PB or JOG mode.
In the REC mode, the clock is stopped (Pin 22 is at low) to save power.

2) With the signal input pin voltage value, the video signal sync tip is clamped.

3) Vdo1 is a CCD OUT output voltage when the SIG IN1 input voltage is Vdi1.
Vdo2 is a SIG OUT output voltage when the SIG IN2 input voltage is Vdi2.
Vdo1 and Vdo2 represent outputs for the sync tip clamp level when a white level signal is input as shown in the diagram.



4) ∆Dab denotes an output voltage difference of CCD OUT when the direct DL and 1/2H DL are switched.

5) IG_{CCD} is a CCD OUT gain when a 1.1Vp-p 100kHz sine wave is input to SIG IN1.

$$IG_{CCD} = 20 \log \frac{\text{Output amplitude (Vp-p)}}{\text{1.1Vp-p}}$$

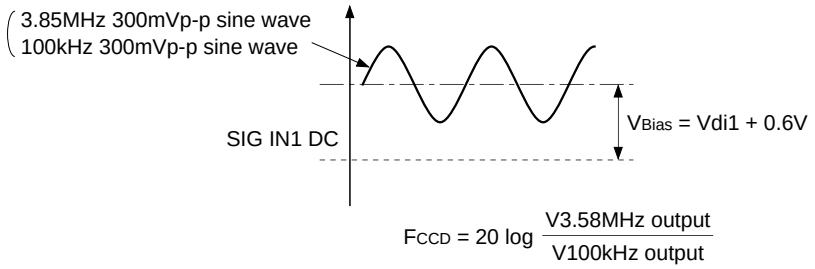
It is measured by giving a Vdi1 + 0.6 bias with V_{Bias}.
IGin2 and IG_{DL} are SIG OUT gains when 2.2Vp-p 100kHz sine wave is input to each of SIG IN2 and SIG DELAY pins.

$$IGin2 = 20 \log \frac{\text{Output amplitude (Vp-p)}}{\text{2.2Vp-p}}$$

It is measured by giving a Vdi2 + 1.1V bias with V_{Bias}.

6) ΔGab is a gain difference between the direct DL and 1/2H DL.

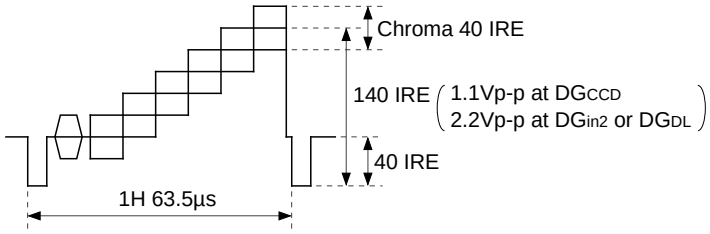
7) It represents a loss at 3.58MHz compared with 100kHz.
It is measured by raising the SIG IN1 input pin by 0.6V higher than the sync tip clamp level (Vdi1) with V_{Bias}.



8) It represents a loss at 10MHz compared with 100kHz.
It is measured by raising the SIG IN2 or SIG DELAY input pin by 1.1V higher than the sync tip clamp level (Vdi2 or Vdi3) with V_{Bias}.

9) ΔFab is a frequency response difference between the direct DL and 1/2H DL.

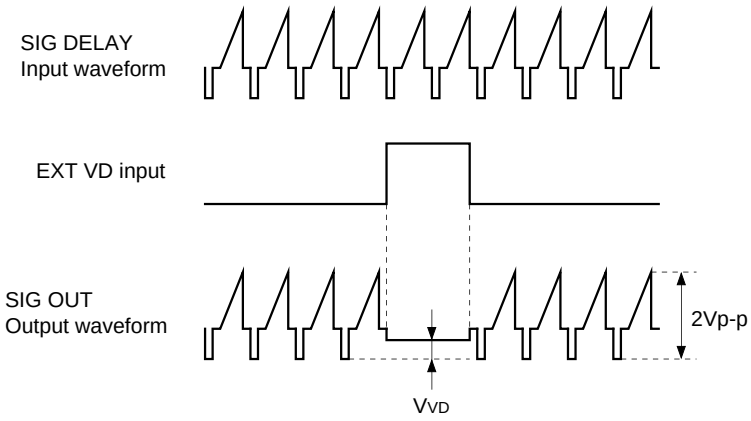
10)



DG is measured with a vectorscope in each mode of the 5-stage waves.

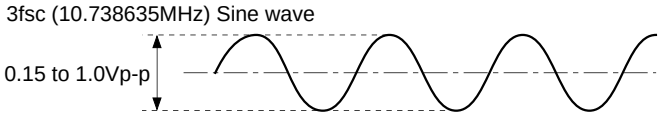
11) Measure S/N of the BPF 100kHz to 4.2MHz in the subcarrier trap mode with a video noise meter.

12)



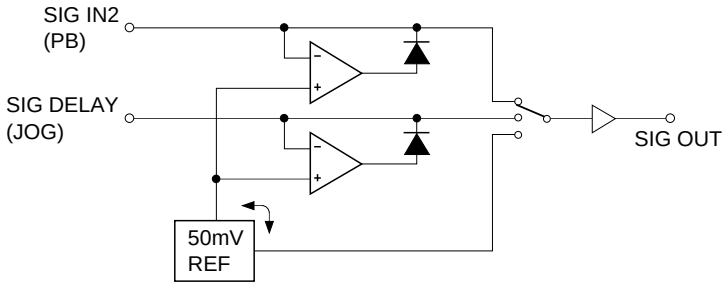
Set a voltage value at V_{VD} when inserting EXT VD to the 2Vp-p signal output waveform sync tip of SIG OUT.

CLOCK



Function Outline

Output signal selection



The video output signal is selected by selecting the output switch for three signals: Pin 10 (MUTE IN), Pin 17 (JOG IN) and Pin 16 (EXT VD).

Table 1. Logic Table of Signal Output Selection State

Input control signal state			Video signal output selection state			
JOG IN	MUTE IN	EXT VD	PB	JOG	VD insert	MUTE
0	0	0	O	×	×	×
0	0	1	O	×	×	×
0	1	0	×	×	×	O
0	1	1	×	×	×	O
1	0	0	×	O	×	×
1	0	1	×	×	O	×
1	1	0	×	×	×	O
1	1	1	×	×	O	O

Note 1) Figures "0" and "1" of the input control signal state are equivalent to "Low" and "High" of logic.

Note 2) Items marked with the symbol "O" in the video signal output selection state are selected.

Note 3) PB = $\overline{\text{JOG IN}} \cdot \overline{\text{MUTE IN}}$

JOG = JOG IN $\cdot \overline{\text{MUTE IN}} \cdot \overline{\text{EXT VD}}$

VD insert = JOG IN $\cdot$ EXT VD

MUTE = MUTE IN

CCD selection

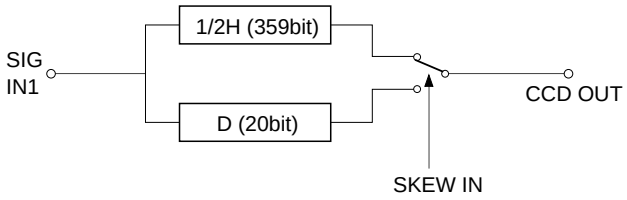
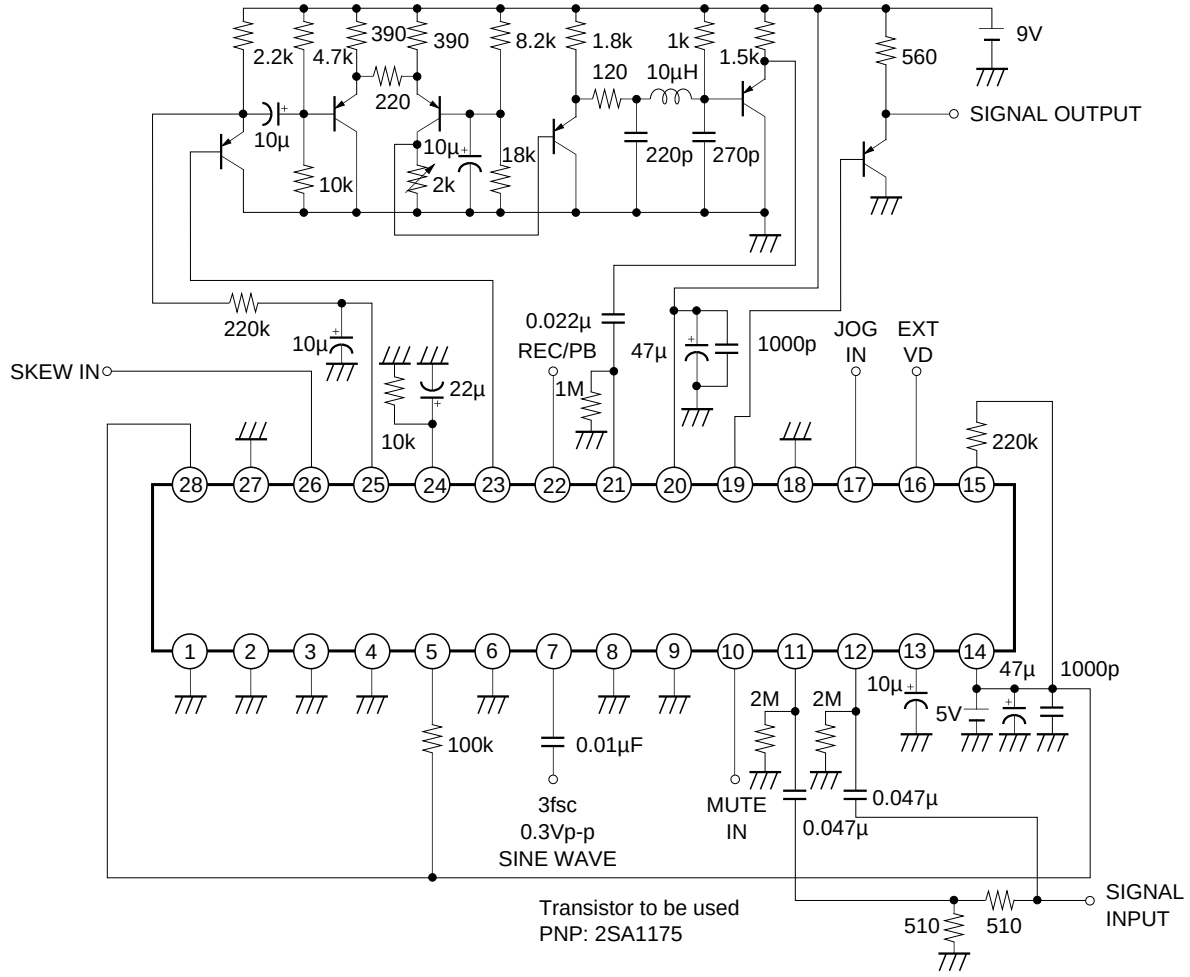


Table 2. Logic Table of CCD DL Mode Selection

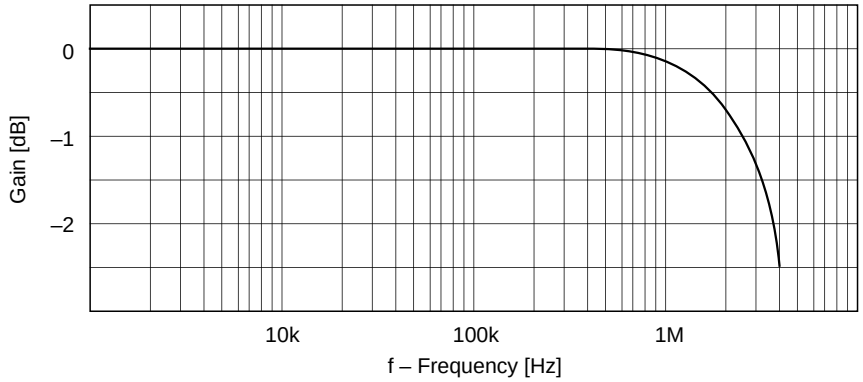
Control signal	CCD DL mode	
SKEW IN	D	1/2H
0	×	O
1	O	×

Application Circuit

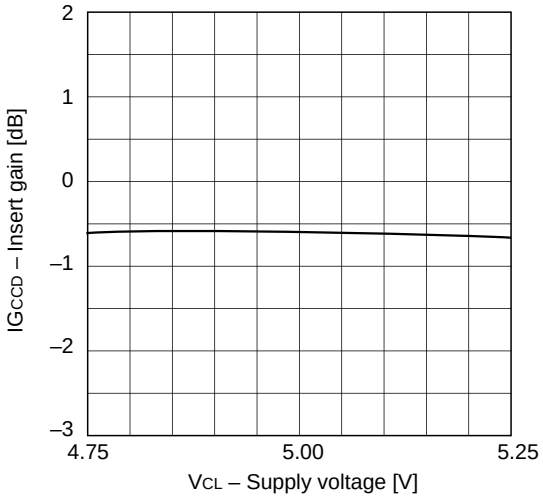


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

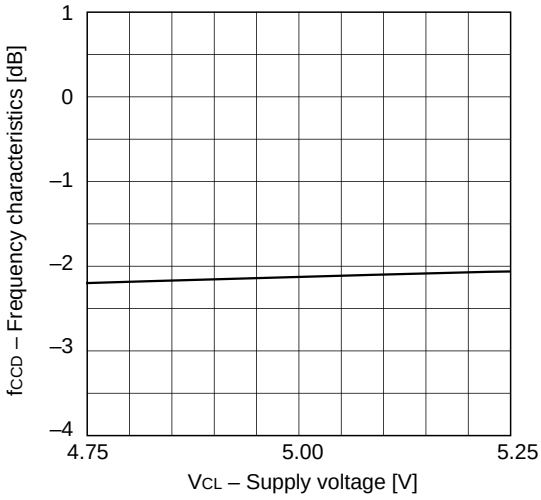
Frequency characteristics (Ta = 25°C)



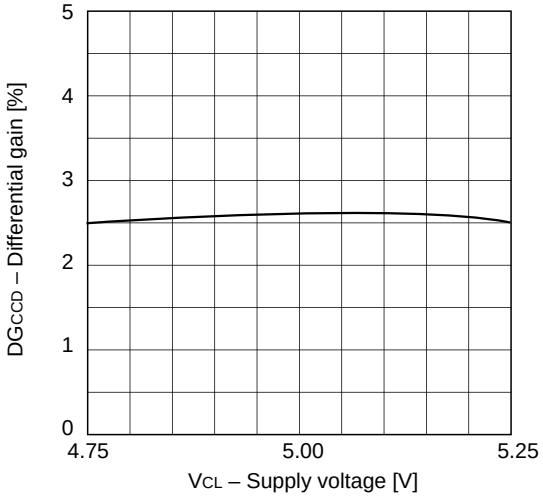
Supply voltage (V_{CL}) vs. Insert gain (IG_{CCD})



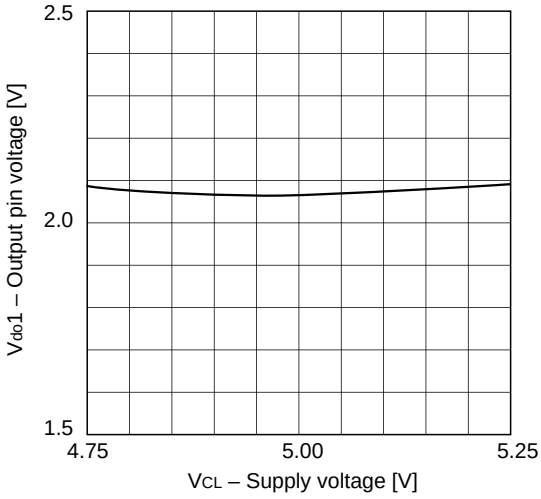
Supply voltage (V_{CL}) vs. Frequency characteristics (f_{CCD})



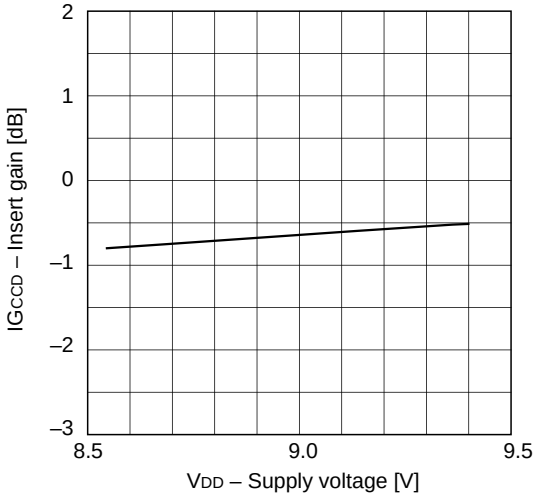
Supply voltage (V_{CL}) vs. Differential gain (DG_{CCD})



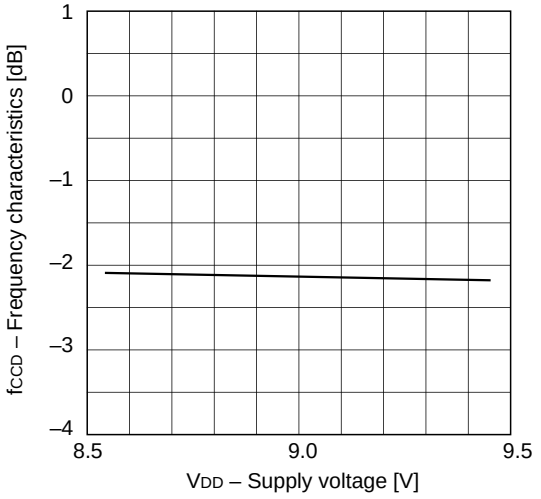
Supply voltage (V_{CL}) vs. Output pin voltage ($V_{do}1$)



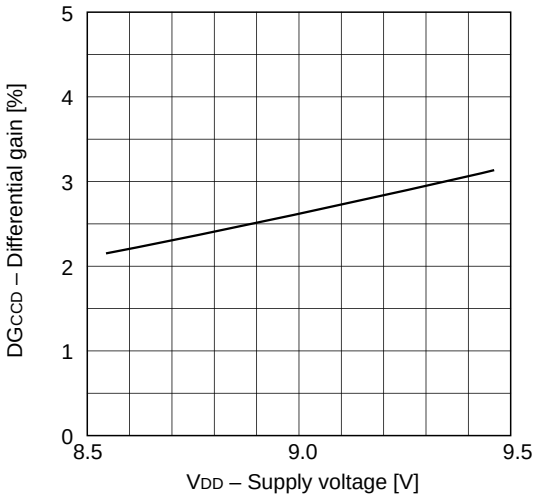
Supply voltage (V_{DD}) vs. Insert gain (IG_{CCD})



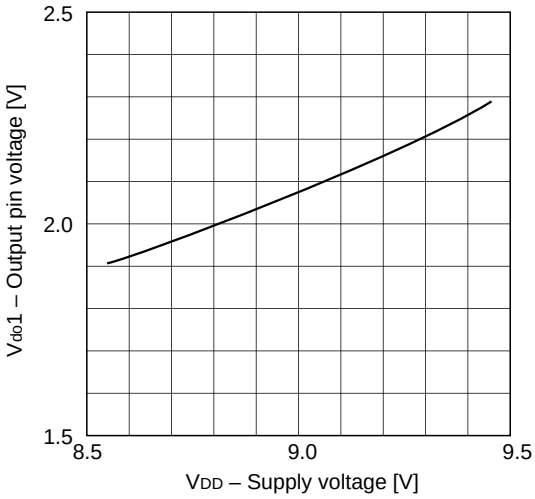
Supply voltage (V_{DD}) vs. Frequency characteristics (f_{CCD})



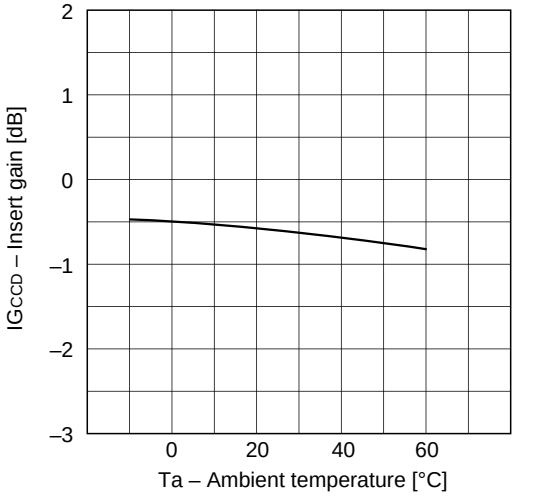
Supply voltage (V_{DD}) vs. Differential gain (DG_{CCD})



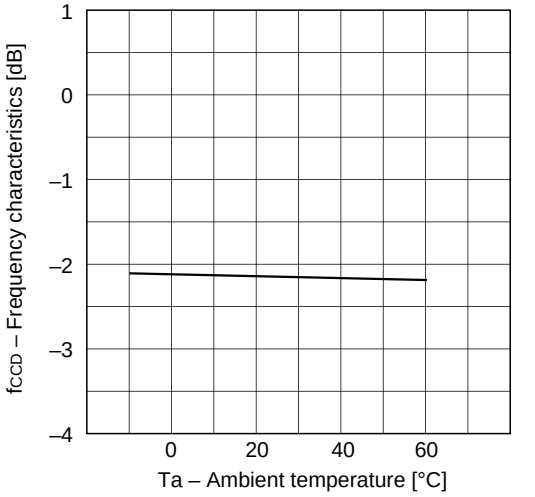
Supply voltage (V_{DD}) vs. Output pin voltage ($V_{do}1$)



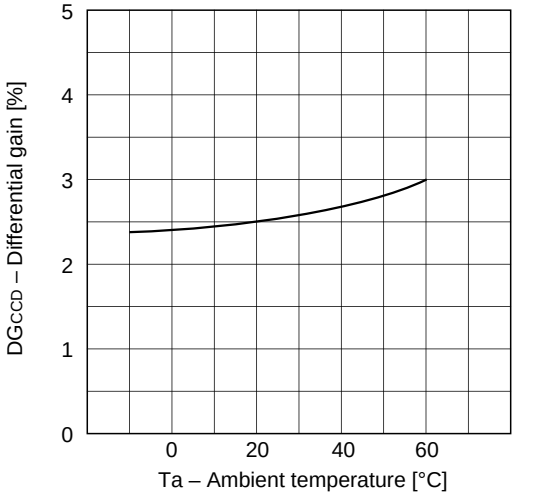
Ambient temperature (Ta) vs. Insert gain (IG_{CCD})



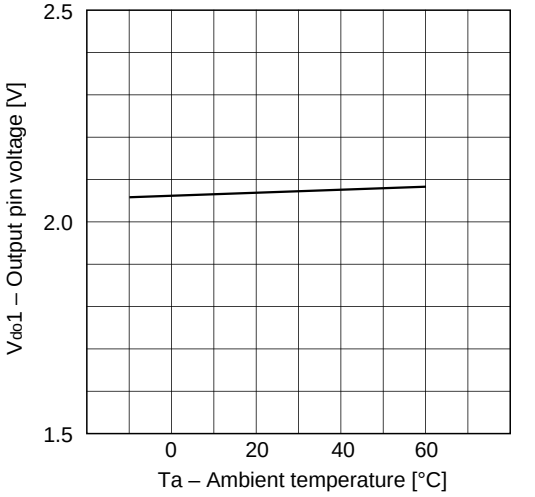
Ambient temperature (Ta) vs. Frequency characteristics (f_{CCD})



Ambient temperature (Ta) vs. Differential gain (DG_{CCD})



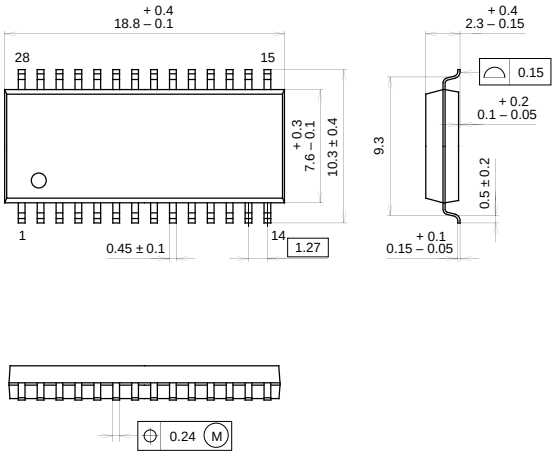
Ambient temperature (Ta) vs. Output pin voltage ($V_{do}1$)



Package Outline Unit: mm

CXL1008M

28PIN SOP (PLASTIC)



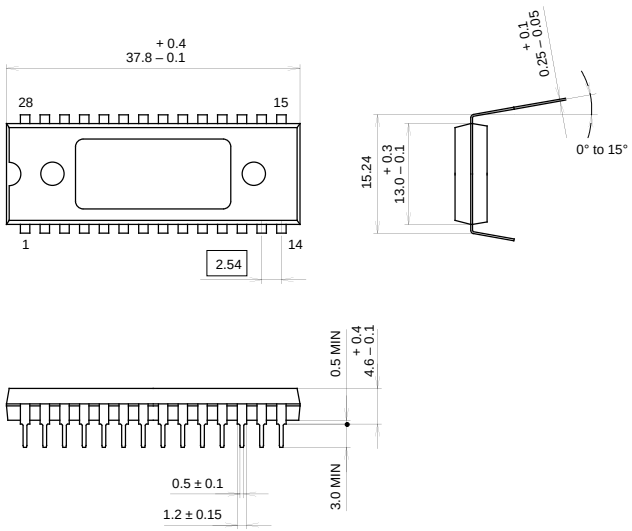
PACKAGE STRUCTURE

SONY CODE	SOP-28P-L02
EIAJ CODE	SOP028-P-0375
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.6g

CXL1008P

28PIN DIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.Center part is mirror surface.

PACKAGE STRUCTURE

SONY CODE	DIP-28P-03
EIAJ CODE	DIP028-P-0600
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	4.2g